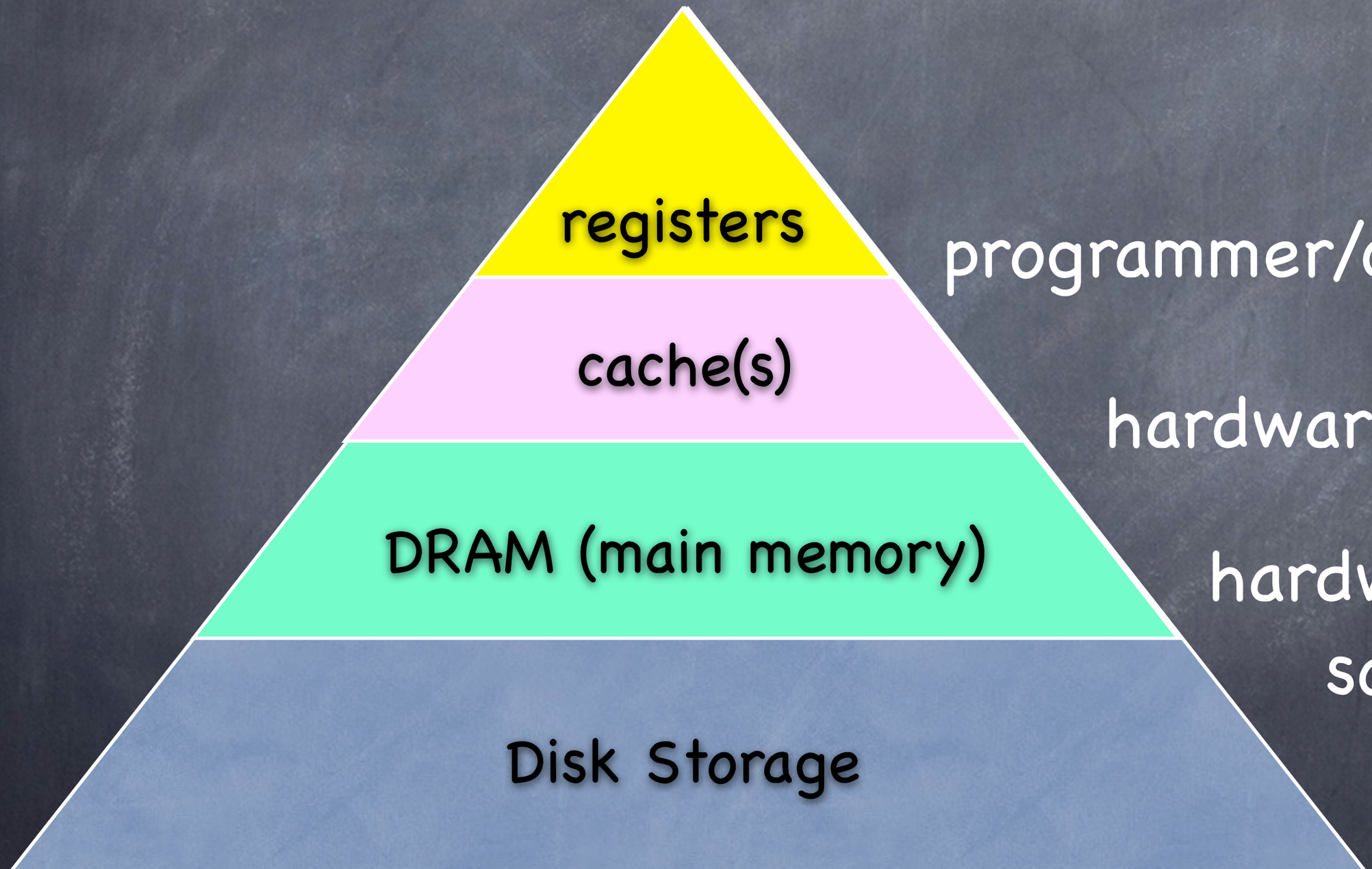
Announcements

TA Application Time - Due today

(No longer optional) ARM Reading linked off labs page (Look at D.7 and D.8)


registers
cache(s)
DRAM (main memory)
Disk Storage
programmer/compiler
hardware
hardware + O.S.
software

Traps / Exceptions

- Divide by zero
- Invalid operation code
- Segmentation fault
- Reference to invalid page table entry
- Syscall

Exception Handling Approaches

- Branch to "fixed" address
  - Actually fixed
  - Address stored in fixed address (typically low or high addresses in memory).
  - Address stored in special register
- Save information including PC where error occurred (like bal saves return address).
- Enter supervisor mode!

Privileged Modes

- Most processors have a register indicating current mode:
  - user mode
  - supervisor mode
- Can only set page table address register in supervisor mode ==> memory protection
- Can only set mode register in supervisor mode!

2.7. Operating modes

In all states there are seven modes of operation:

- User mode is the usual ARM program execution state, and is used for executing most application programs
- *Fast interrupt* (FIQ) mode is used for handling fast interrupts
- *Interrupt* (IRQ) mode is used for general-purpose interrupt handling
- Supervisor mode is a protected mode for the operating system
- Abort mode is entered after a data or instruction Prefetch Abort
- System mode is a privileged user mode for the operating system
- Undefined mode is entered when an Undefined instruction exception occurs.

Modes other than User mode are collectively known as privileged modes.

Table 2-4 Exception vectors

Exception	Vector address
Reset	0x00000000
Undefined instruction	0x00000004
SWI	0x00000008
Prefetch Abort	0x0000000C
Data Abort	0x00000010
Reserved	0x00000014
IRQ	0x00000018
FIQ	0x0000001C

All modes	FIQ mode only	Supervisor mode only	Abort mode only	IRQ mode only	Undefined mode only
r0					
r1					
r2					
r3					
r4					
r5					
r6					
r7					
r8	r8_fiq				
r9	r9_fiq				
r10	r10_fiq				
r11	r11_fiq				
r12	r12_fiq				
r13 (SP)	r13_fiq	r13_svc	r13_abt	r13_irq	r13_und
r14 (LR)	r14_fiq	r14_svc	r14_abt	r14_irq	r14_und
r15 (PC)					
CPSR	SPSR_fiq	SPSR_svc	SPSR_abt	SPSR_irq	SPSR_und

16 general-purpose registers

15 banked general-purpose registers

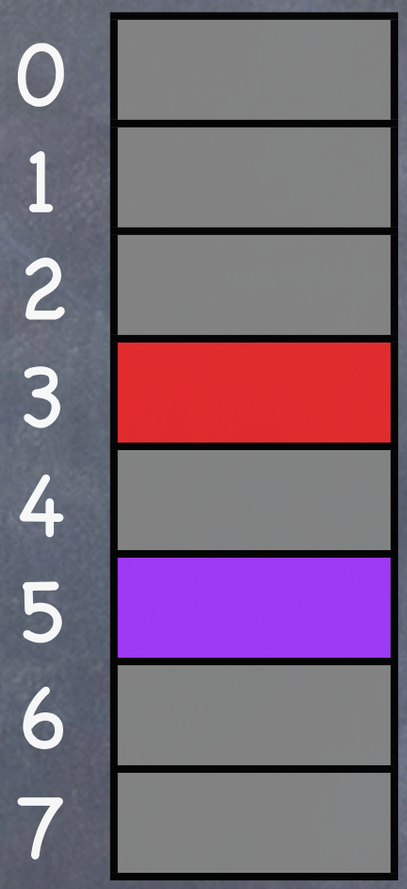
Current Program Status Register

Five banked Saved Program Status Registers

Figure 2-1 ARM968E-S register set

Program 1's Virtual Addr Space

Program 2's Virtual Addr Space

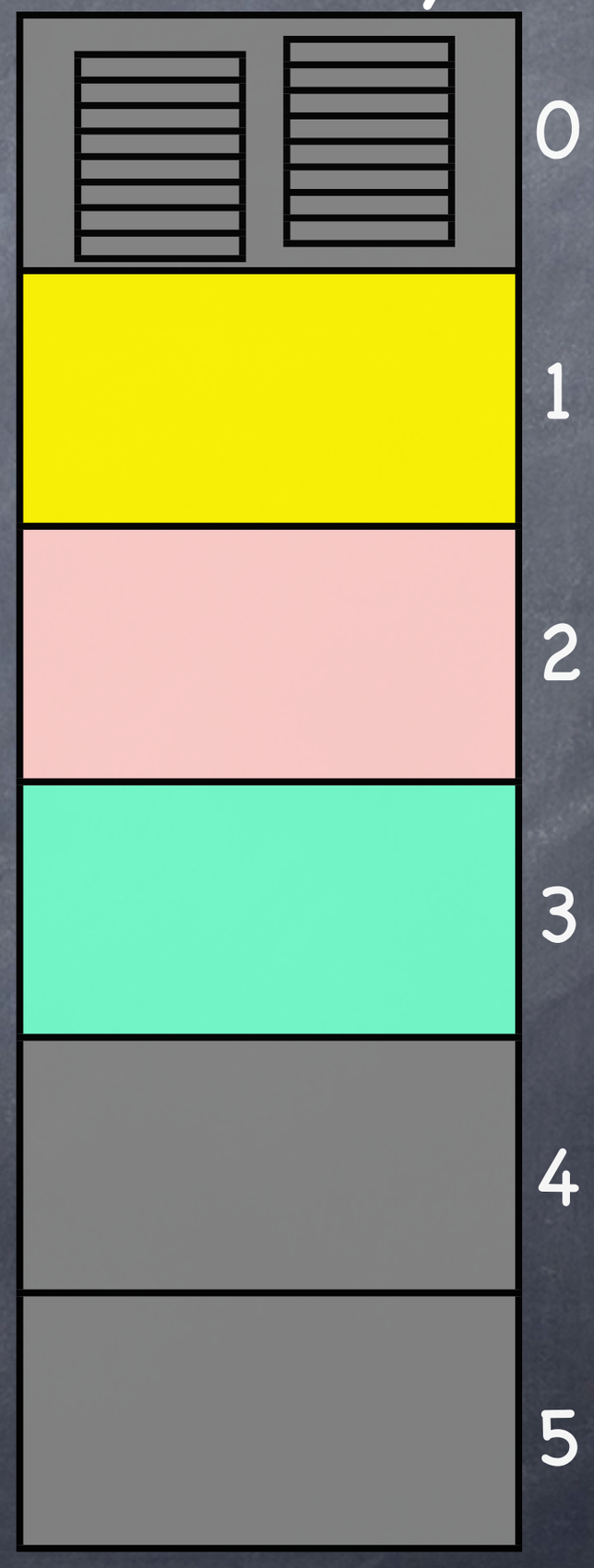


Real/Physical Memory

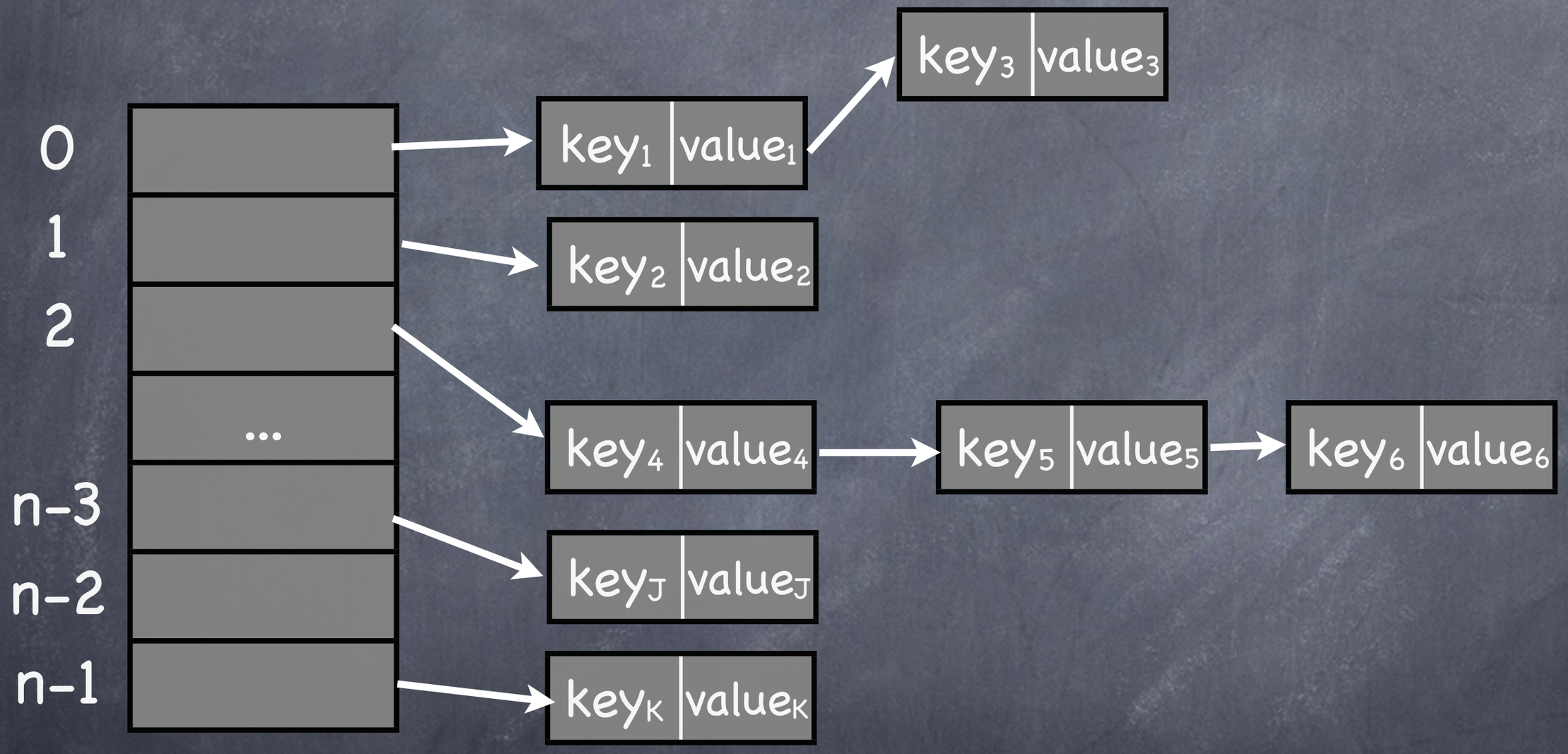
Program's virtual address space divided into pages

Gray pages in virt. addr. space are stored on disk

Real/Physical Memory

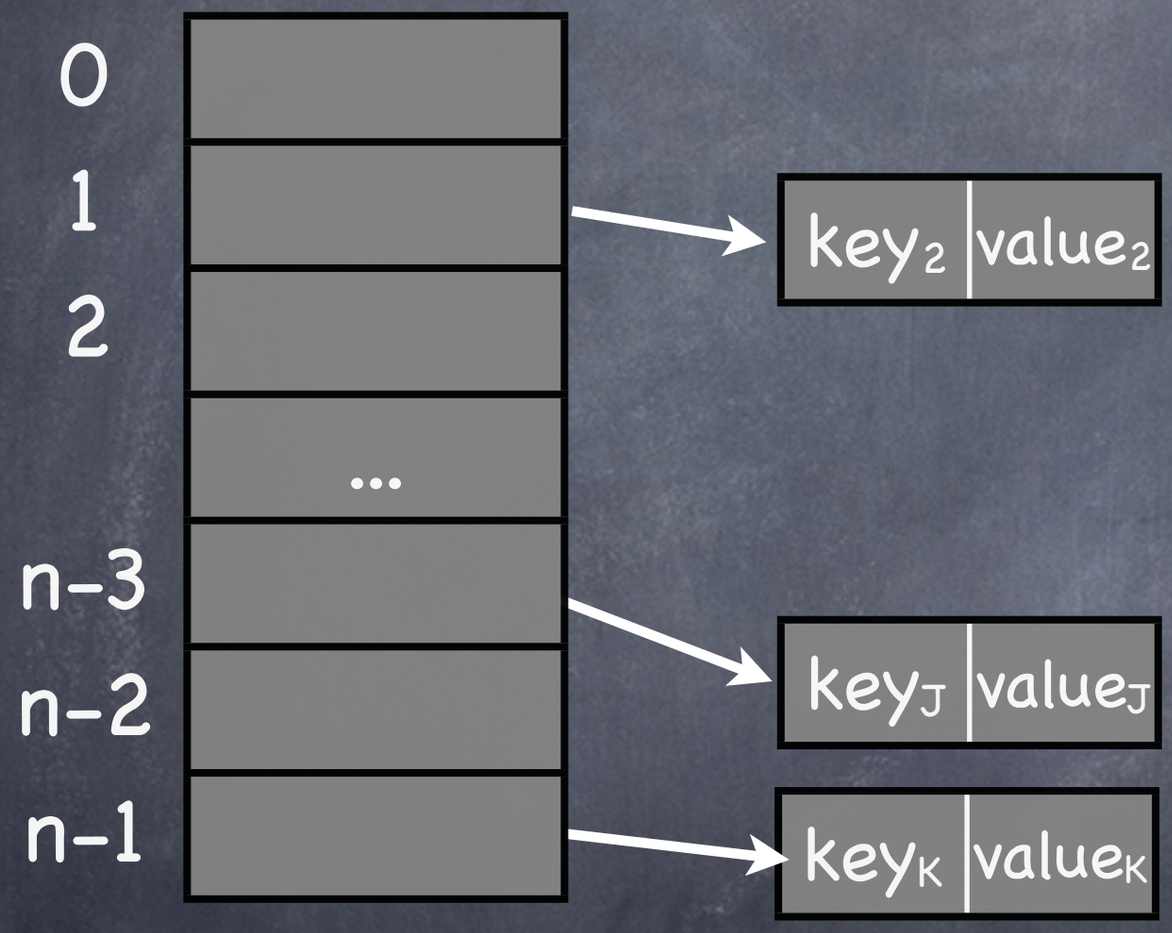


Hash vs. Page Table



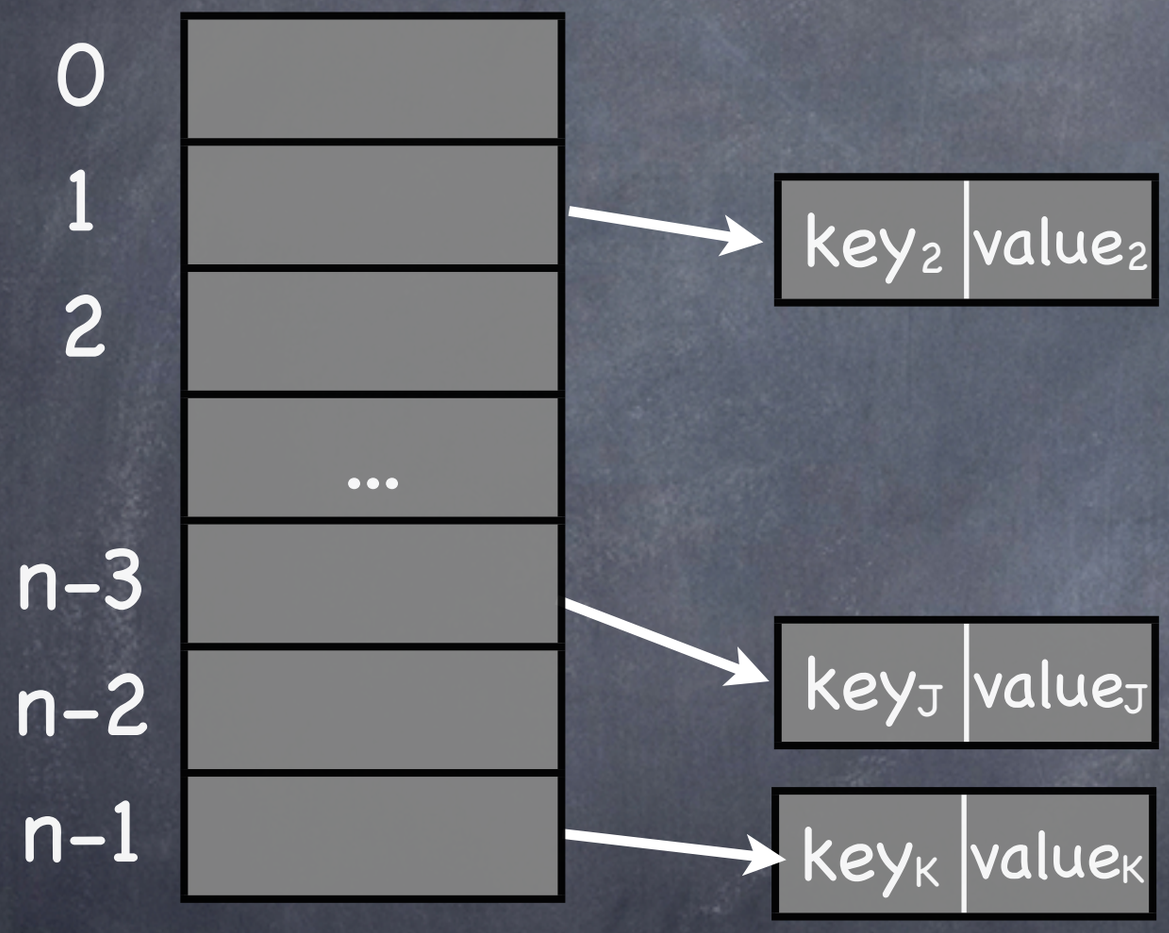
- Can't afford to traverse chains
- Can't afford to discard entries!

Sparse Hash = Page Table



- Let n = number of pages in address space

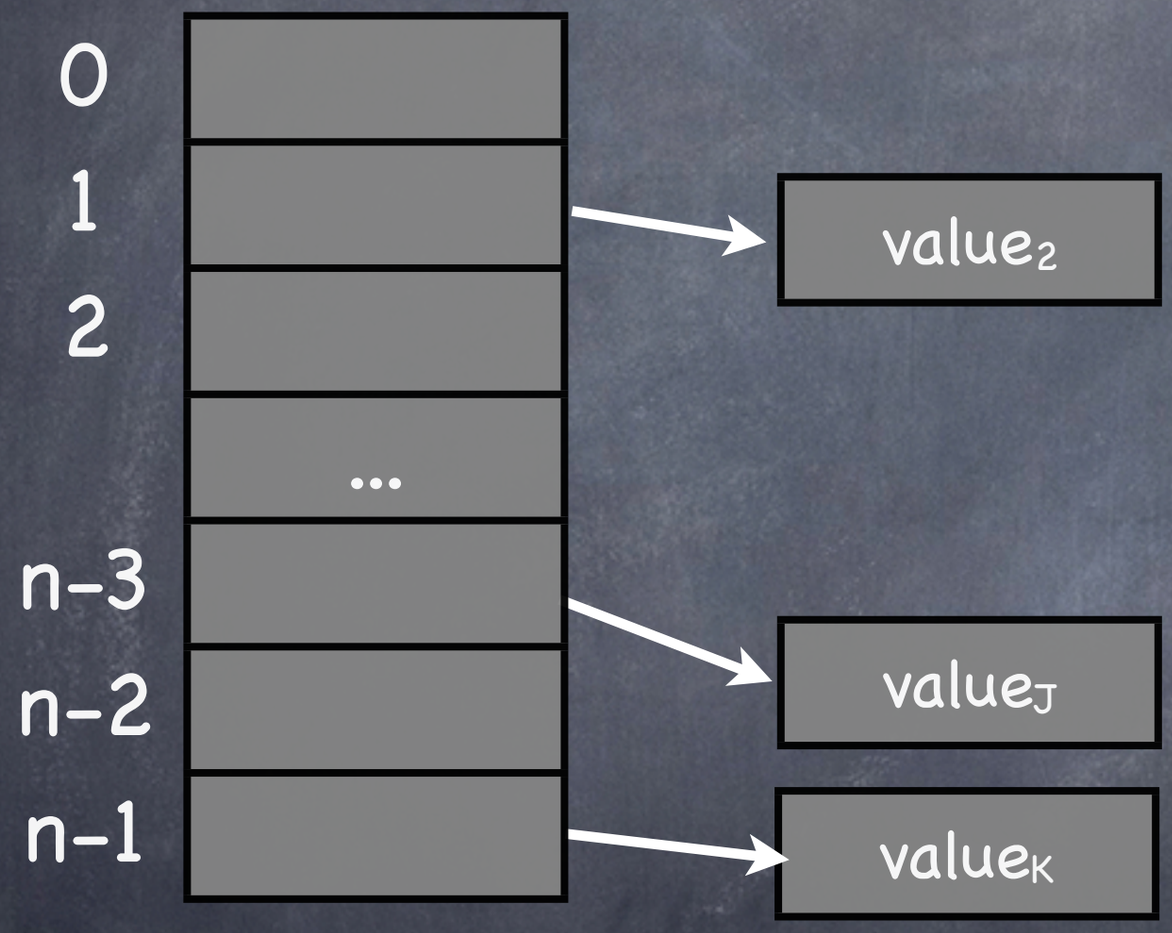
Sparse Hash = Page Table



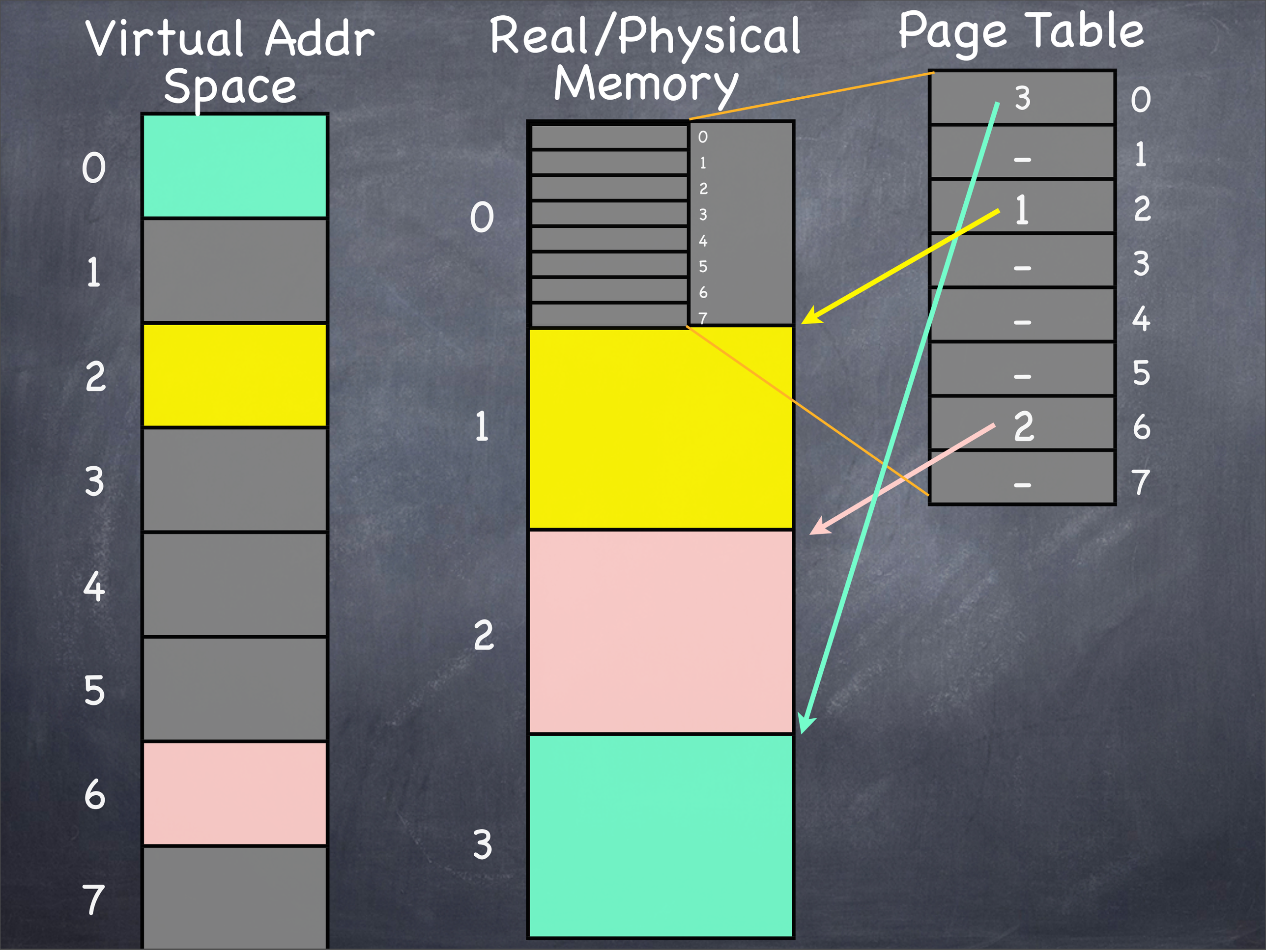
hash(x) = x !

- Let n = number of pages in address space

Sparse Hash = Page Table

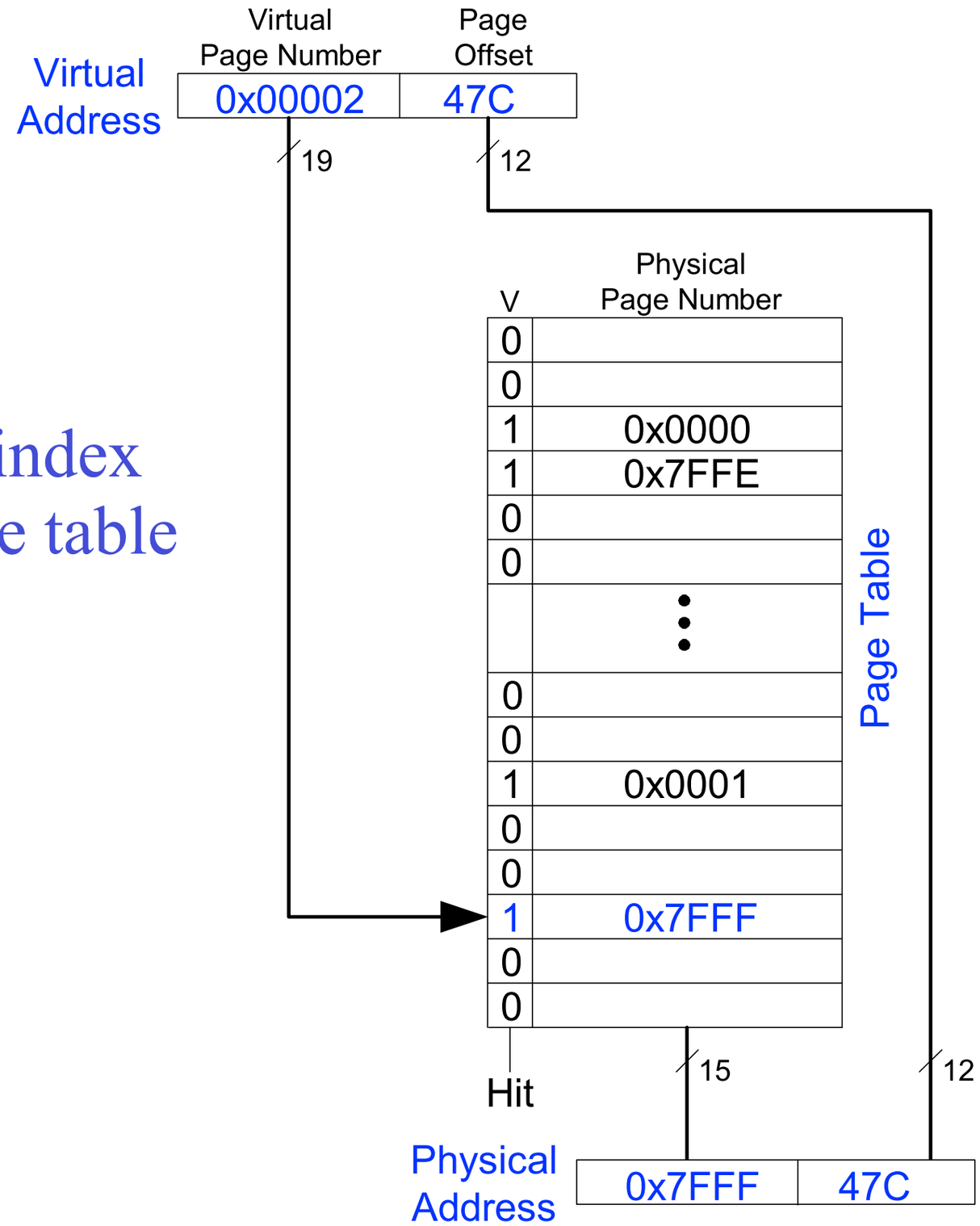


- "Values" in key/value pairs of page table are huge. Can't afford to put them inline.


Virtual Addr Space
0
1
2
3
4
5
6
7
Real/Physical Memory
0
1
2
3
0
1
2
3
4
5
6
7
Page Table
3
–
1
–
–
–
2
–
0
1
2
3
4
5
6
7

Page Table

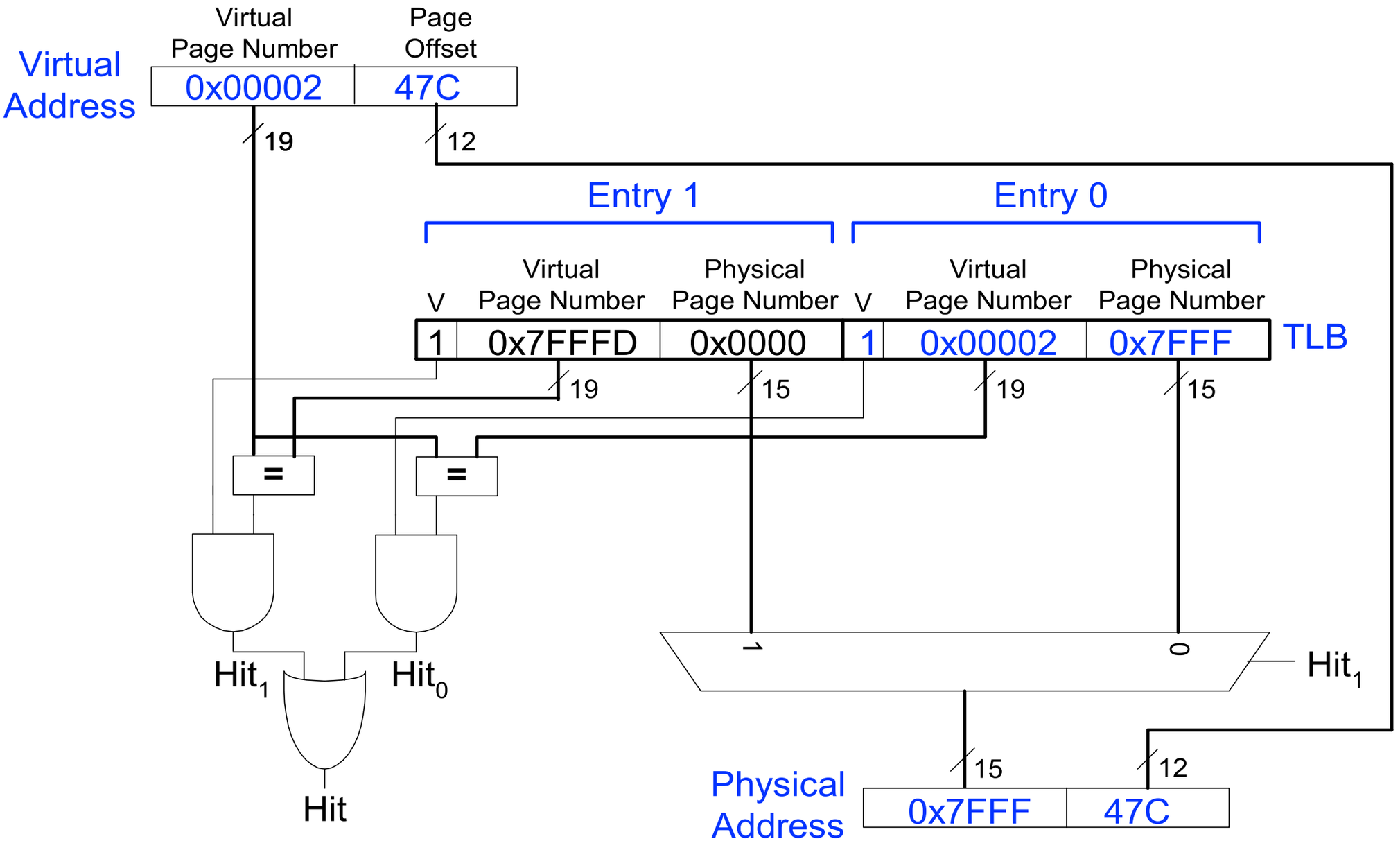
VPN is index into page table



Translation Lookaside Buffer (TLB)

- Page table accesses have a lot of temporal locality
  - Data accesses have temporal and spatial locality
  - Large page size, so consecutive loads/stores likely to access same page
- TLB
  - Small: accessed in < 1 cycle
  - Typically 16 - 512 entries
  - Fully associative
  - > 99 % hit rates typical
  - Reduces # of memory accesses for most loads and stores from 2 to 1

Example Two-Entry TLB

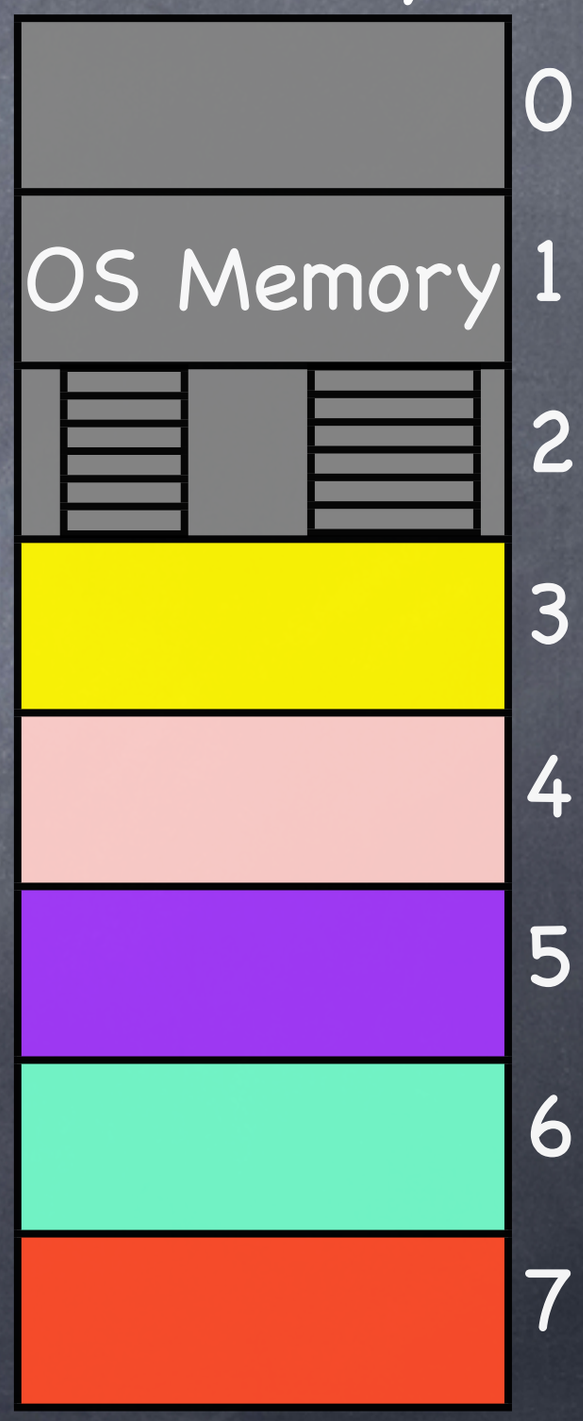


O.S. / HARDWARE INTERFACE

Program 1's Virtual Addr Space

Program 2's Virtual Addr Space

Real/Physical Memory



Page Table Address Register

Program 1's page table

6	0
–	1
3	2
–	3
–	4
–	5
4	6
–	7

Program 2's page table

–	0
–	1
–	2
7	3
–	4
5	5
–	6
–	7

Real/Physical Memory

Program 1's Virtual Addr Space

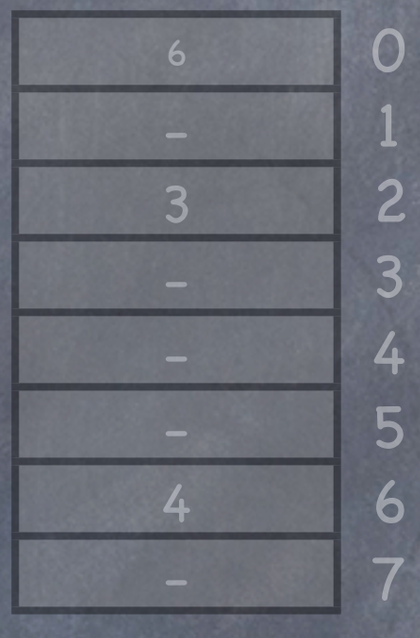
Program 2's Virtual Addr Space

Page Table Address Register

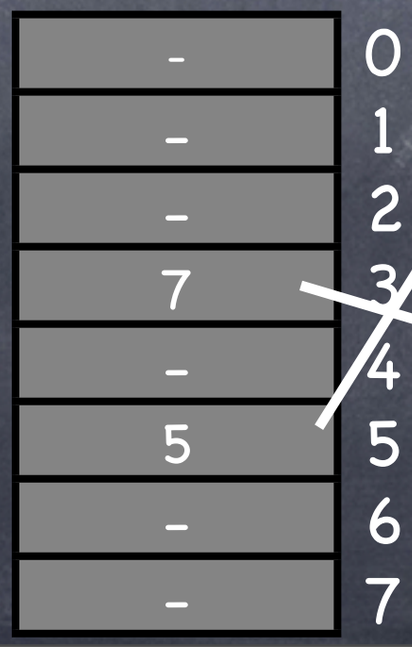
Program 1's Virtual Addr Space

Program 2's Virtual Addr Space

Program 1's page table



Program 2's page table



Real/Physical Memory