# Announcements

TA Application Time - Due by Monday

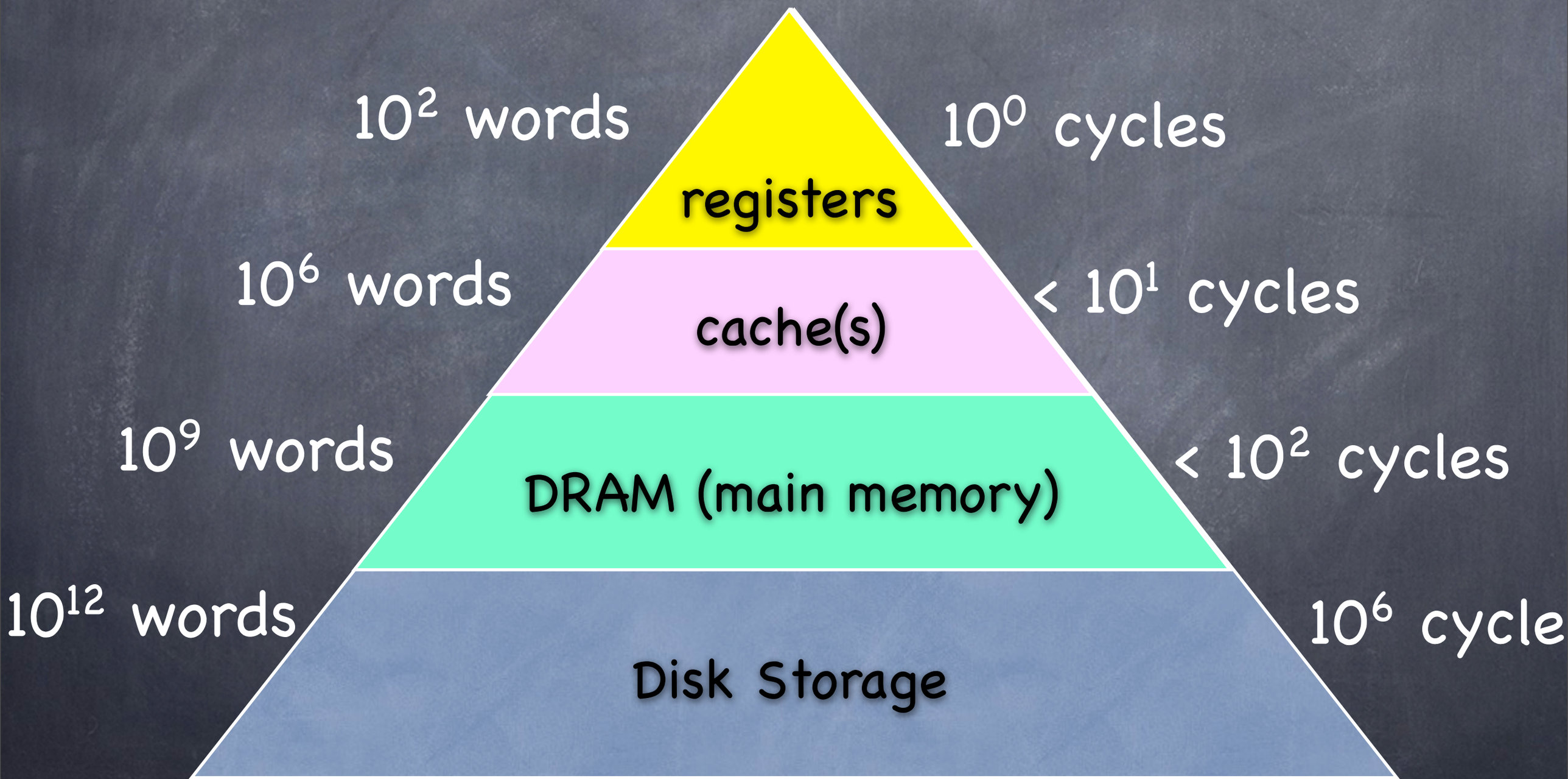
(Optional) ARM Reading linked off labs page

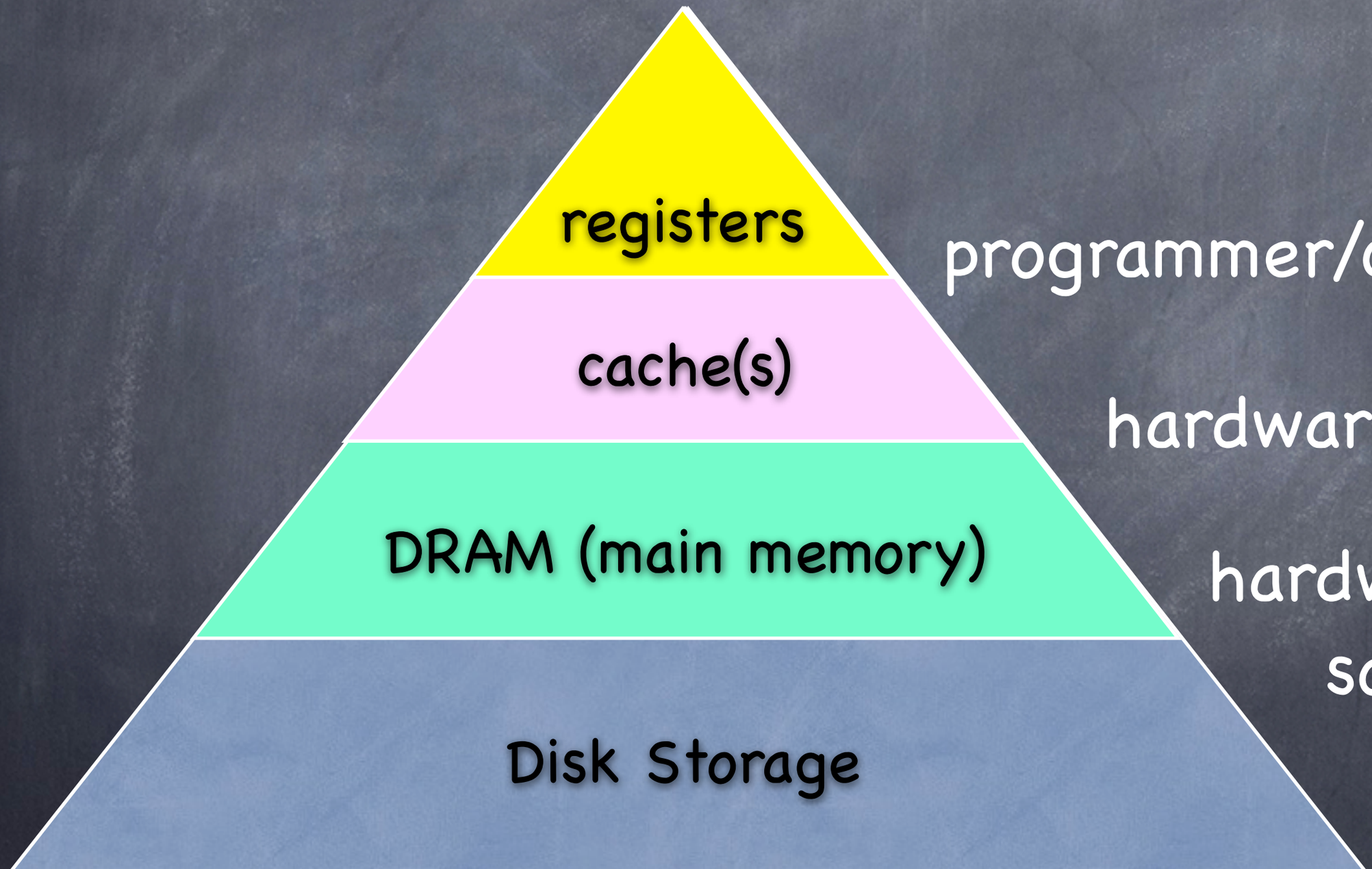
**Subject:** **Fwd: You've Got the Votes, You're Almost on Team REFUEL!**
**To:** Tom Murtagh <tom@cs.williams.edu>

DAD!!! I MADE IT PAST THE FIRST ROUND FOR CHOCOLATE MILK!!!! I need to submit some paperwork and then im a winner!!!

Thanks for your help!!!

# Virtual Memory?




registers
cache(s)
DRAM (main memory)
Disk Storage
programmer/compiler
hardware
hardware + O.S.
software

# Cache Miss Penalty

| | Cache | DRAM | Disk |
|---|---|---|---|
| | 5 | 25 | 1000000 |
| 0.5 | 3 | 13 | 500001 |
| 0.8 | 1.8 | 5.8 | 200001 |
| 0.9 | 1.4 | 3.4 | 100001 |
| 0.999 | 1.00 | 1.02 | 1001 |
| 0.99999 | 1 | 1 | 11 |
| 0.999999 | 1 | 1 | 2 |

Access time in cycles

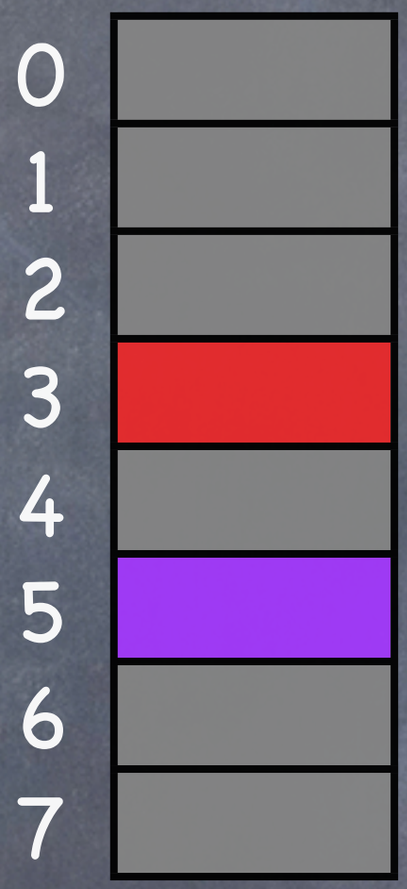
Hit Rate

Effective Memory Access Times

Effective = 1*hit-rate + access-time*(1 - hit-rate)

Program 1's Virtual Addr Space


Program 2's Virtual Addr Space




Real/Physical Memory

# Privileged Modes

- Most processors have a register indicating current mode:
  - user mode
  - supervisor mode
- Can only set page table address register in supervisor mode ==> memory protection
- Can only set mode register in supervisor mode!

# Traps / Exceptions

- Divide by zero
- Invalid operation code
- Segmentation fault
- Reference to invalid page table entry

# Exception Handling Approaches

- Branch to "fixed" address
  - Actually fixed
  - Address stored in fixed address (typically low or high addresses in memory).
  - Address stored in special register
- Save information including PC where error occurred (like bal saves return address).
- Enter supervisor mode!

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- Syscall