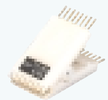
Call for pricing on quantities over 500 – we carry major manufacturers.

IC Test Clip Series

- For temporary connections to DIP package components
- Heavy-duty spring loaded hinge provides positive contact
- 20 AWG insulated gold contacts • Color: white


22103

Part No.	Product No.	Description	1	10	25
22103	JTC16	16-pin (for 8, 14 and 16-pin ICs)	$4.95	$4.49	$3.95
22120	JTC20	20-pin (for 18 and 20-pin ICs)	6.95	6.25	5.59
22162	JTC28	28-pin	8.95	7.95	6.49
22189	JTC40	40-pin	9.95	8.95	7.95

7400 Series

Dual-In-Line Package

Part No.	Product No.	Pins	Description	1	10	100
48979	7400	14	Quad 2-input NAND gate	$.59	$.49	$.45
49007	7401	14	Quad 2-input NAND gate (O.C.)	.49	.45	.39
49015	7402	14	Quad 2-input NOR gate	.59	.49	.45
49040	7404	14	Hex inverter	.59	.49	.45
49074	7405	14	Hex inverter (O.C.)	.29	.25	.22
49091	7406	14	Hex inverter buffer/driver (O.C.)	.45	.39	.35
49120	7407	14	Hex buffer/driver (O.C.)	.59	.49	.45
49146	7408	14	Quad 2-input AND gate	.59	.49	.45
49189	7410	14	Triple 3-input NAND gate	.25	.22	.15
49269	7411	14	Triple 3-input AND gate	3.95	3.59	3.25
49402	7413	14	Dual 4-input NAND gate Schmitt trigger	.29	.25	.19
49437	7414	14	Hex inverter Schmitt trigger	.45	.39	.35
49630	7416	14	Hex inverter buffer/driver (O.C.)	.25	.19	.10
49728	7417	14	Hex buffer/driver (O.C. hi-voltage)	.79	.69	.59
50008	7420	14	Dual 4-input NAND gate	.49	.45	.39
50024	7421	14	Dual 4-input AND gate	2.95	2.75	2.49
50083	7425	14	Dual 4-input NOR gate with strobe	1.09	.99	.89
50139	7427	14	Triple 3-input NOR gate	.49	.45	.39
50198	7428	14	Quad 2-input NOR buffer	.39	.35	.25
50227	7430	14	8-input NAND gate	.25	.22	.12
50235	7432	14	Quad 2-input OR gate	.59	.49	.45
50315	7438	14	Quad 2-input NAND buffer (O.C.)	.35	.29	.25
50358	7440	14	Dual 4-input NAND buffer	.13	.11	.09
50374	7442	16	BCD-to-decimal decoder	.89	.79	.69
50403	7445	16	BCD-to-decimal decoder/driver (30V)	.99	.89	.79
50411	7446	16	BCD-to-7 segment decoder/driver (30V)	1.29	1.19	1.09
50420	7447	16	BCD-to-7 segment decoder/driver (15V)	1.09	.99	.89
50518	7470	14	Edge-triggered JK flip-flop	.49	.45	.35
50526	7472	14	AND gated JK master/slave flip-flop	.49	.45	.35
50534	7473	14	Dual JK flip-flop with clear	.99	.89	.79
50551	7474	14	Dual D flip-flop	.45	.39	.29
50577	7475	16	4-bit bi-stable latch	2.95	2.75	2.49
50593	7476	16	Dual JK flip-flop with preset and clear	1.19	1.09	.99
50631	7483	16	4-bit binary full adder	.89	.79	.69
50657	7485	16	4-bit magnitude comp.	.39	.29	.22
50665	7486	14	Quad EXCLUSIVE-OR gate	.79	.69	.59
50681	7489	16	64-bit RAM P 50ns	2.95	2.75	2.49
50690	7490	14	Decade counter	.89	.79	.69
50737	7492	14	Divide-by-12 counter	1.19	1.09	.89
50745	7493	14	4-bit binary counter	1.29	1.19	1.09
50770	7495	14	4-bit parallel-access shift register (K155N)	.69	.59	.39
50788	7496	16	5-bit parallel-in, parallel-out shift register	.49	.39	.29
50796	7497	16	Synch. 6-bit binary rate multipliers	3.49	3.29	2.95
49234	74107	14	Dual JK flip-flop with clear	.39	.35	.25
49251	74109	16	Dual positive edge triggered JK flip-flop	.37	.34	.31
49293	74116	24	Dual 4-bit latches with clear	.99	.89	.79
49322	74121	14	Monostable multivibrator	.99	.89	.79
49349	74122	14	Retriggerable mono. multivibrator with clear	.69	.59	.45
49357	74123	16	Dual retriggerable mono. multivibrator	.89	.79	.69
49373	74125	14	Quad bus buffer tri-state (DM8093N)	.99	.89	.79
49381	74126	14	Quad bus buffer tri-state (DM8094N)	.79	.69	.59
49411	74132	14	Quad 2-input NAND Schmitt trigger	.69	.59	.35
49496	74148	16	8 to 3 line octal priority encoder	.89	.79	.69
49509	74150	24	16 to 1 line multiplexer	1.95	1.75	1.55
49525	74151	16	8-input multiplexer	.29	.25	.15
49550	74153	16	Dual 4/1 data selector/multiplexer	.25	.22	.15
49568	74154	24	4 to16 line decoder/demultiplexer	2.25	1.95	1.75
49605	74157	16	Quad 2/1 data selector	.39	.35	.29

7400 Series (Continued)

Dual-In-Line Package

Part No.	Product No.	Pins	Description	1	10	100
49648	74160	16	Decade counter with asynch. clear	$.35	$.29	$.19
49664	74161	16	Synchronous 4-bit counter	.39	.35	.25
49672	74163	16	Synchronous 4-bit counter	.29	.22	.12
49681	74164	14	8-bit serial shift register	.35	.29	.25
49699	74165	16	8-bit serial shift register, parallel load	.49	.45	.29
49779	74174	16	Hex D-type flip-flop with clear	.49	.45	.35
49795	74175	16	Quad D-type flip-flop with clear	.49	.45	.35
49824	74179	16	4-bit parallel-access shift register	.13	.11	.09
49832	74180	14	9-bit odd/even parity generator/checker	.25	.23	.21
49841	74181	24	Arithmetic logic unit/function generator	1.95	1.75	1.55
49883	74189	16	64-bit RAM tri-state (DM8599N)	3.59	3.25	2.95
49904	74191	16	Binary up/down counter	.99	.89	.79
49912	74192	16	Decade up/down counter with clear	3.95	3.59	3.25
49939	74193	16	Binary up/down counter with clear	1.39	1.19	1.09
49955	74194	16	4-bit bi-directional shift register	1.25	.99	.79
49963	74195	16	4-bit parallel-access shift register	.13	.11	.09
50041	74221	16	Dual mono. multiv. Schmitt trigger	.15	.13	.11
50104	74259	16	8-bit addressable latch (9334)	.15	.13	.12
50171	74279	16	Quad set-reset latch	.39	.35	.29
50286	74367	16	Hex buffer tri-state (DM8097N)	.13	.11	.09
88225	SDLD001A	—	Texas Instruments TTL Data Book	34.95	31.49	29.95

Part No.	Description	1	10
84953	360 pc. 7400 series IC cabinet kit	$129.95	$116.95

See page 62 for details

$160 Value

74C00 Series

Dual-In-Line Package

Part No.	Product No.	Pins	Description	1	10
44222	74C00	14	Quad 2-input NAND gate	$.49	$.39
63538	74C02	14	Quad 2-input NOR gate	.24	.22
44231	74C04	14	Hex inverter (CD4069)	.39	.35
44257	74C14	14	Hex inverter Schmitt trigger (CD40106)	.39	.35
44441	74C74	14	Dual D flip-flop	1.29	1.19
44329	74C174	16	Hex flip-flop (CD40174/MC14174BPC)	.19	.15
44345	74C193	16	Binary up/down counter w/ clear (40193)	1.49	1.29
44361	74C221	16	Dual monostable multivibrator	3.95	3.59
13469	74C367	16	Hex buffer tri-state (80C97/CD4503)	.49	.45
44396	74C373	20	Octal D-type flip-flop with clear tri-state	3.95	3.59
44409	74C374	20	Octal D flip-flop tri-state (INS82C06N)	1.49	1.25
44564	74C922	18	16-key keyboard encoder (INS8245N)	6.95	6.25
44572	74C923	20	20-key keyboard encoder (INS8246N)	6.95	6.25
44581	74C925	16	4-digit CTR with MUX D segment driver	6.95	5.95
44599	74C926	18	4-digit CTR with MUX D segment driver	7.95	6.95

74LS00 Series

Dual-In-Line Package

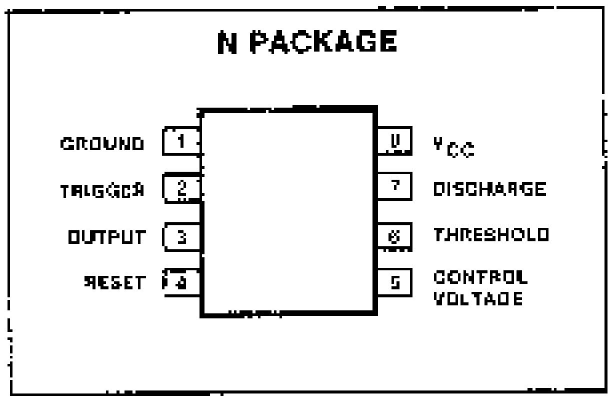
Part No.	Product No.	Pins	Description	1	10	100
46252	74LS00	14	Quad 2-input NAND gate	$.25	$.19	$.15
46287	74LS02	14	Quad 2-input NOR gate	.25	.19	.17
46308	74LS03	14	Quad 2-input NAND gate (O.C.)	.25	.19	.17
46316	74LS04	14	Hex inverter	.29	.25	.19
46341	74LS05	14	Hex inverter (O.C.)	.29	.25	.19
46359	74LS06	14	Hex inverter buffer/driver (O.C.)	.49	.45	.39
46367	74LS07	14	Hex buffer/driver (O.C. hi-voltage)	.89	.79	.69
46375	74LS08	14	Quad 2-input AND gate	.29	.25	.19
46391	74LS09	14	Quad 2-input AND gate (O.C.)	.25	.19	.15
46404	74LS10	14	Triple 3-input NAND gate	.29	.25	.19
46439	74LS11	14	Triple 3-input AND gate	.29	.25	.19
46640	74LS14	14	Hex inverter Schmitt trigger	.25	.19	.17
47095	74LS20	14	Dual 4-input NAND gate	.25	.19	.17
47108	74LS21	14	Dual 4-input AND gate	.25	.19	.17
47378	74LS27	14	Triple 3-input NOR gate	.25	.19	.17
47458	74LS30	14	8-input NAND gate	.25	.19	.17
47466	74LS32	14	Quad 2-input OR gate	.25	.19	.17
47597	74LS37	14	Quad 2-input NAND buffer	.39	.35	.29
47693	74LS38	14	Quad 2-input NAND buffer (O.C.)	.29	.25	.15
47773	74LS42	16	BCD-to-decimal decoder	.69	.59	.49
47790	74LS47	16	BCD to 7-seg. decoder/driver (O.C.)	.89	.79	.69
47811	74LS48	16	BCD to 7-seg. decoder/driver	4.95	4.49	3.95

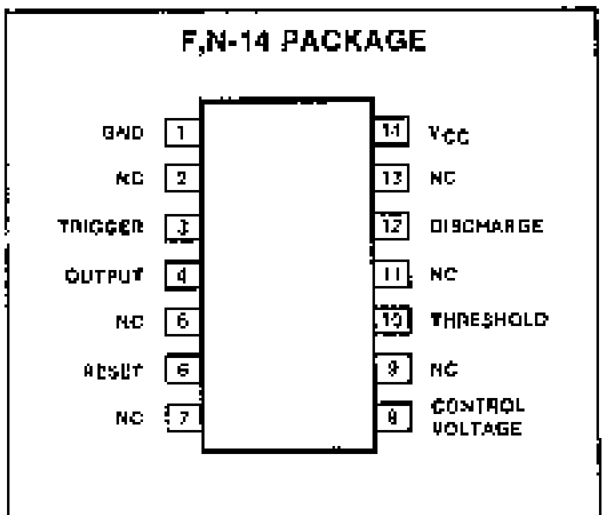
SA555F,N,N-14 • SE555F,T,N,N-14 • SE555C,F,T,N,N-14 • NE555F,T,N,N-14

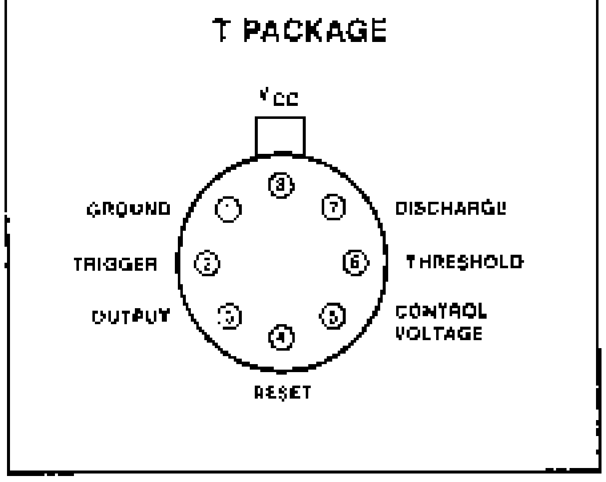
FEATURES

- Turn off time less than 2µs
- Maximum operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C
- SE555 Mil std 883A,B,C available M38510 (JAN) approved, M38510 processing available.

PIN CONFIGURATIONS







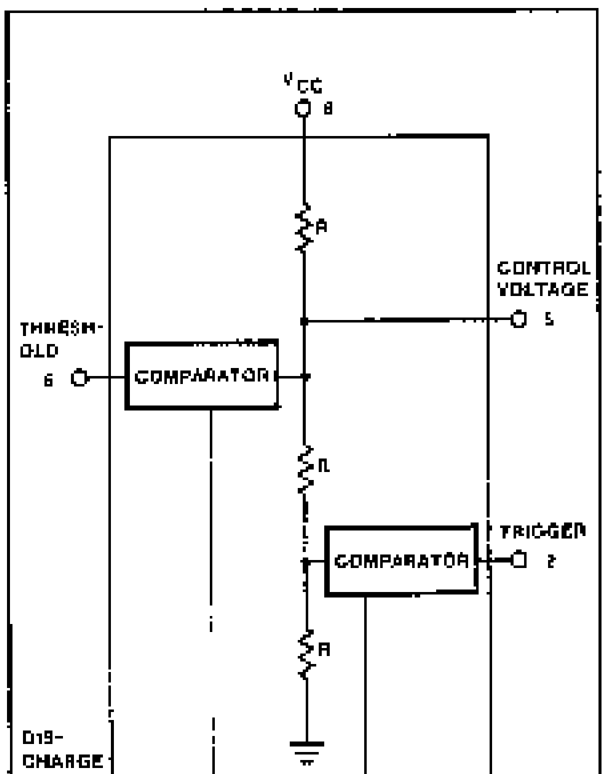
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

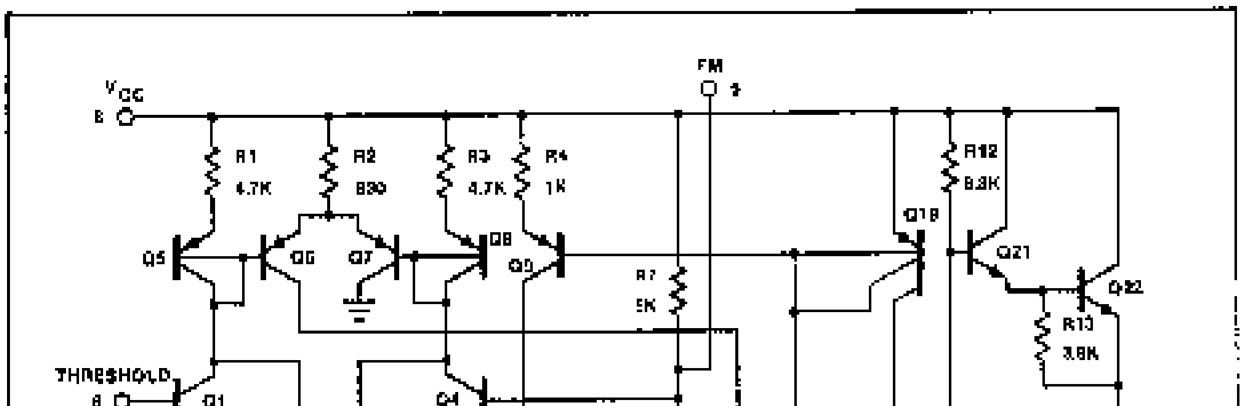
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE555	+18	V
NE555, SE555C, SA555	+16	V
Power dissipation	600	mW
Operating temperature range		
NE555	0 to +70	°C
SA555	-40 to +85	°C
SE555, SE555C	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60sec)	300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = +5V$ to $+15$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE555 Min	SE555 Typ	SE555 Max	NE555/SE555C/SA555 Min	NE555/SE555C/SA555 Typ	NE555/SE555C/SA555 Max	UNIT
Supply voltage		4.5		18	4.5		16	V
Supply current (low state)[1]	$V_{CC} = 5V$ $R_L = \infty$		3	5		3	6	mA
	$V_{CC} = 15V$ $R_L = \infty$		10	12		10	15	mA
Timing error (monostable)	$R_A = 2K\Omega$ to $100K\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		0.5	2.0		1.0	3.0	%
Drift with temperature			30	100		50		ppm/°C
Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
Timing error (astable)	$R_A, R_B = 1k\Omega$ to $100k\Omega$							
Initial accuracy[2]	$C = 0.1\mu F$		1.5			2.25		%
Drift with temperature	$V_{CC} = 15V$		90			150		ppm/°C
Drift with supply voltage			0.15			0.3		%/V
Control voltage level	$V_{CC} = 15V$	9.6	10.0	10.4	9.0	10.0	11.0	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4.0	V
Threshold voltage	$V_{CC} = 15V$	9.4	10.0	10.6	8.8	10.0	11.2	V
	$V_{CC} = 5V$	2.7	3.33	4.0	2.4	3.33	4.2	V
Threshold current[3]			0.1	0.25		0.1	0.25	μA
Trigger voltage	$V_{CC} = 15V$	4.8	5.0	5.2	4.5	5.0	5.6	V
	$V_{CC} = 5V$	1.45	1.67	1.9	1.1	1.67	2.2	V
Trigger current	$V_{TRIG} = 0V$		0.5	0.9		0.5	2.0	μA
Reset voltage[4]		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset current			0.1	0.4		0.1	0.4	mA
Reset current	$V_{RESET} = 0V$		0.4	1.0		0.4	1.5	mA
Output voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	0.25	V
	$I_{SINK} = 50mA$		0.4	0.5		0.4	0.75	V
	$I_{SINK} = 100mA$		2.0	2.2		2.0	2.5	V
	$I_{SINK} = 200mA$		2.5			2.5		V
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25		0.3	0.4	V
	$I_{SINK} = 5mA$		0.05	0.2		0.25	0.35	V
Output voltage (high)	$V_{CC} = 15V$							
	$I_{SOURCE} = 200mA$		12.5			12.5		V
	$I_{SOURCE} = 100mA$	13.0	13.3		12.75	13.3		V
	$V_{CC} = 5V$							
	$I_{SOURCE} = 100mA$	3.0	3.3		2.75	3.3		V
Turn off time[5]	$V_{RESET} = V_{CC}$		0.5	2.0		0.5		μs
Rise time of output			100	200		100	300	ns
Fall time of output			100	200		100	300	ns
Discharge leakage current			20	100		20	100	na

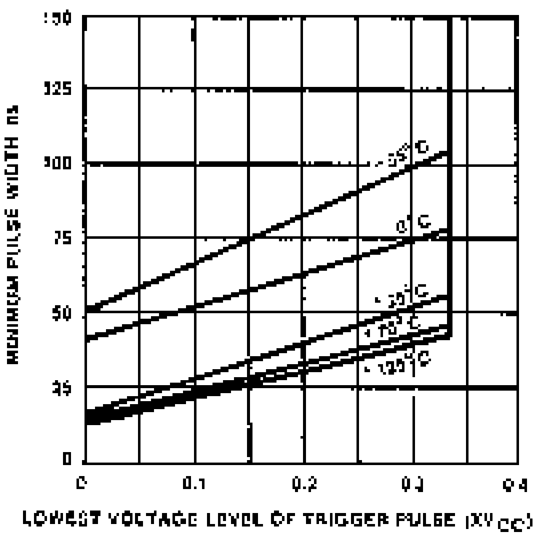
NOTES

1. Supply current when output high typically 1mA less
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation the max total $R = 10$ megohm and for 5V operation the max total $R = 3.4$ megohm.
4. Specified with trigger input high
5. Time measured from a positive going input pulse from 0 to $0.8xV_{CC}$ into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

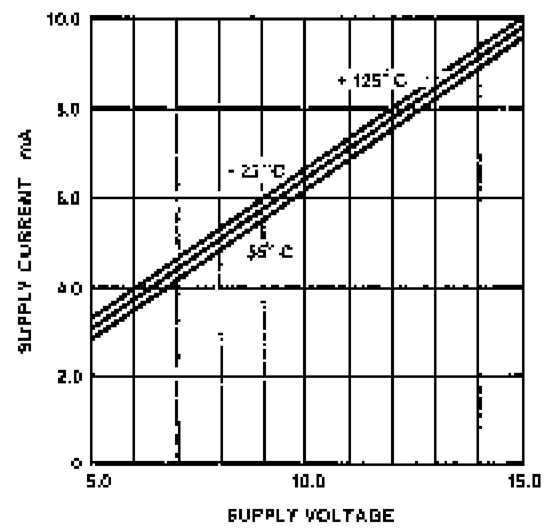
SA555F,N,N-14 • SE555F,T,N,N-14 • SE555C,F,T,N,N-14 • NE555F,T,N,N-14

TYPICAL PERFORMANCE CHARACTERISTICS

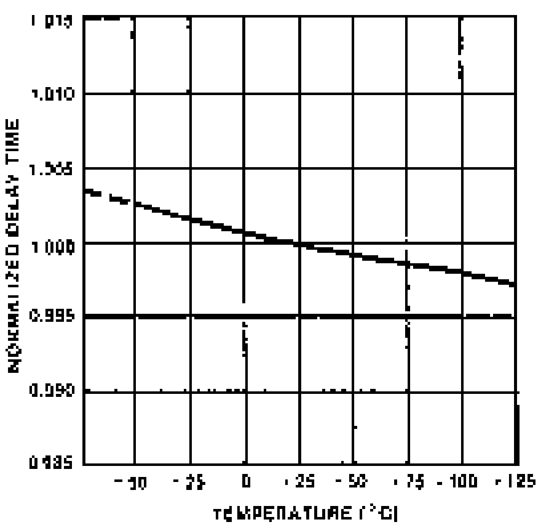
MINIMUM PULSE WIDTH
REQUIRED FOR TRIGGERING



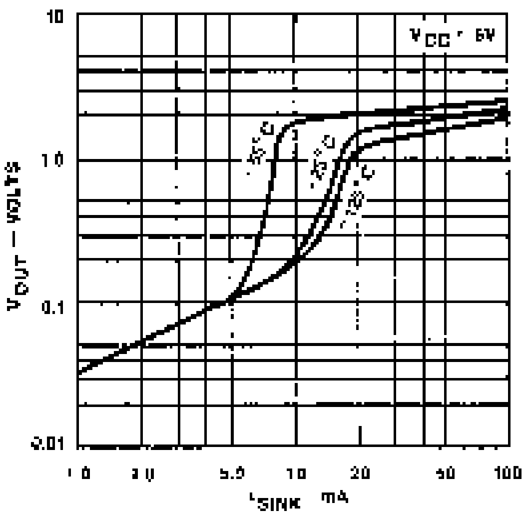
SUPPLY CURRENT
vs SUPPLY VOLTAGE



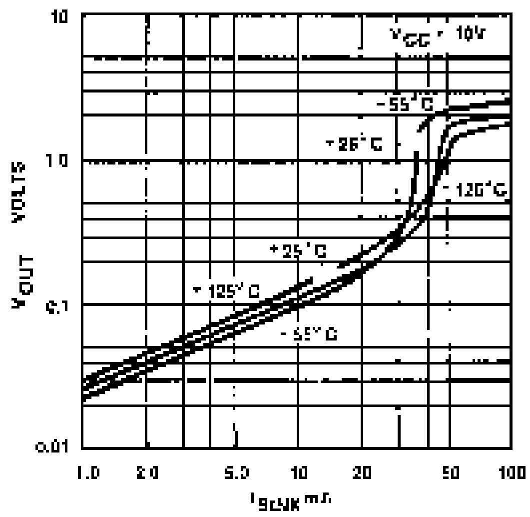
DELAY TIME
vs TEMPERATURE



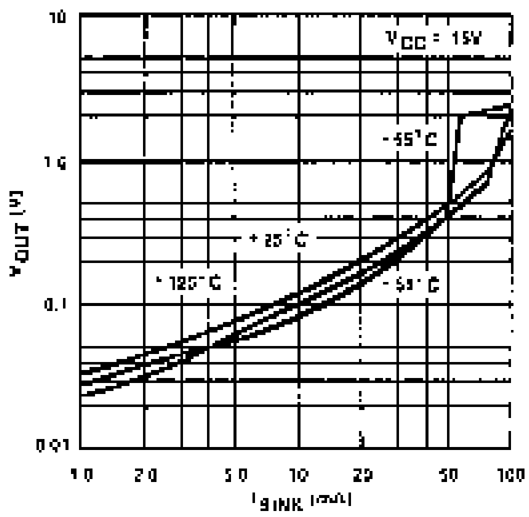
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



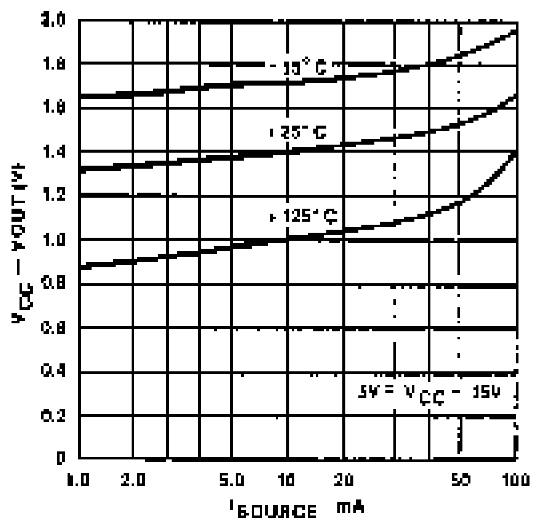
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



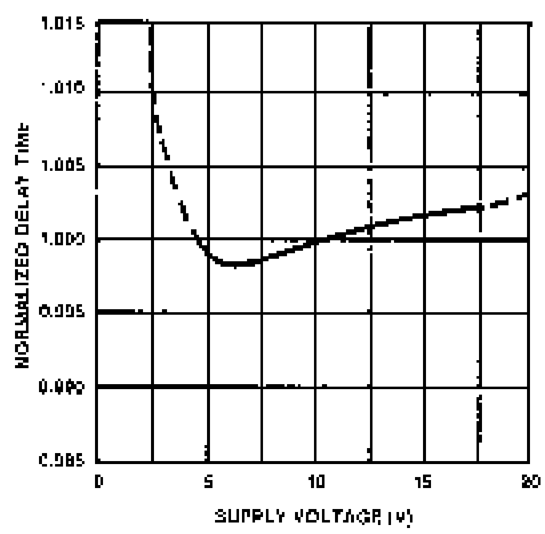
LOW OUTPUT VOLTAGE
vs OUTPUT SINK CURRENT



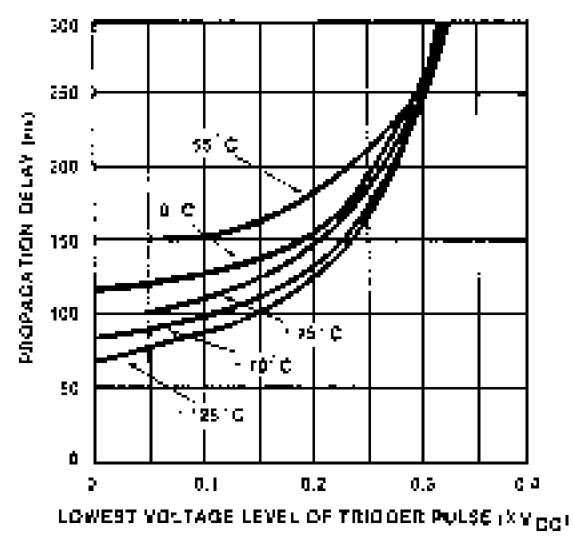
HIGH OUTPUT VOLTAGE DROP
vs OUTPUT SOURCE CURRENT



DELAY TIME vs
SUPPLY VOLTAGE



PROPAGATION DELAY
vs VOLTAGE LEVEL
OF TRIGGER PULSE



ORIGINAL
→38957 & 38981

National Semiconductor

NMOS RAMs

MM2114, MM2114L Family 4096-Bit (1024 × 4) Static RAMs

General Description

The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

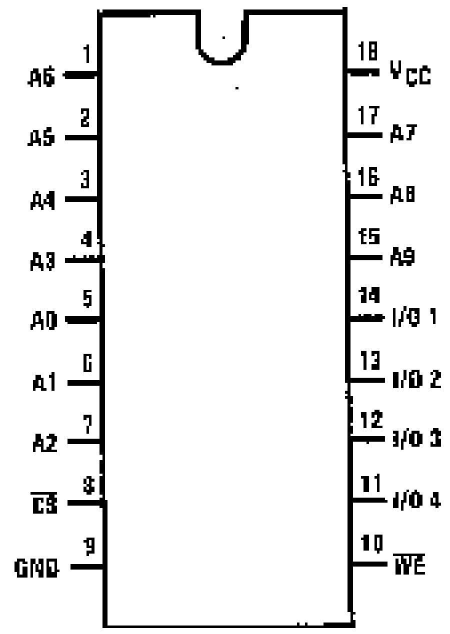
The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 200 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package

Connection Diagram

Dual-In-Line Package

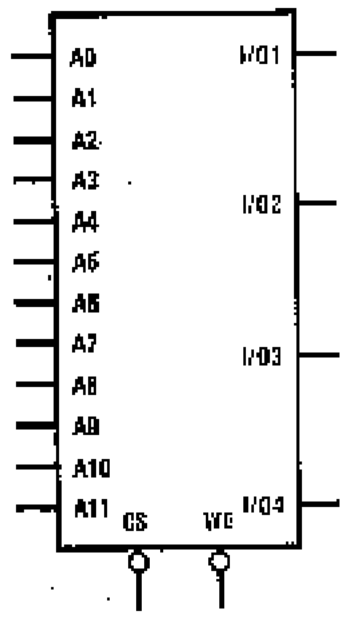


TOP VIEW

Order Number MM2114J-25L, MM2114J-25, MM2114J-2L, MM2114J-2, MM2114J, MM2114J-L, MM2114J-3L or MM2114J-3
See NS Package J18A

Order Number MM2114N-2L, MM2114N-2, MM2114N, MM2114N-L, MM2114N-3L or MM2114N-3
See NS Package N18A

Logic Symbol



Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	MODE
H	X	HI-Z	Not Selected
L	L	H	Write 1
L	L	L	Write 0
L	H	DOUT	Read

Functional Description

Two pins control the operation of the MM2114. Chip Select ($\overline{CS}$) enables write and read operations and controls TRI-STATING of the data-output buffer. Write Enable ($\overline{WE}$) chooses between READ and WRITE modes and also controls output TRI-STATING. The truth table details the states produced by combinations of the $\overline{CS}$ and $\overline{WE}$ controls.

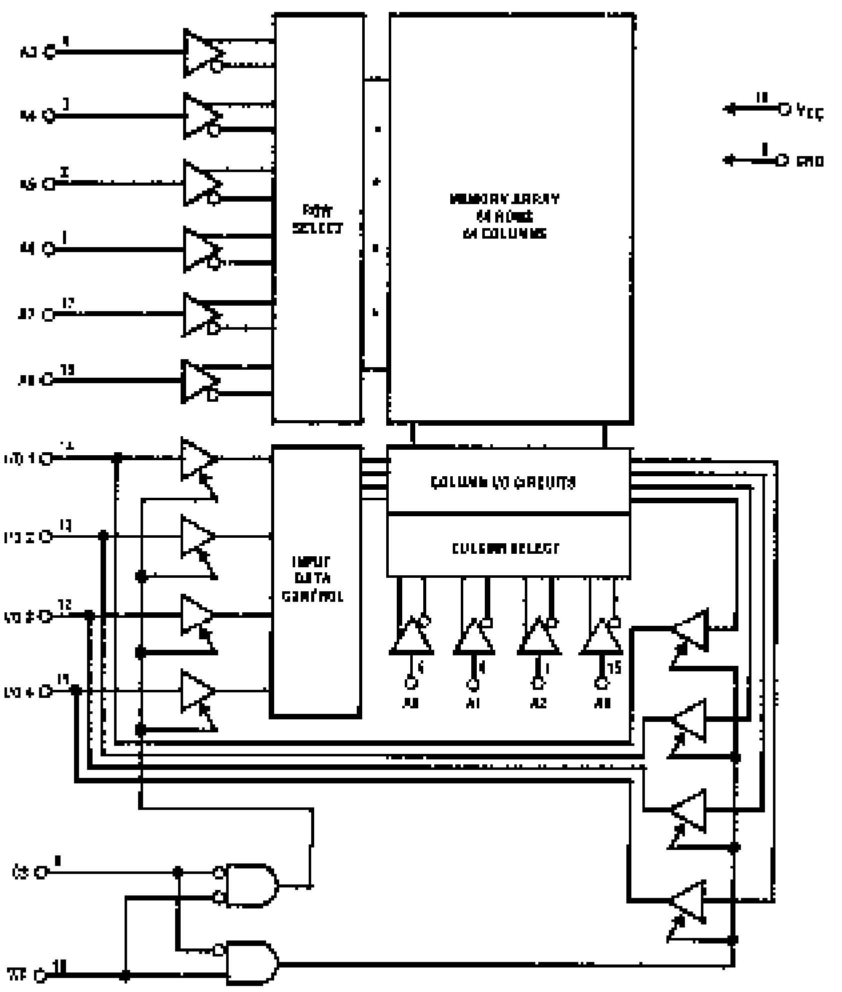
READ-cycle timing is shown in the section on Switching Time Waveforms. $\overline{WE}$ is kept high. Independent of $\overline{CS}$, any change in address code causes new data to be fetched and brought to the output buffer. $\overline{CS}$ must be low, however, for the output buffer to be enabled and transfer the data to the output pin.

Address access time, t_A, is the time required for an address change to produce new data at the output pin, assuming $\overline{CS}$ has enabled the output buffer prior to data arrival. Chip Select-to-output delay, t_{CO}, is the time required for $\overline{CS}$ to enable the output buffer and transfer previously fetched data to the output pin. Operation with $\overline{CS}$ continuously held low is permissible.

WRITE-cycle timing is shown in the section on Switching Time Waveforms. Writing occurs only during the time both $\overline{CS}$ and $\overline{WE}$ are low. Minimum write pulse width, t_{WP}, refers to this simultaneous low region. Data set-up and hold times are measured with respect to whichever control first rises. Successive write operations may be performed with $\overline{CS}$ continuously held low. $\overline{WE}$ then is used to terminate WRITE between address changes. Alternatively, $\overline{WE}$ may be held low for successive WRITES and $\overline{CS}$ used for WRITE interruption between address change.

In any event, either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous WRITE.

Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		−0.5	0.8	0.5	0.8	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -1.0$ mA	2.4		2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
I_{LI}	Input Load Current	$V_{IN} = 0$ to 5.25V	−10	10	10	10	μA
I_{LO}	Output Leakage Current	$V_O = 4V$ to 0.4V, $\overline{CS} = V_{IH}$	−10	10	10	10	μA
I_{CC1}	Power Supply Current	All Inputs = 5.25V, $T_A = 25°C$		95		65	mA
I_{CC2}	Power Supply Current	All Inputs = 5.25V, $T_A = 0°C$		100		70	mA

AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$, (Note 2)

SYMBOL	PARAMETER	MM2114-2 MM2114-2L		MM2114-25 MM2114-25L		MM2114-3 MM2114-3L		MM2114 MM2114-L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE										
t_{RC}	Read Cycle Time ($\overline{WE} = V_{IH}$)	200		250		300		450		ns
t_A	Access Time		200		250		300		450	ns
t_{CO}	Chip Select to Output Valid		70		90		100		120	ns
t_{CX}	Chip Select to Output Active	20		20		20		20		ns
t_{COT}	Chip Select to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	10		10		10		10		ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	200		250		300		450		ns
t_{WP}	Write Pulse Width	100		125		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DS}	Data Set-Up Time	100		125		150		200		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{WOT}	Write Enable to Output TRI-STATE	0	40	0	60	0	80	0	100	ns
t_{WO}	Write Enable to Output Valid		80		90		100		120	ns

Capacitance $T_A = 25°C$, f = 1 MHz, (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MM2114 MM2114-2 MM2114-25 MM2114-3		MM2114-L MM2114-2L MM2114-25L MM2114-3L		UNITS
			MIN	MAX	MIN	MAX	
C_{IN}	Input Capacitance	All Inputs $V_{IN} = 0V$		5		5	pF
C_{OUT}	Output Capacitance	$V_O = 0V$		10		10	pF

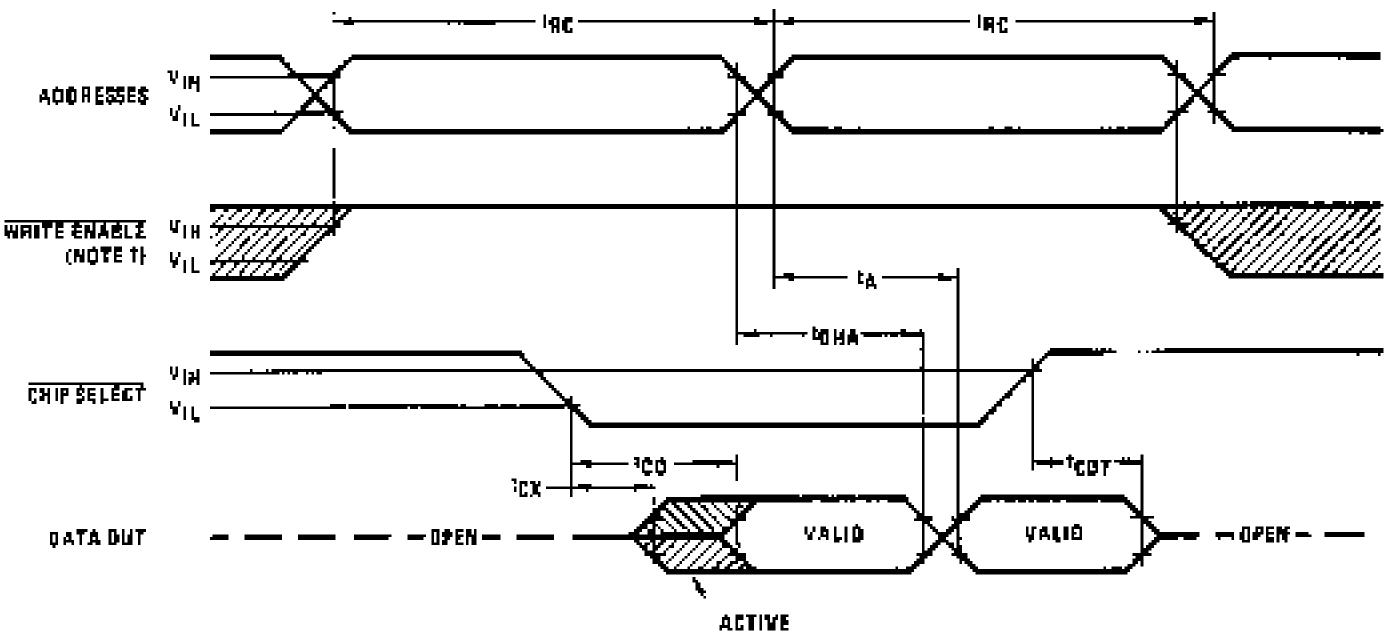
Note 1: Typical values at $T_A = 25°C$.

Note 2: All input transitions ≤ 10 ns. Timing referenced to $V_{IL(MAX)}$ or $V_{IH(MIN)}$ for inputs, 0.8V and 2V for output. For test purposes, input levels should swing between 0V and 3V. Output load = 1 TTL gate and C_L = 100 pF.

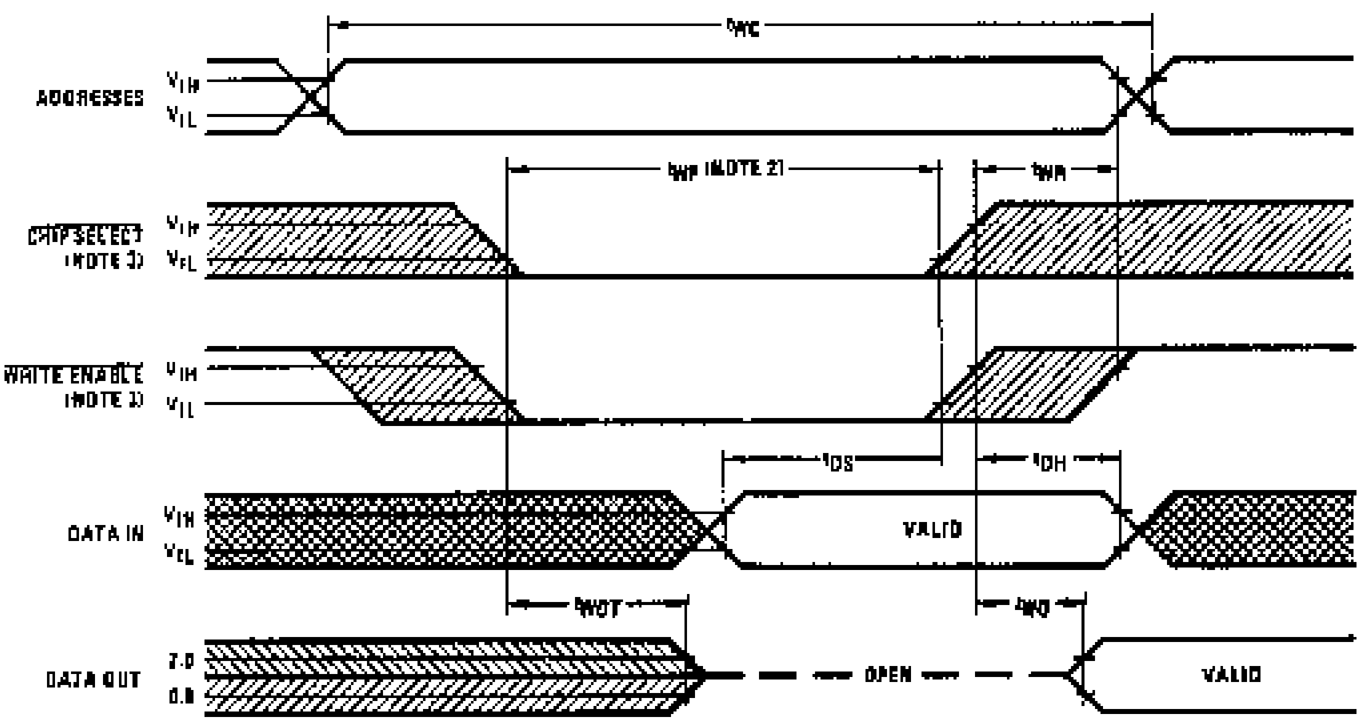
Note 3: This parameter is guaranteed by periodic testing.

Switching Time Waveforms

Read Cycle



Write Cycle



Note 1: $\overline{WE}$ is high during a read cycle ($\overline{WE} \geq V_{IH(MIN)}$).

Note 2: t_{WP} defines the period when both CS and $\overline{WE}$ are low. t_{AW} is referenced to the later of $\overline{CS}$ or $\overline{WE}$ going low while t_{DS}, t_{DH} and t_{WR} are referenced to the earlier of $\overline{CS}$ or $\overline{WE}$ going high. t_{WOT} and t_{WO} are referenced to $\overline{WE}$ with $\overline{CS}$ low.

Note 3: Either $\overline{WE}$ or $\overline{CS}$ (or both) must be high during address transitions to prevent erroneous write.

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March 1998

DM74LS00
Quad 2-Input NAND Gates

General Description

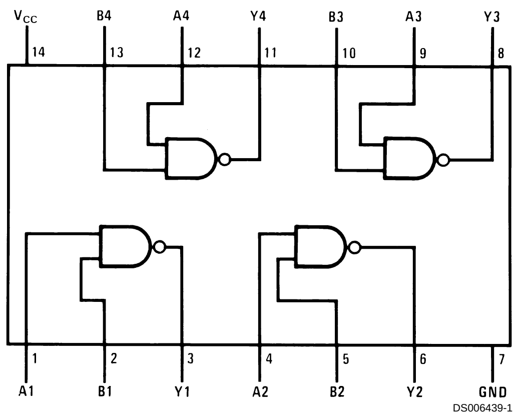
This device contains four independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS00) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS00DMQB, 54LS00FMQB, 54LS00LMQB, DM54LS00J, DM54LS00W, DM74LS00M or DM74LS00N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics

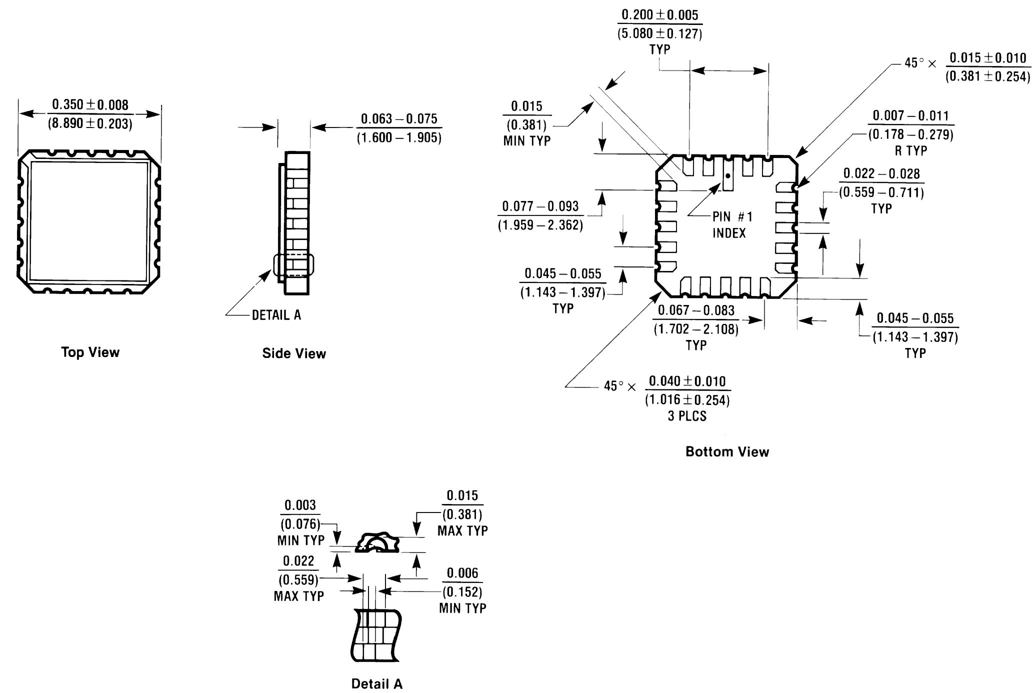
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

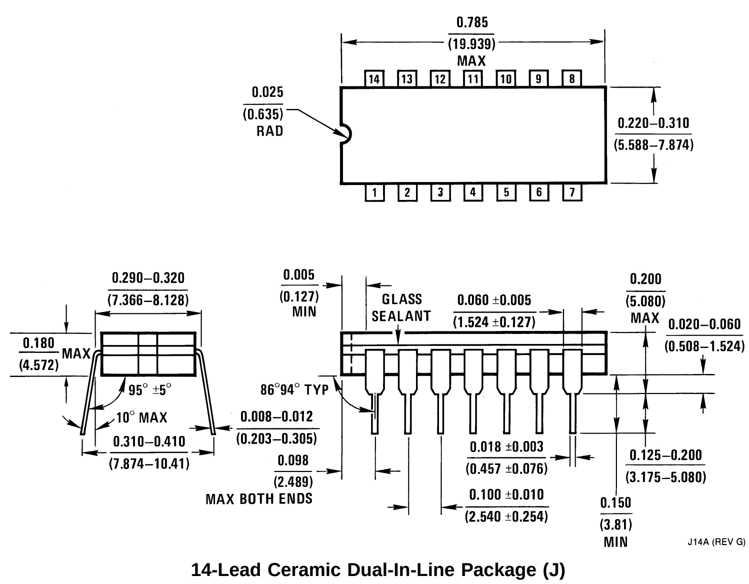
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

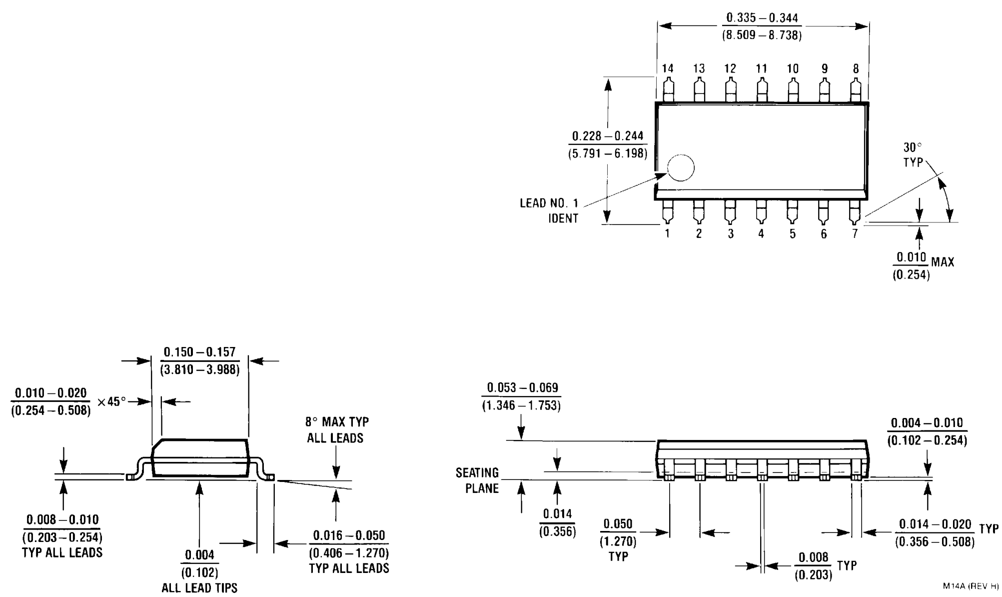


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS00LMQB
Package Number E20A

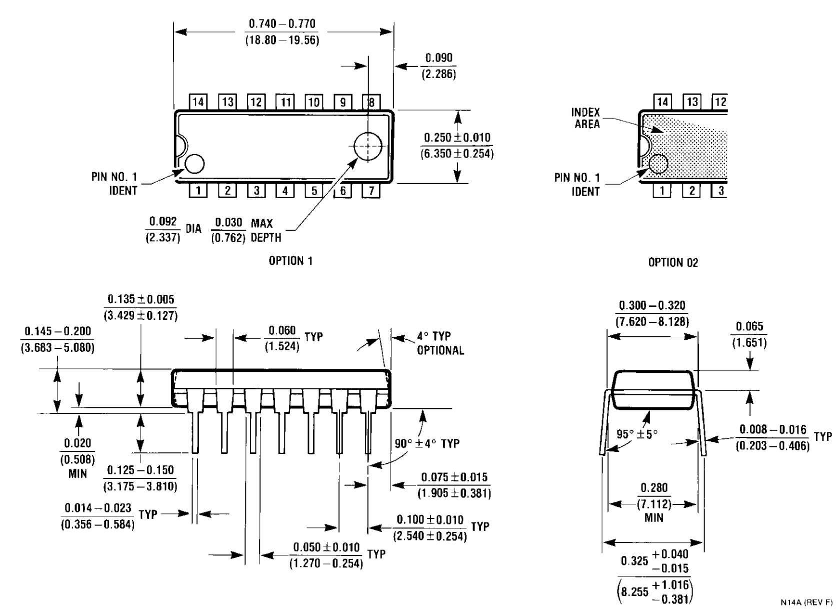


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS00DMQB or DM54LS00J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

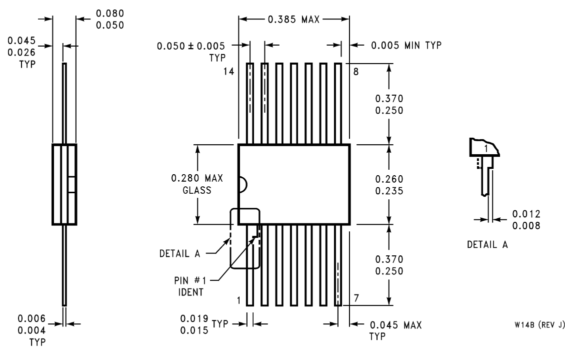


14-Lead Small Outline Molded Package (M)
Order Number DM74LS00M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS00N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS00FMQB or DM54LS00W
Package Number W14B

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March 1998

DM74LS02
Quad 2-Input NOR Gates

General Description

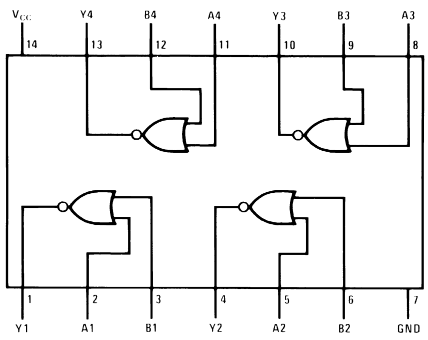
This device contains four independent gates each of which performs the logic NOR function.

Features

- Alternate Military/Aerospace device (54LS02) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



Order Number 54LS02DMQB, 54LS02FMQB, 54LS02LMQB, DM54LS02J, DM54LS02W, DM74LS02M or DM74LS02N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A + B}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS02			DM74LS02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.40	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.6	3.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.8	5.4	mA

Switching Characteristics

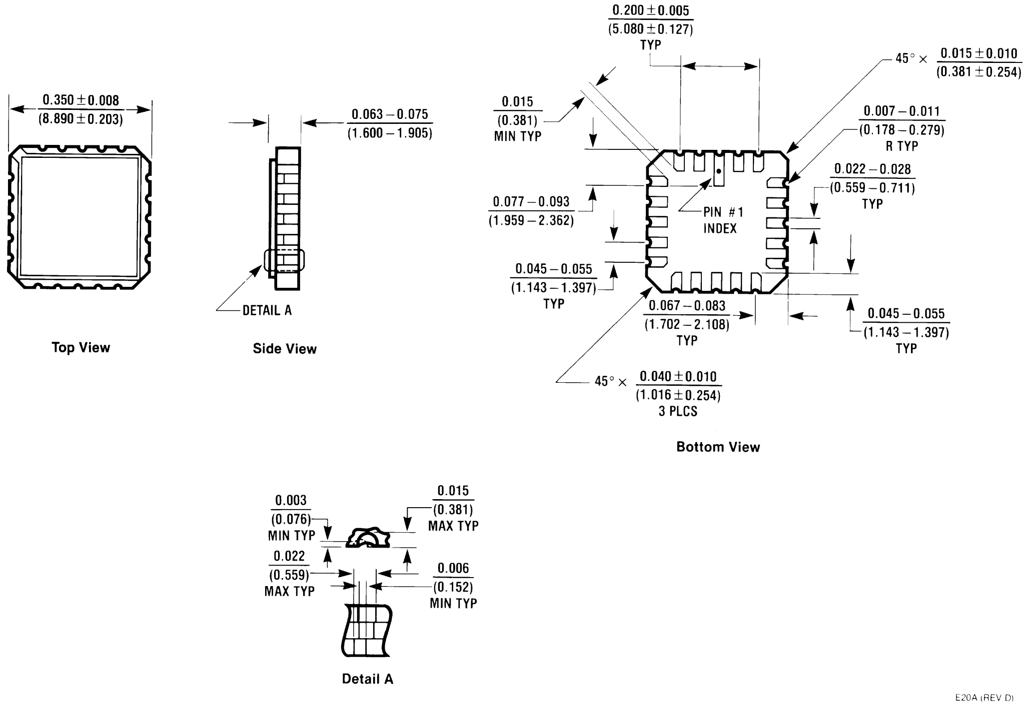
at V_{CC} = 5V and T_A = 25˚C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		13		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		10		15	ns

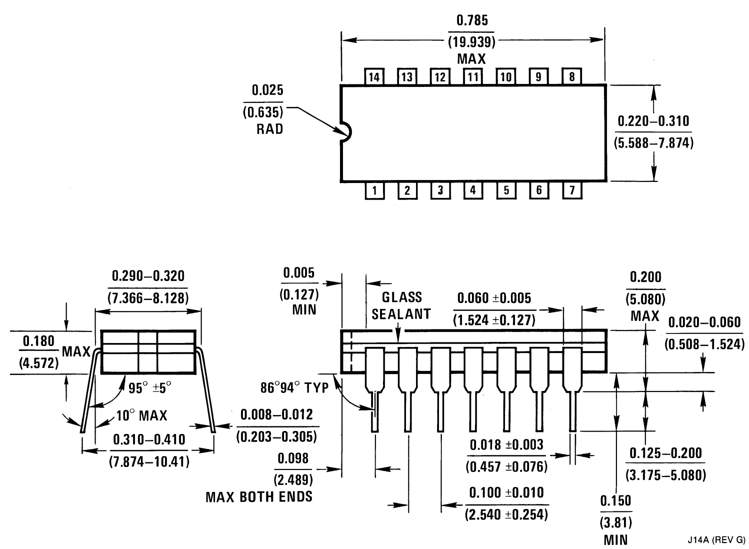
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

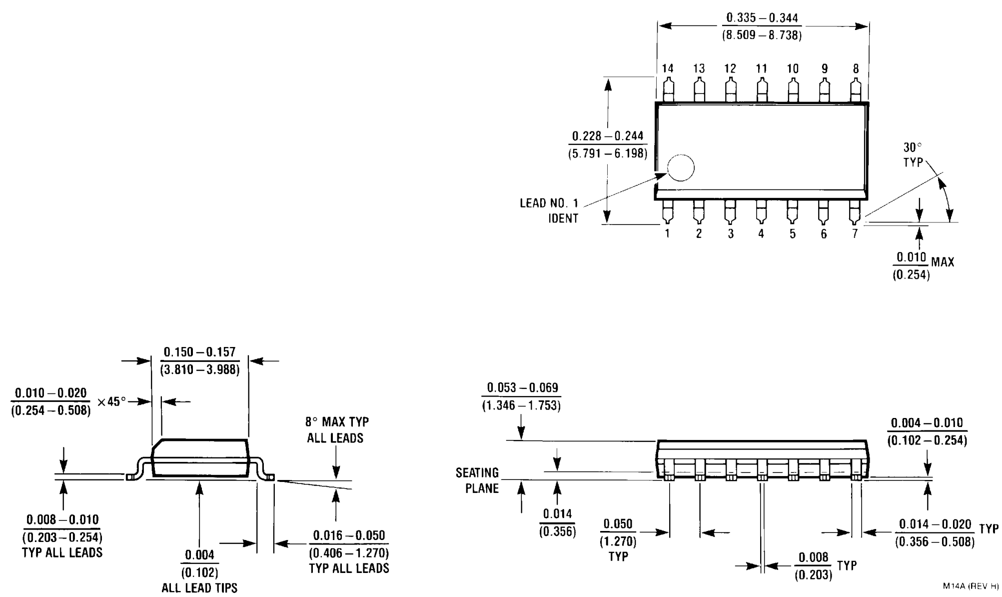


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS02LMQB
Package Number E20A

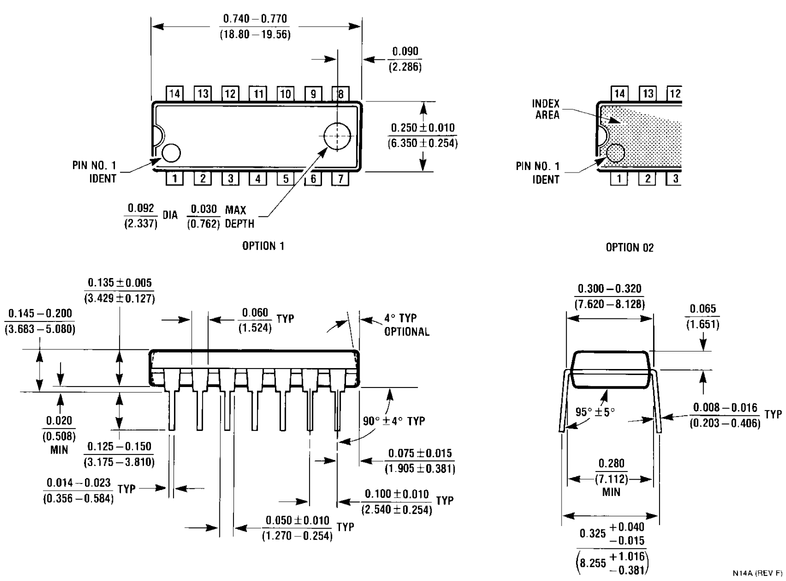


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS02DMQB or DM54LS02J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

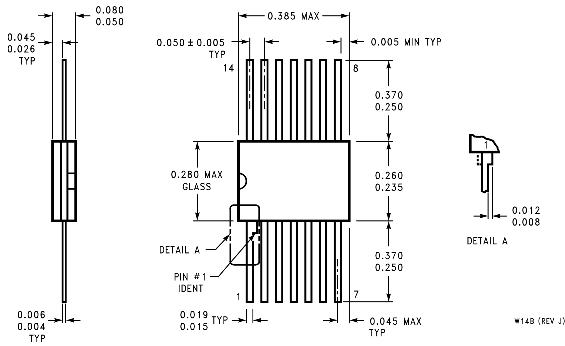


14-Lead Small Outline Molded Package (M)
Order Number DM74LS02M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS02N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS02FMQB or DM54LS02W
Package Number W14B

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March 1998

DM74LS03
Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS03) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

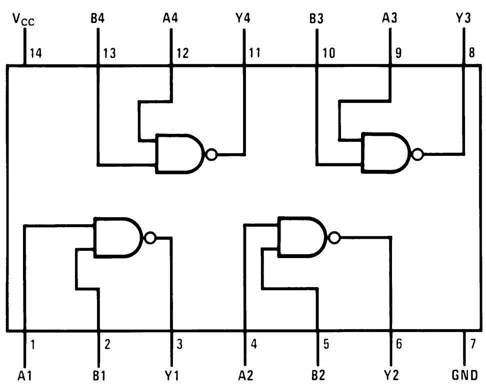
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



Order Number 54LS03DMQB, 54LS03FMQB, 54LS03LMQB, DM54LS03J, DM54LS03W, DM74LS03M or DM74LS03N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS03			DM74LS03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

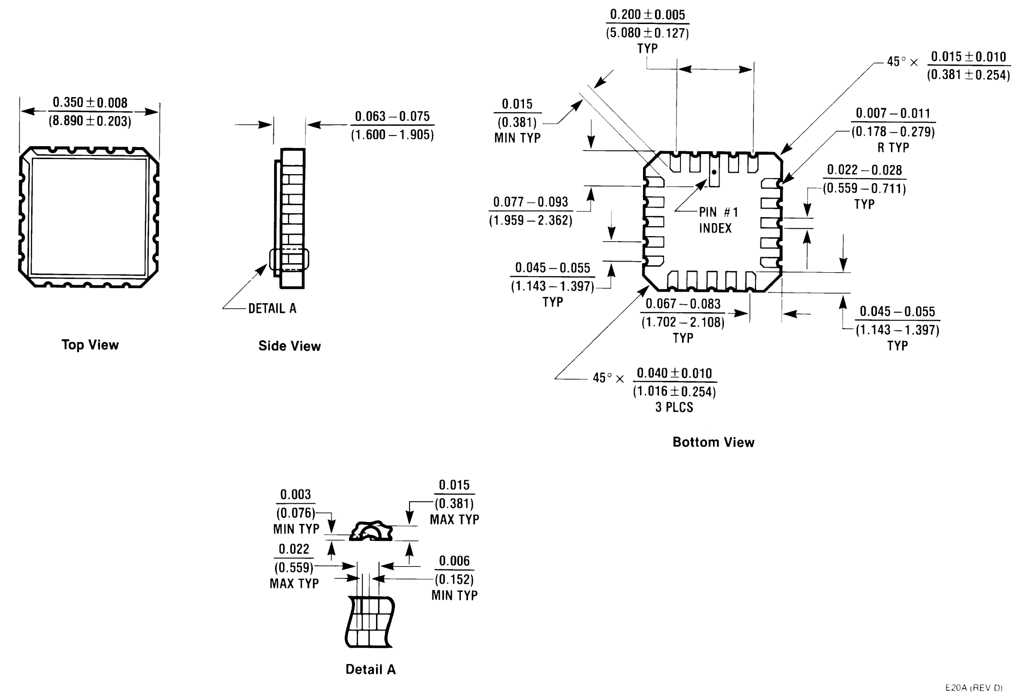
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

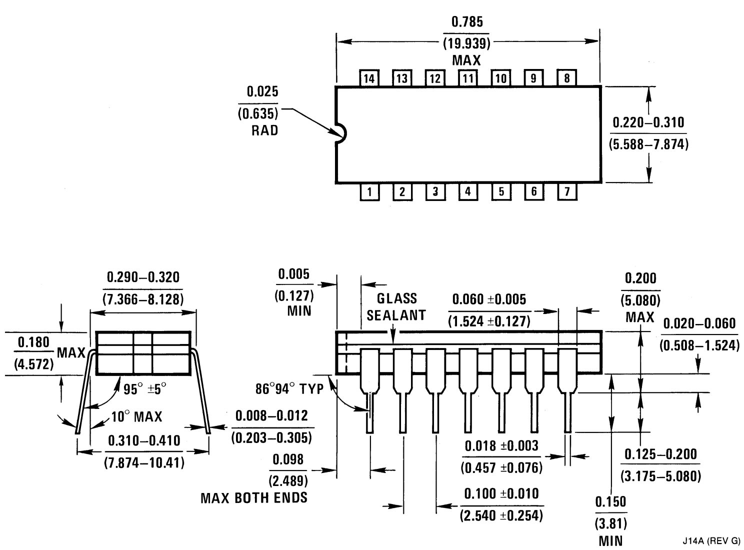
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Physical Dimensions inches (millimeters) unless otherwise noted

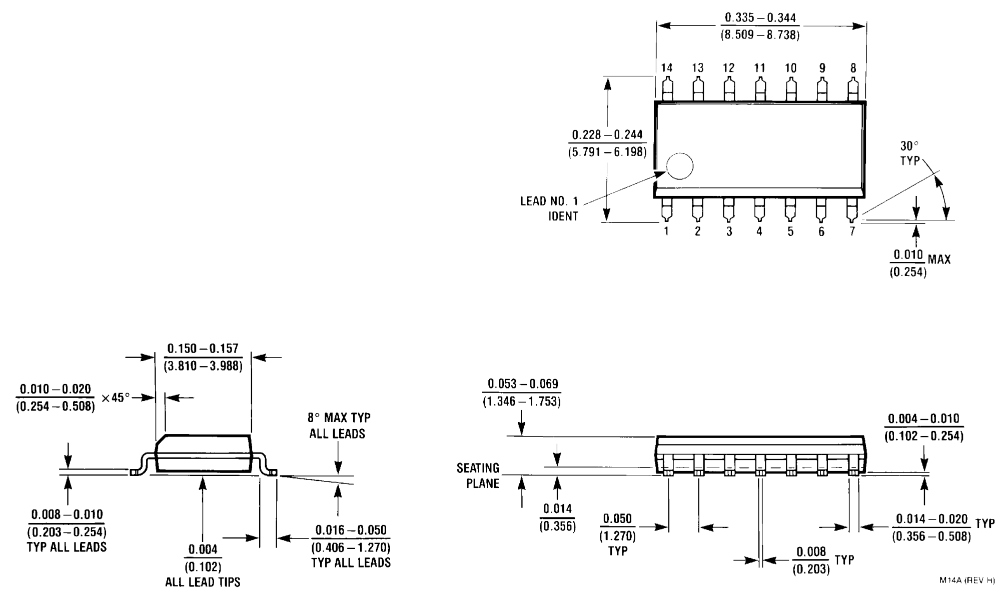


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS03LMQB
Package Number E20A

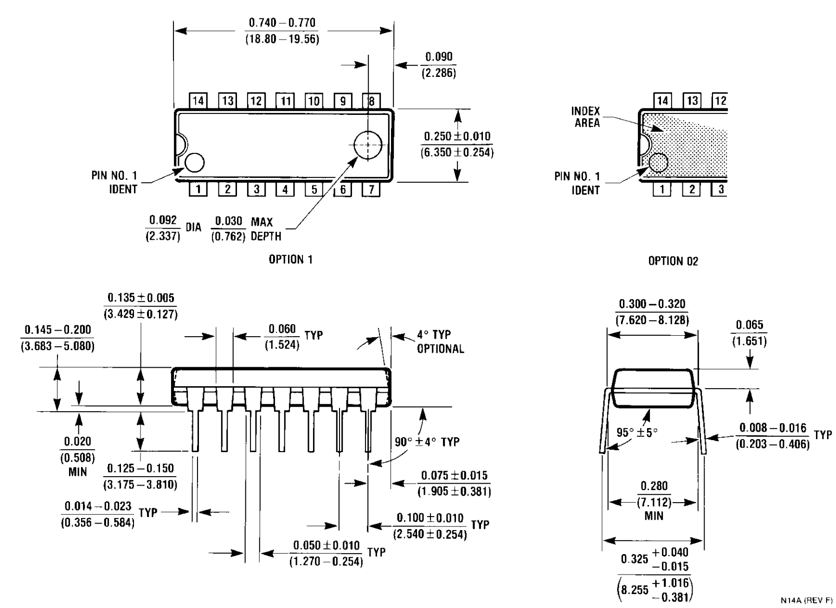


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS03DMQB or DM54LS03J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

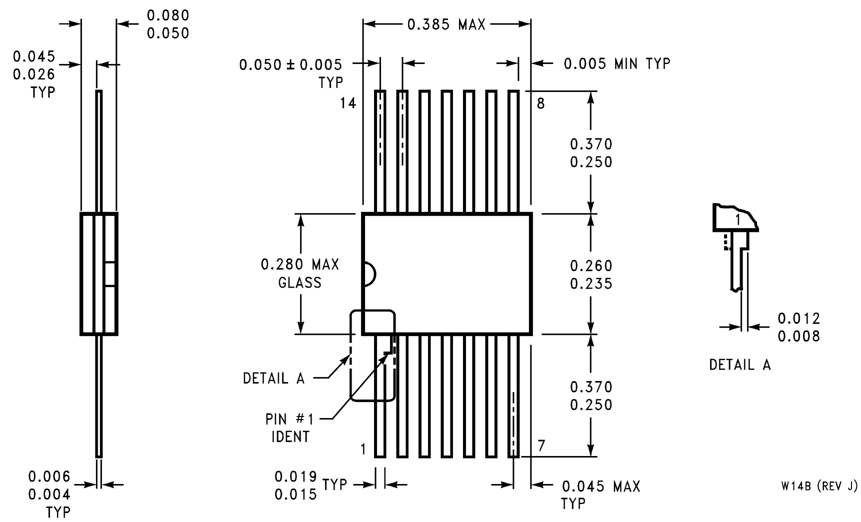


14-Lead Small Outline Molded Package (M)
Order Number DM74LS03M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS03N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS03FMQB or DM54LS03W
Package Number W14B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS04
Hex Inverting Gates

General Description

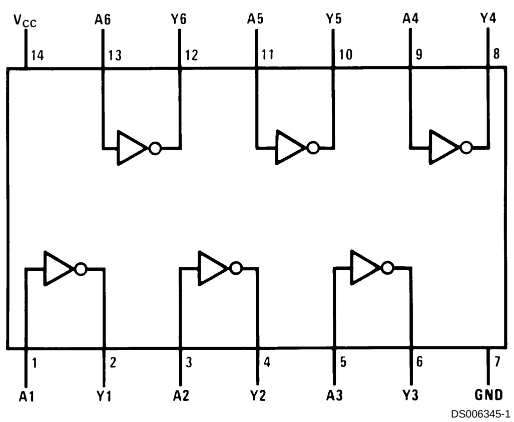
This device contains six independent gates each of which performs the logic INVERT function.

Features

- Alternate Military/Aerospace device (54LS04) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS04DMQB, 54LS04FMQB, 54LS04LMQB, DM54LS04J, DM54LS04W, DM74LS04M or DM74LS04N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A}$$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS04			DM74LS04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics

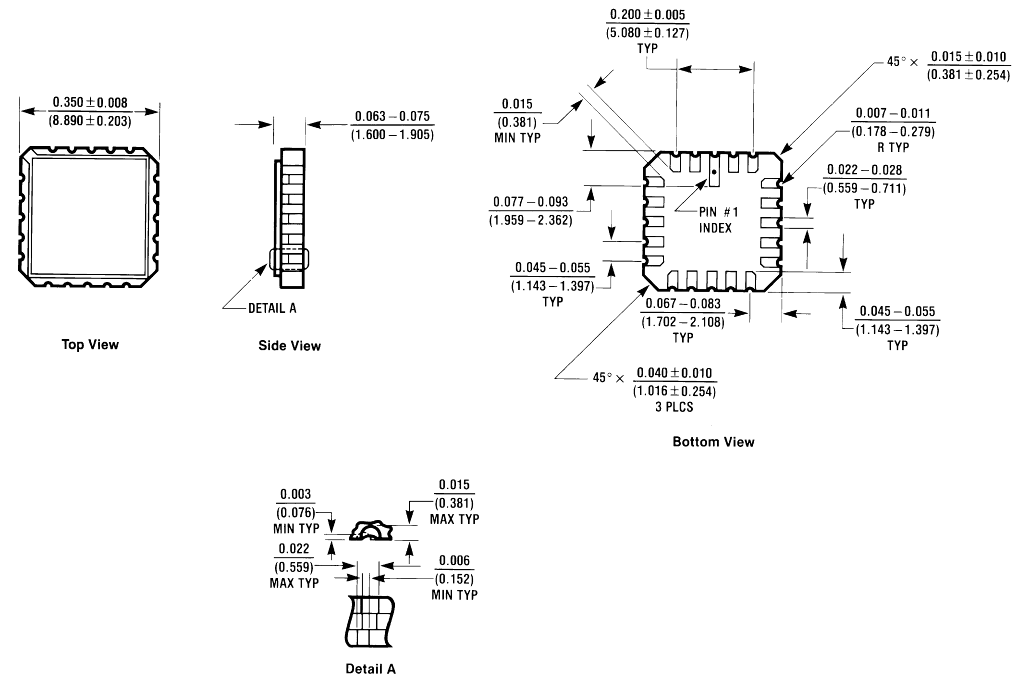
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

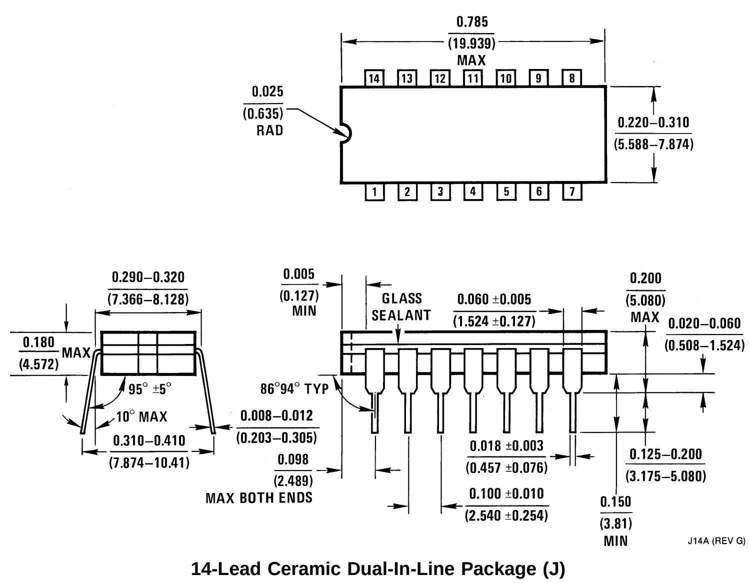
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

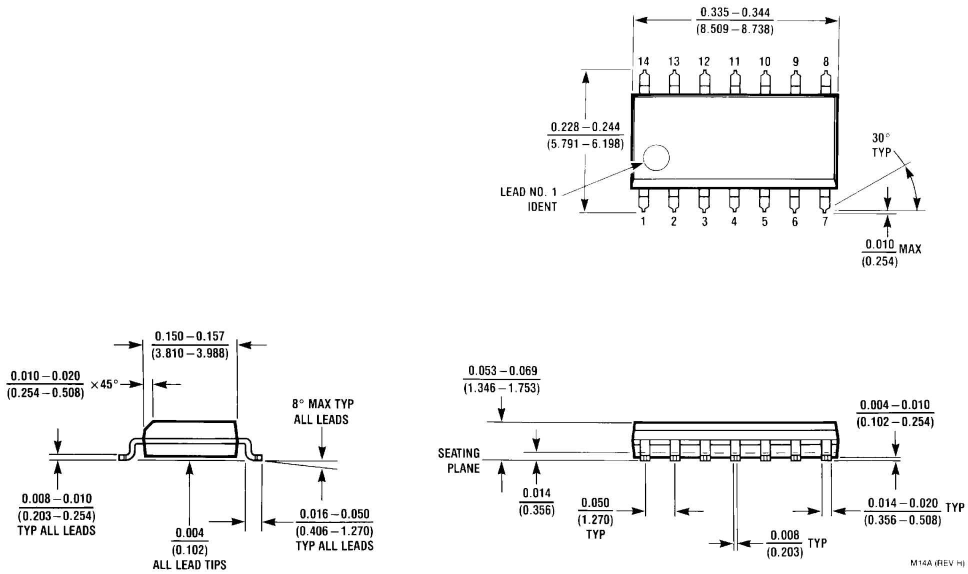


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS04LMQB
Package Number E20A

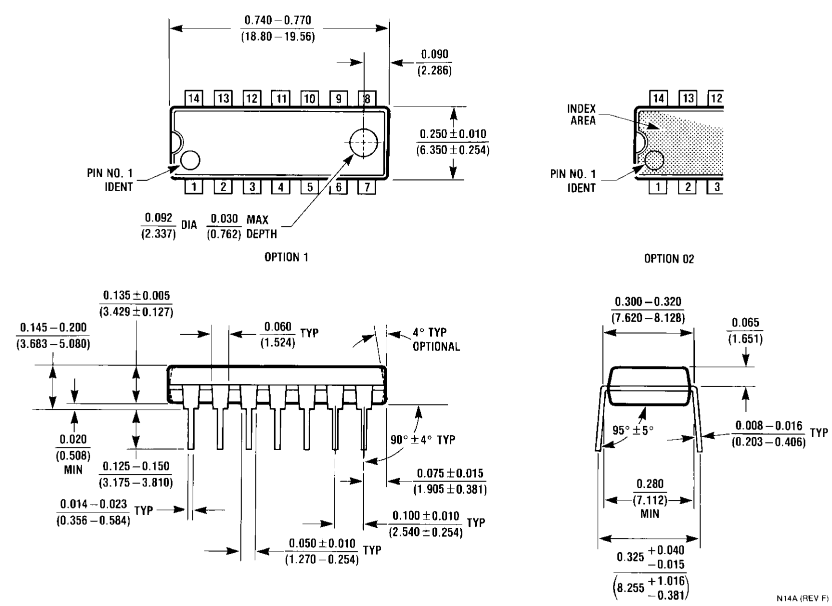


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS04DMQB or DM54LS04J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

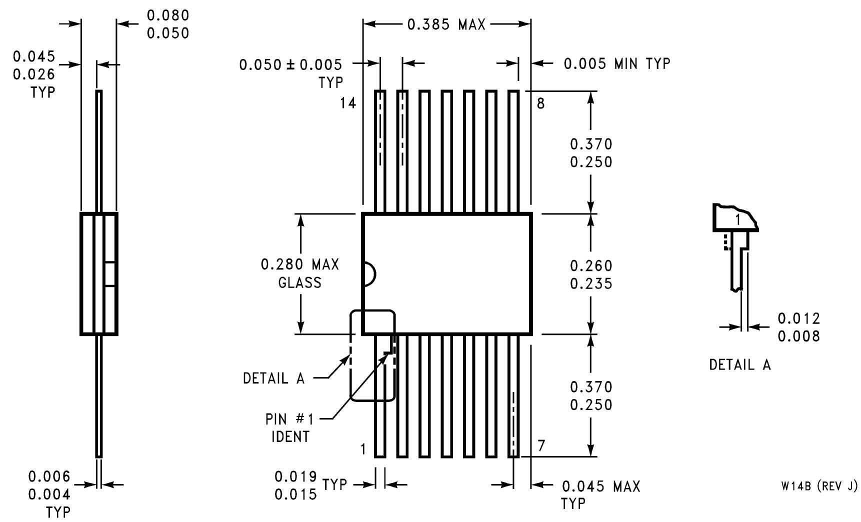


14-Lead Small Outline Molded Package (M)
Order Number DM74LS04M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS04N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS04FMQB or DM54LS04W
Package Number W14B

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March 1998

DM74LS05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS05) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

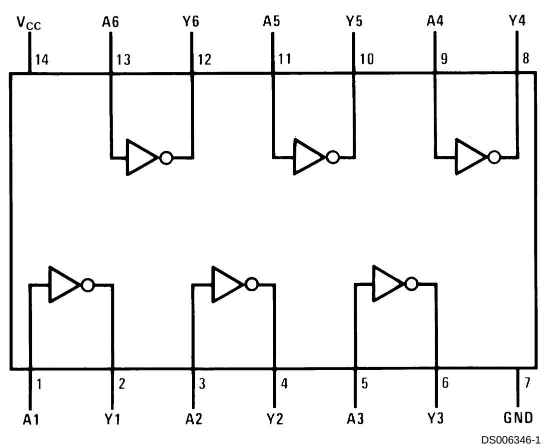
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



Order Number 54LS05DMQB, 54LS05FMQB, DM54LS05J, DM54LS05W, DM74LS05M or DM74LS05N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS05			DM74LS05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

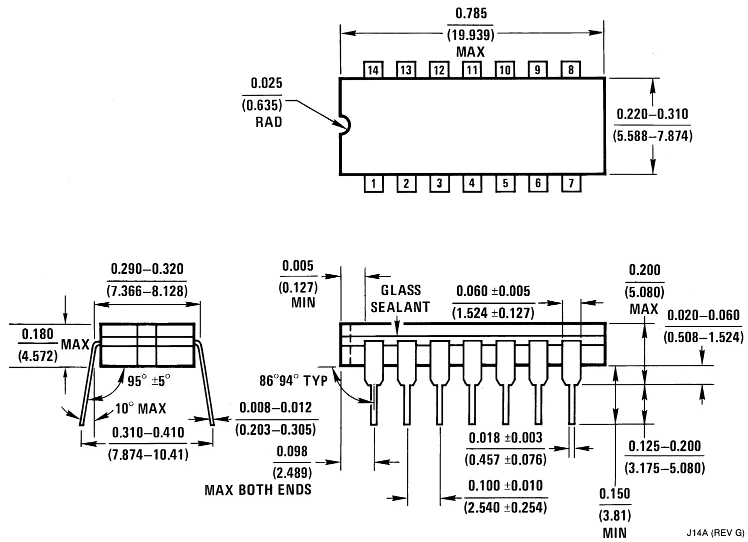
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C (See Section 1 for Test Waveforms and Output Load)

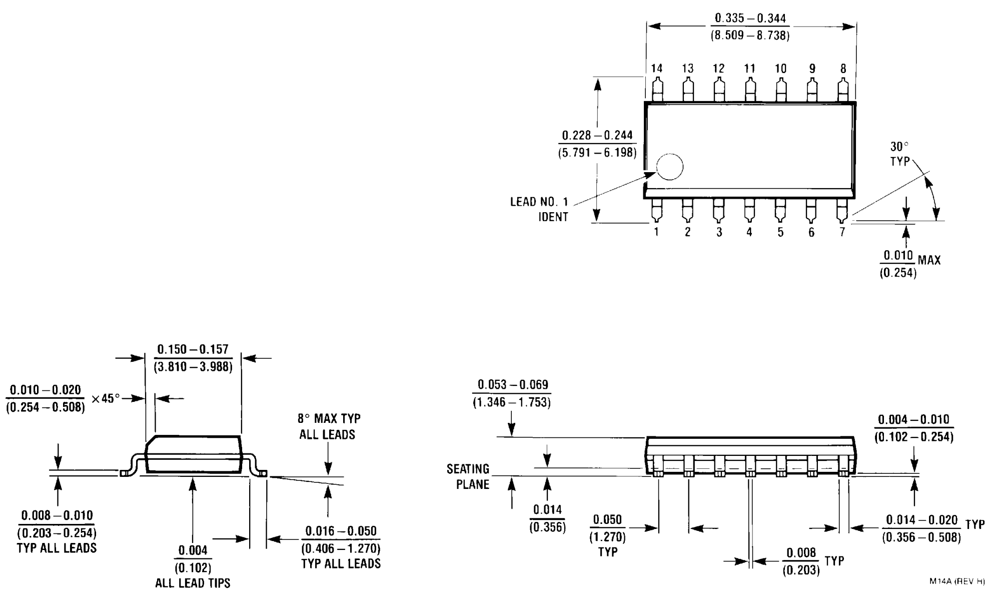
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Physical Dimensions inches (millimeters) unless otherwise noted

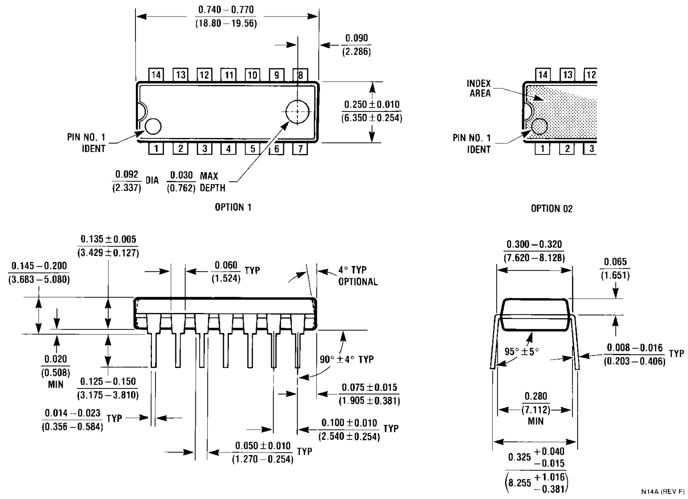


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS05DMQB or DM54LS05J
Package Number J14A

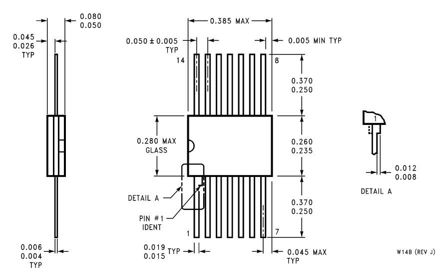


14-Lead Small Outline Molded Package (M)
Order Number DM74LS05M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS05N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number 54LS05FMQB or DM54LS05W
Package Number W14B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM7406
Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent buffers each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

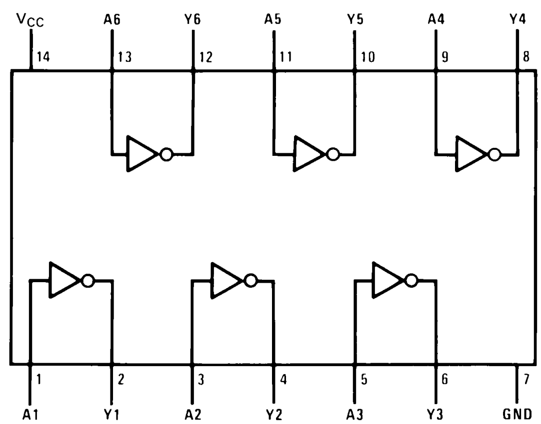
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



Order Number DM5406J, DM5406W, DM7406M or DM7406N
See Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM5406			DM7406			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		30	48	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		27	51	mA

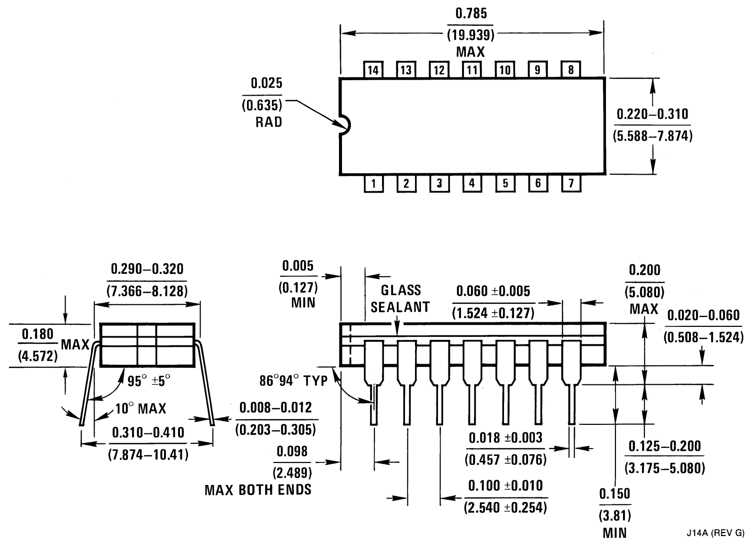
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

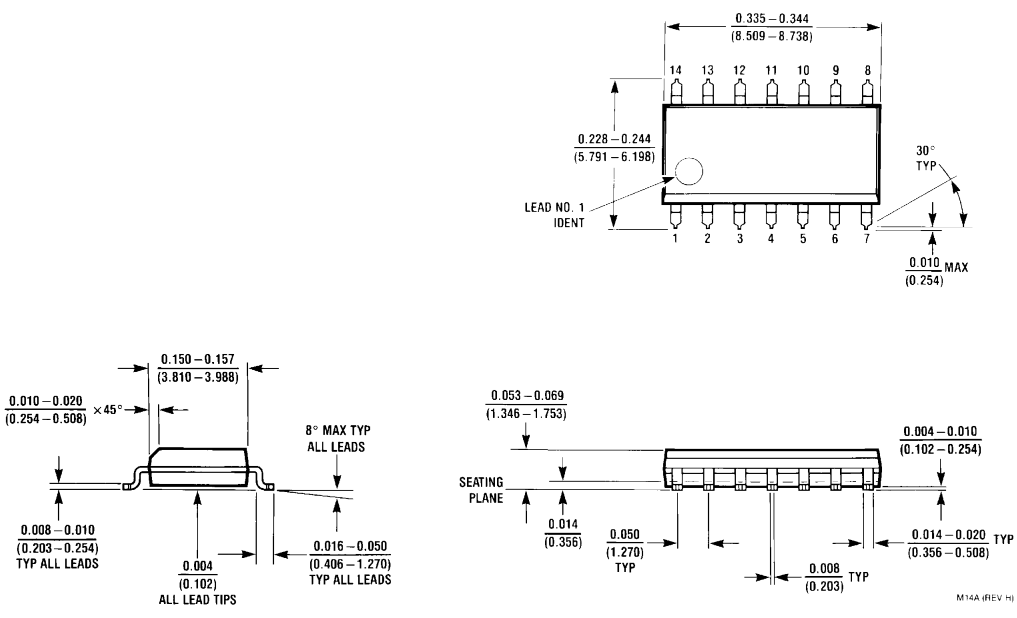
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			23	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Physical Dimensions inches (millimeters) unless otherwise noted

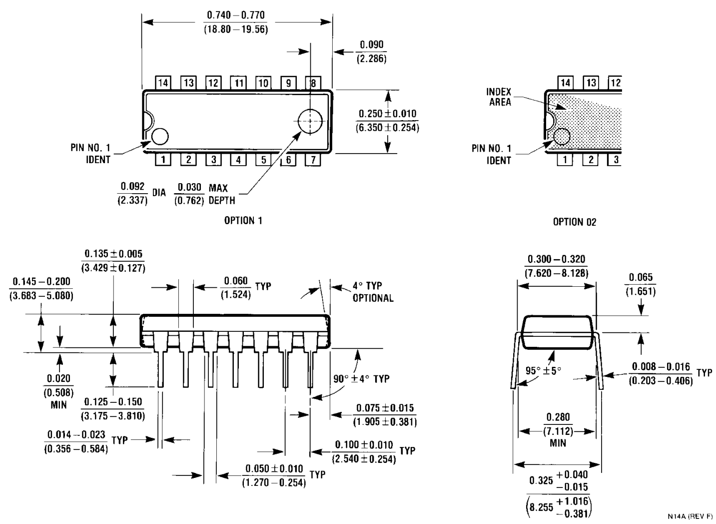


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM5406J
Package Number J14A

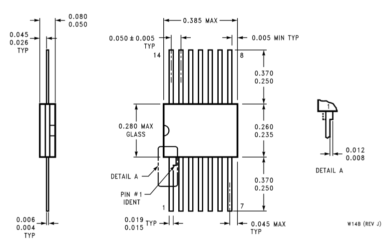


14-Lead Small Outline Molded Package (M)
Order Number DM7406M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM7406N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM5406W
Package Number W14B

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM7407
Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

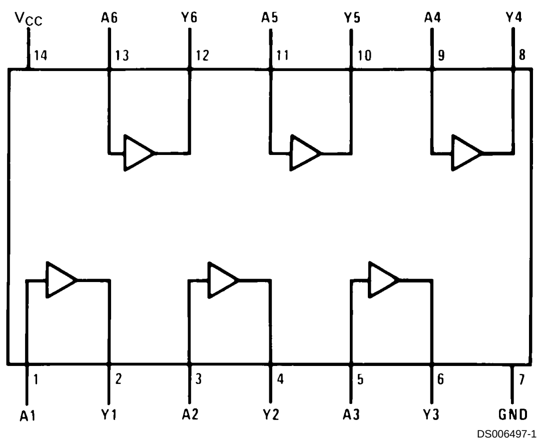
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



Order Number DM5407J, DM5407W, DM7407M or DM7407N
See Package Number J14A, M14A, N14A or W14B

Function Table

Y = A

Input	Output
A	**Y**
L	L
H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM5407			DM7407			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IH} = Min			250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		21	30	mA

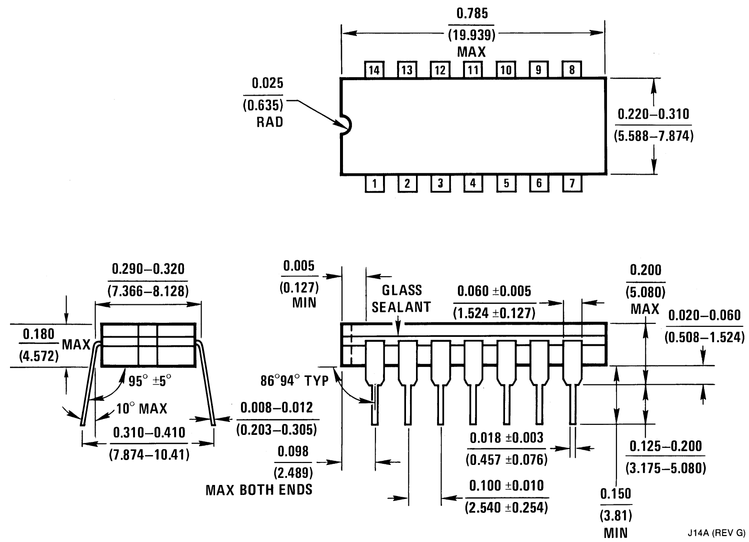
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

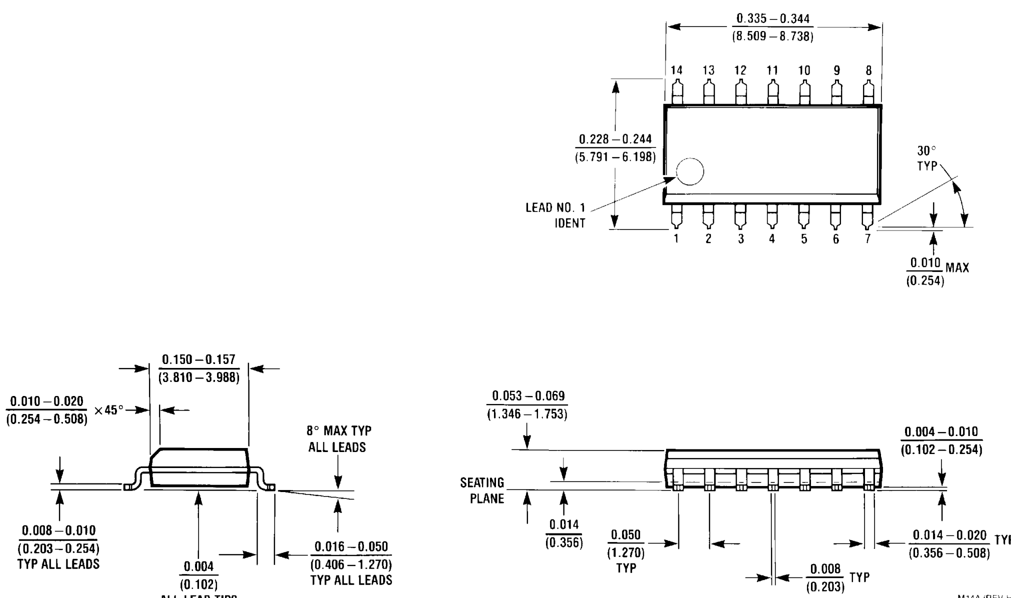
Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Physical Dimensions inches (millimeters) unless otherwise noted

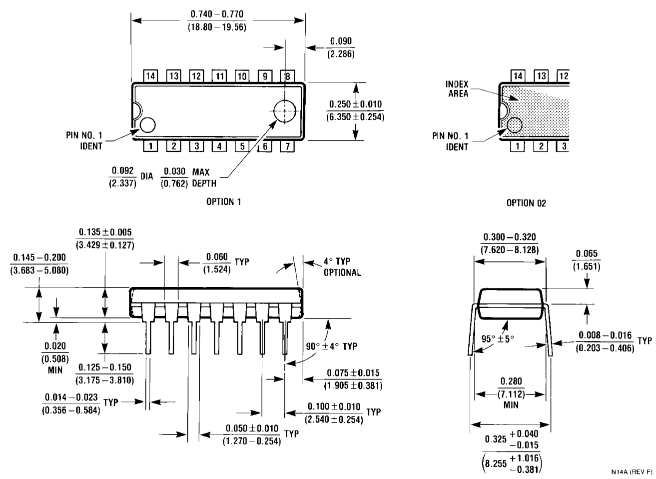


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM5407J
Package Number J14A

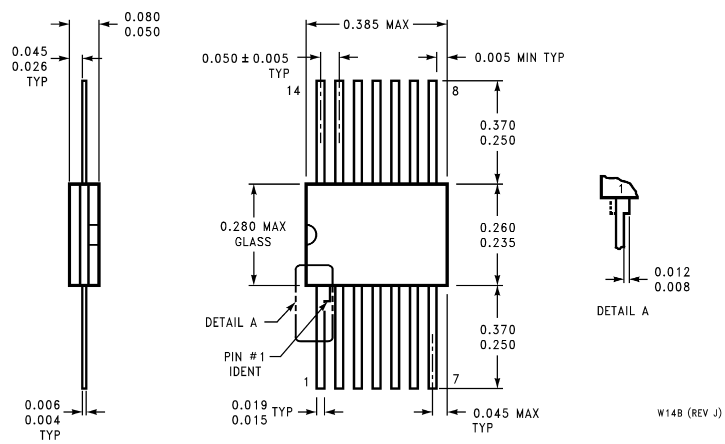


14-Lead Small Outline Molded Package (M)
Order Number DM7407M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM7407N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM5407W
Package Number W14B

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March 1998

DM74LS08
Quad 2-Input AND Gates

General Description

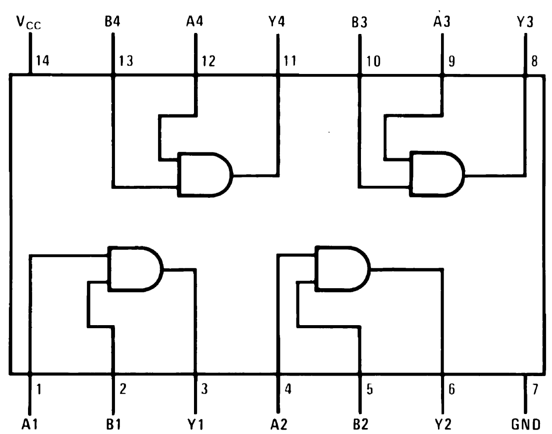
This device contains four independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS08) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006347-1

Order Number 54LS08DMQB, 54LS08FMQB, 54LS08LMQB, DM54LS08J, DM54LS08W, DM74LS08M or DM74LS08N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics

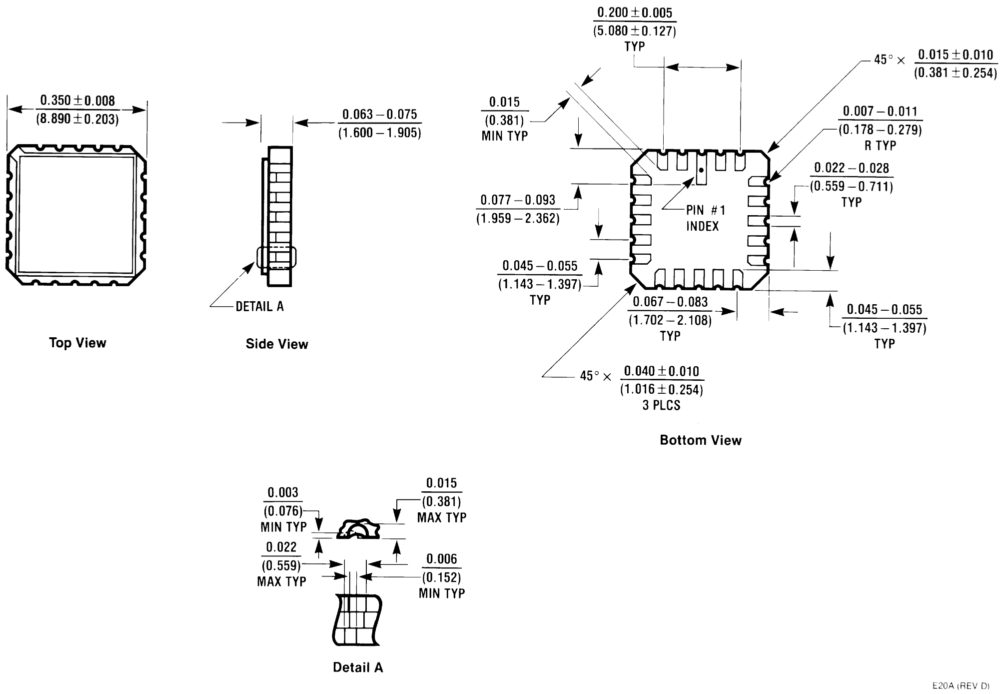
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

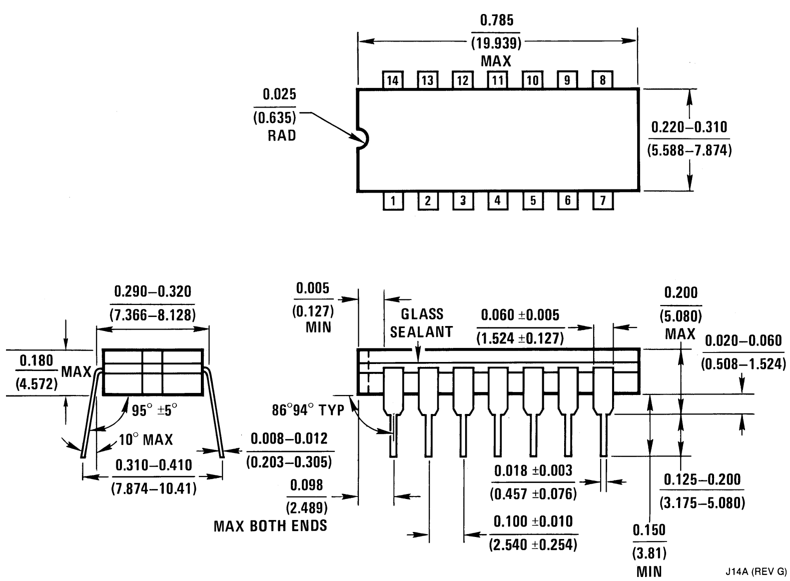
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

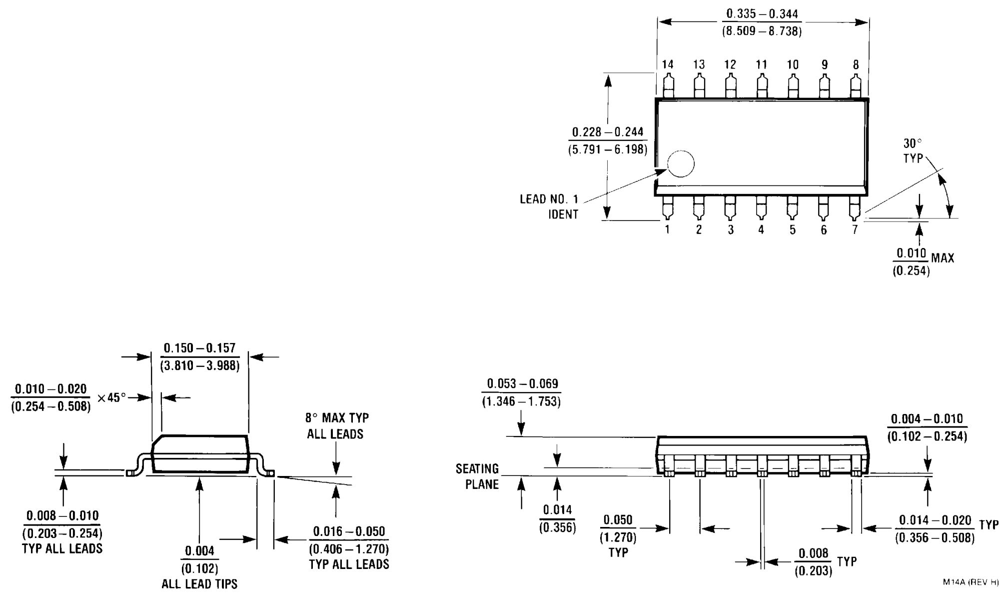


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS08LMQB
Package Number E20A

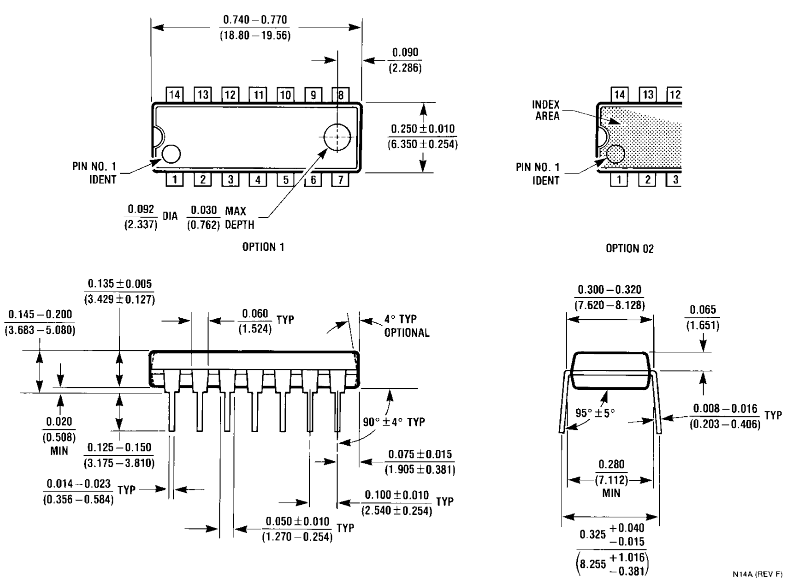


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS08DMQB or DM54LS08J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

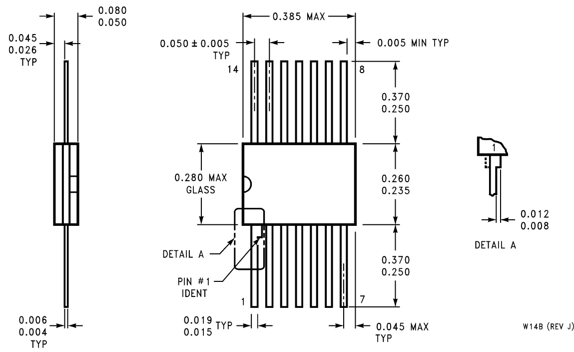


14-Lead Small Outline Molded Package (M)
Order Number DM74LS08M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS08N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS08FMQB or DM54LS08W
Package Number W14B

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March 1998

DM74LS09
Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS09) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\ (\text{Min}) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\ (\text{Max}) - V_{OL}}{I_{OL} - N_3\ (I_{IL})}$$

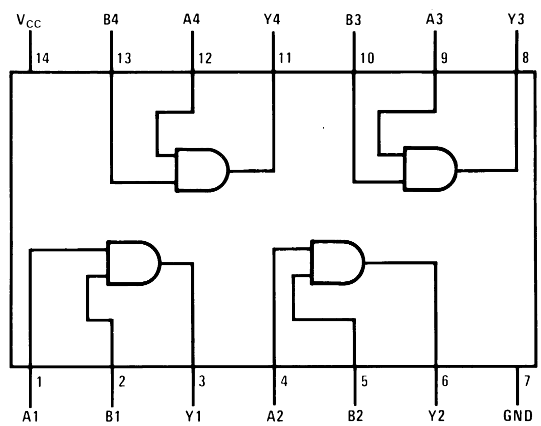
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



DS006348-1

Order Number 54LS09DMQB, 54LS09FMQB, DM54LS09J, DM54LS09W, DM74LS09M or DM74LS09N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = AB

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS09			DM74LS09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

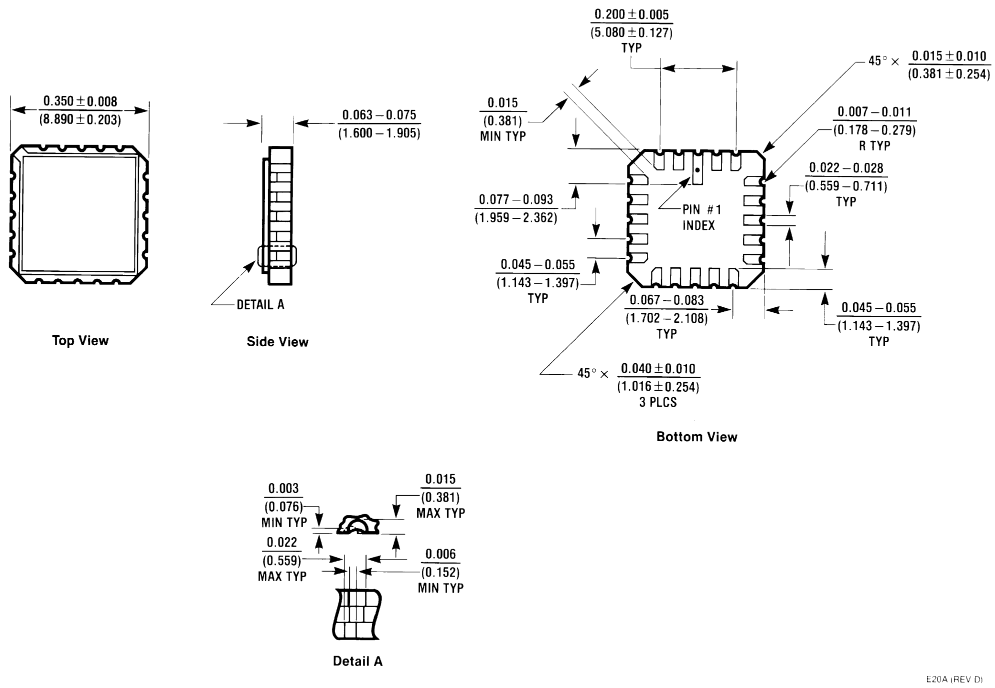
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

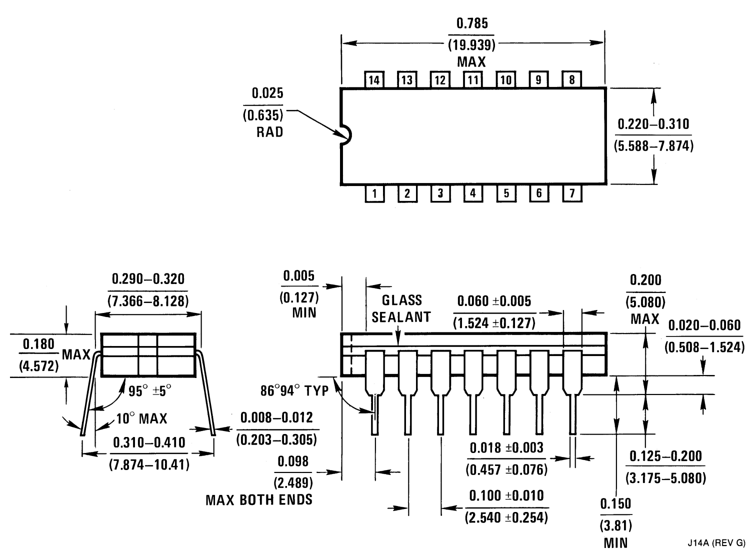
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	20	8	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	6	27	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Physical Dimensions inches (millimeters) unless otherwise noted

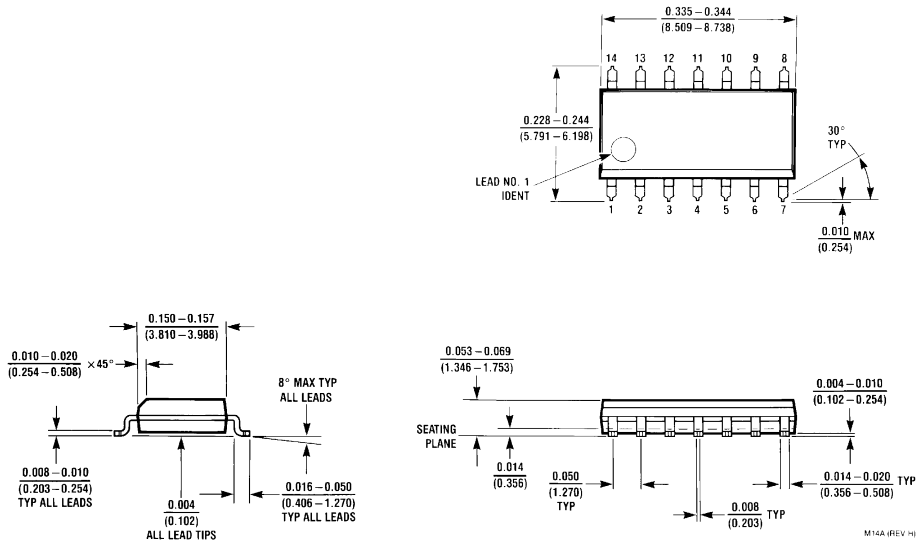


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS09LMQB
Package Number E20A

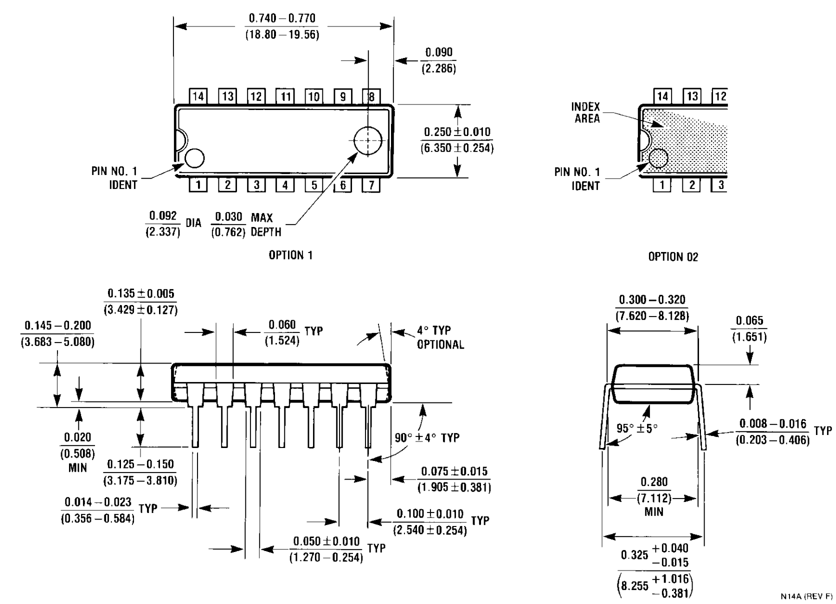


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS09DMQB or DM54LS09J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

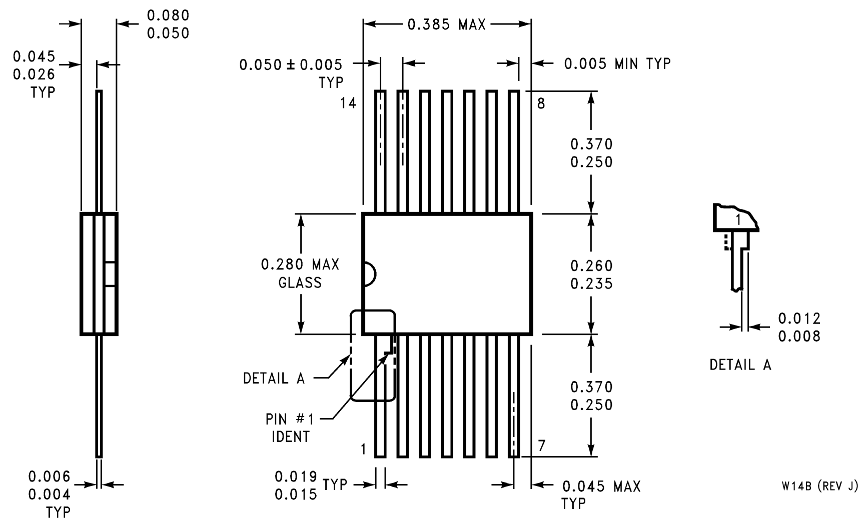


14-Lead Small Outline Molded Package (M)
Order Number DM74LS09M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS09N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS09FMQB or DM54LS09W
Package Number W14B

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March 1998

DM74LS10
Triple 3-Input NAND Gates

General Description

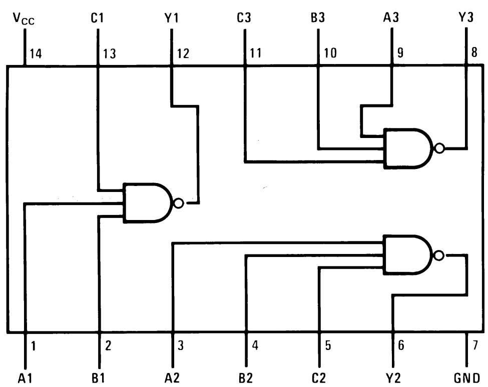
This device contains three independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS10) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006349-1

Order Number 54LS10DMQB, 54LS10FMQB, 54LS10LMQB, DM54LS10J, DM54LS10W, DM74LS10M or DM74LS10N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS10			DM74LS10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics

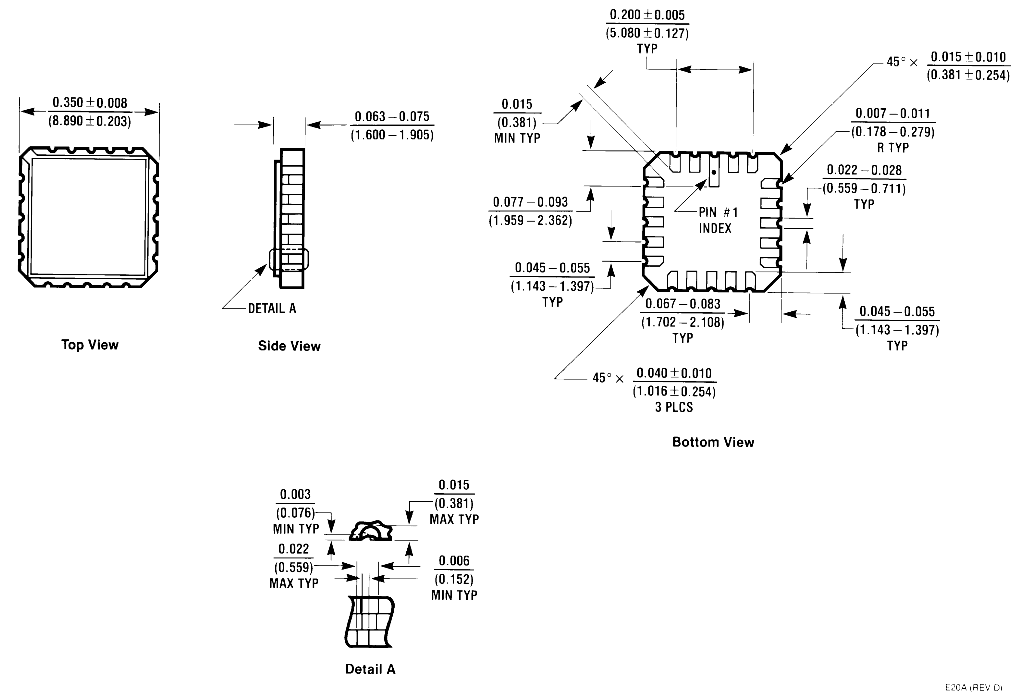
at V_{CC} = 5V and T_A = 25˚C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

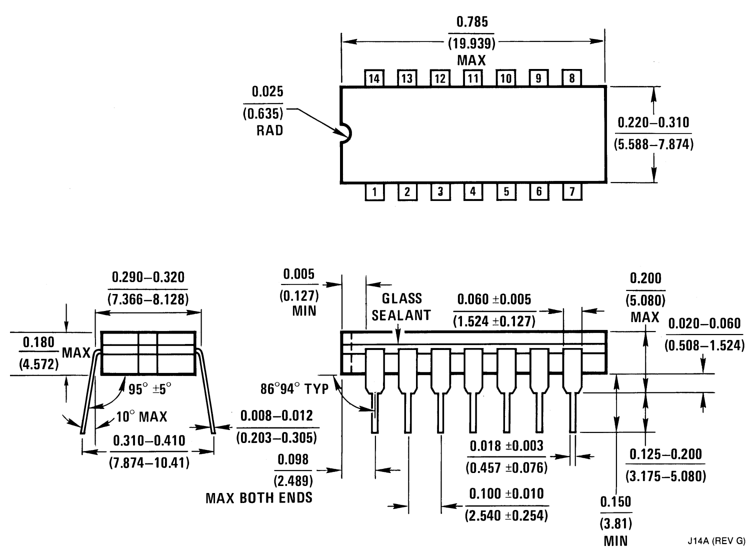
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

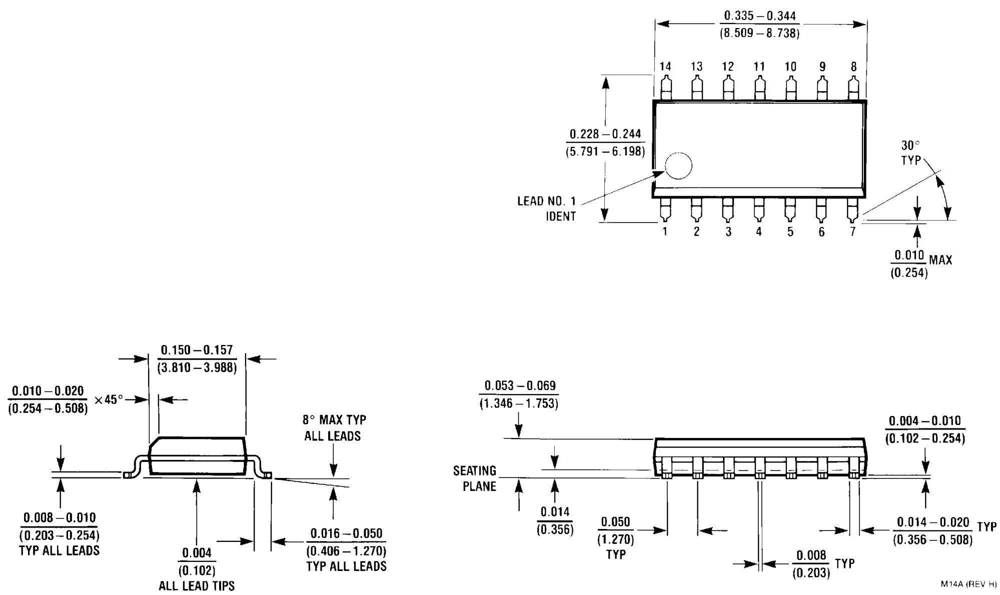


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS10LMQB
Package Number E20A

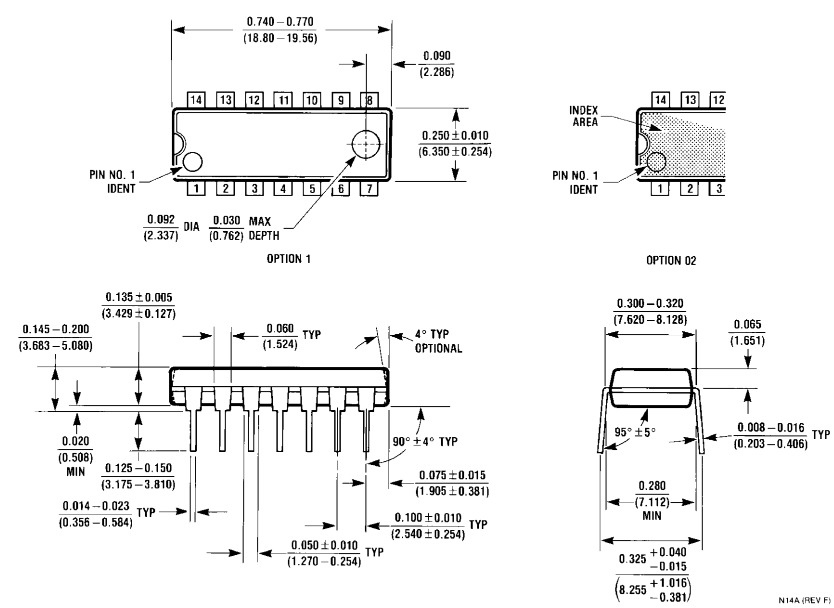


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS10DMQB or DM54LS10J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

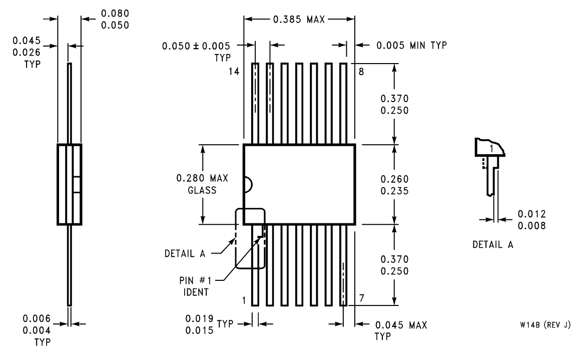


14-Lead Small Outline Molded Package (M)
Order Number DM74LS10M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS10N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS10FMQB or DM54LS10W
Package Number W14B

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March 1998

DM74LS11
Triple 3-Input AND Gates

General Description

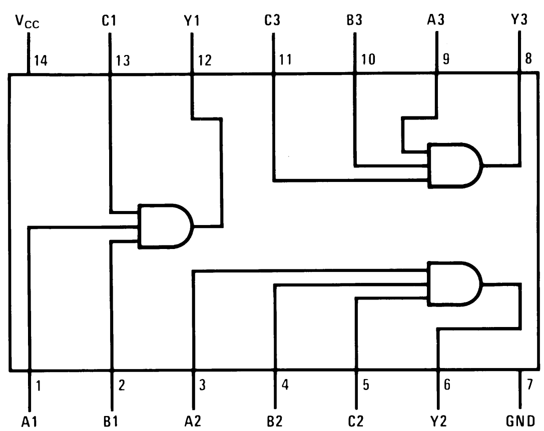
This device contains three independent gates each of which performs the logic AND function.

Features

- Alternate military/aerospace device (54LS11) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006350-1

Order Number 54LS11DMQB, 54LS11FMQB, 54LS11LMQB, DM54LS11J, DM54LS11W, DM74LS11M or DM74LS11N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = ABC

Inputs			Output
A	**B**	**C**	**Y**
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS11			DM74LS11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.8	3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.3	6.6	mA

Switching Characteristics

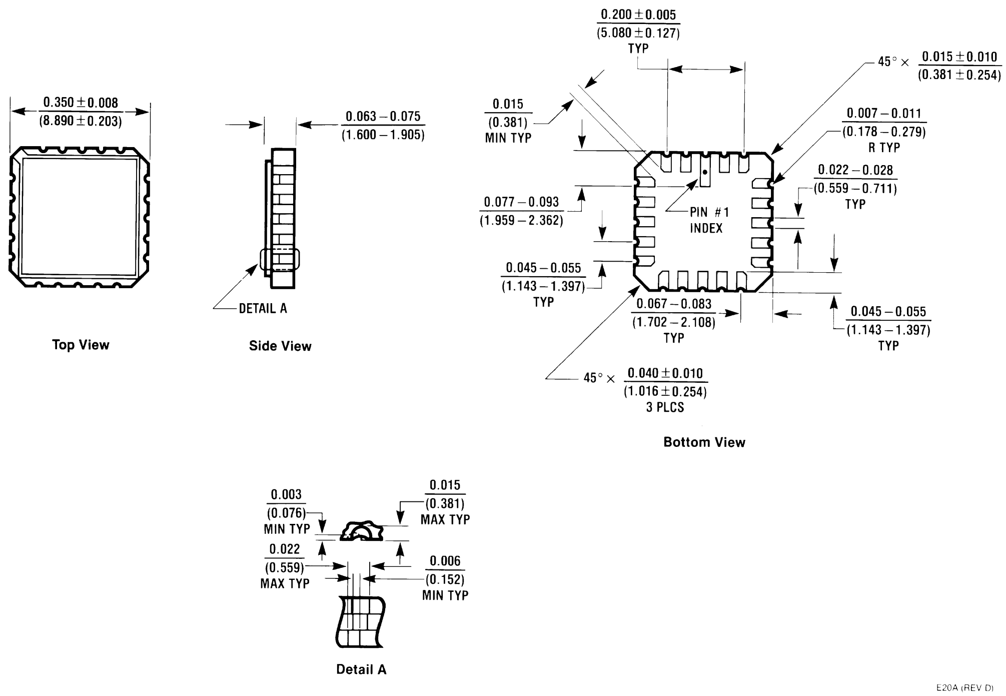
at V_{CC} = 5V and T_A = 25˚C (See for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	**Max**	**Min**	**Max**	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

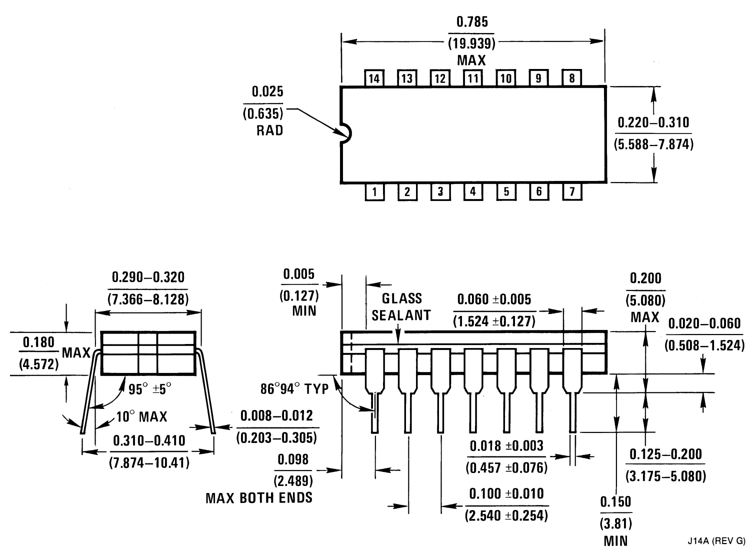
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

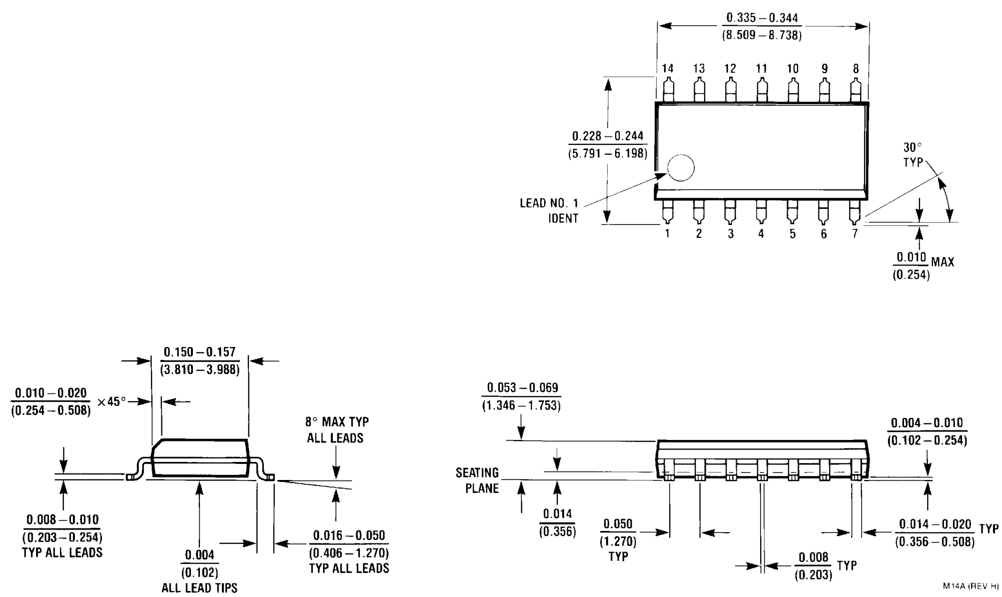


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS11LMQB
Package Number E20A

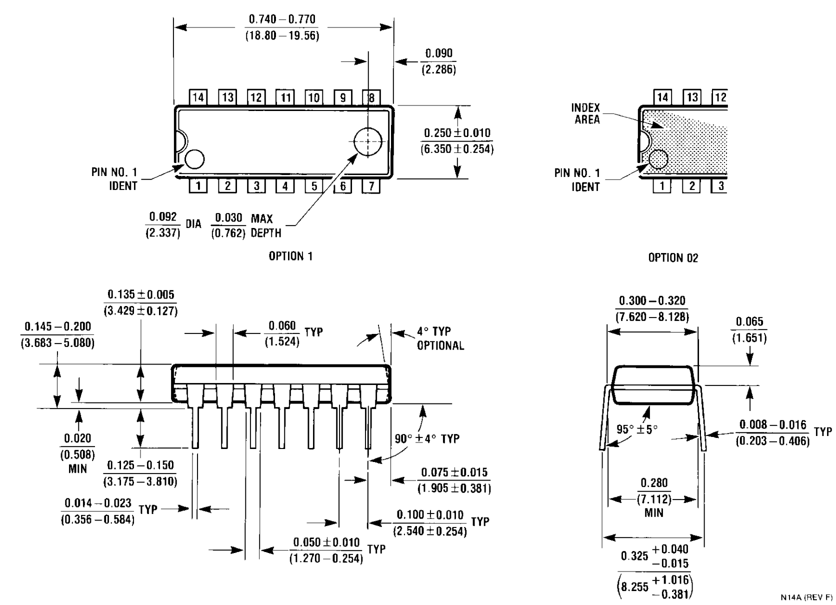


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS11DMQB or DM54LS11J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

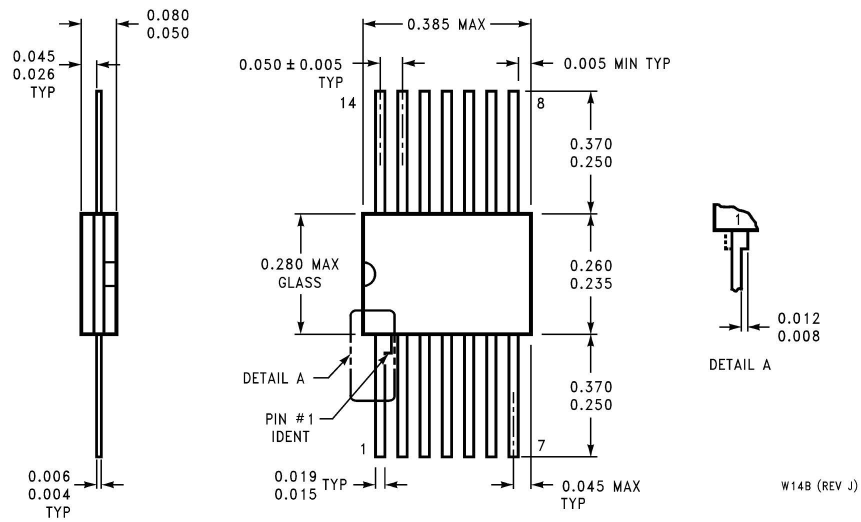


14-Lead Small Outline Molded Package (M)
Order Number DM74LS11M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS11N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS11FMQB or DM54LS11W
Package Number W14B

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National Semiconductor

June 1989

DM54LS12/DM74LS12 Triple 3-Input NAND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

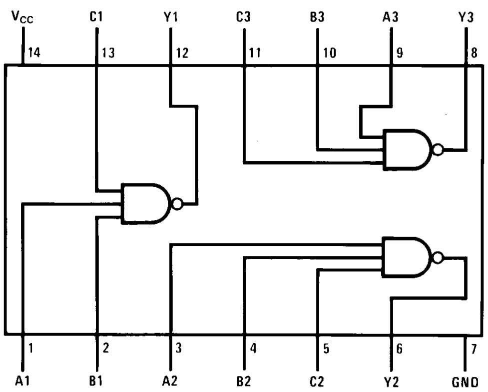
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6351–1

Order Number DM54LS12J, DM54LS12W, DM74LS12M or DM74LS12N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS12			DM74LS12			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

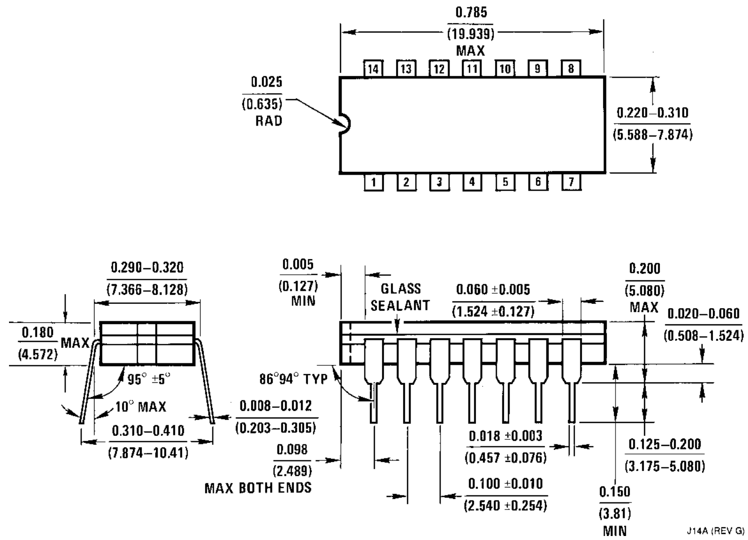
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5 V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.7	1.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

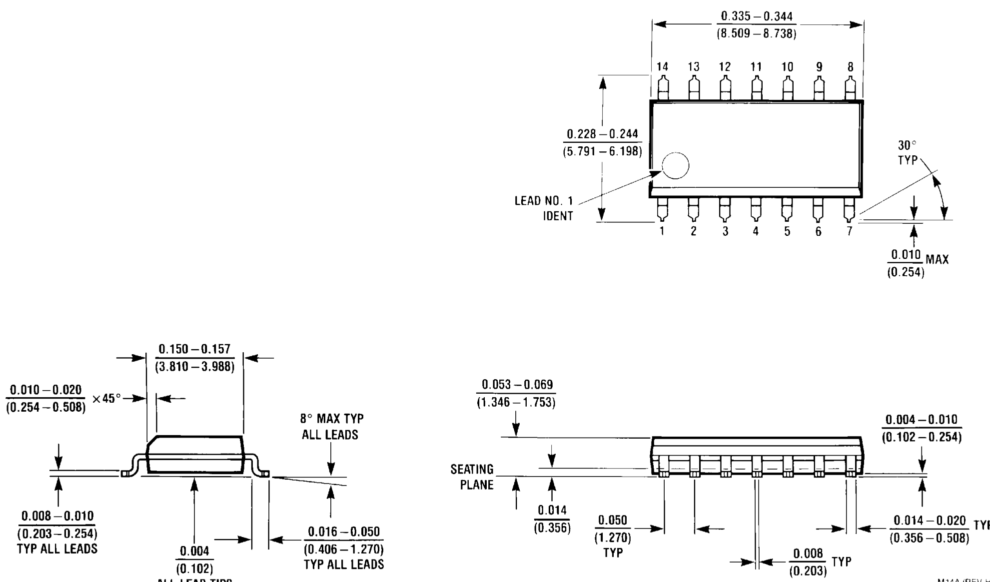
Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Physical Dimensions inches (millimeters)



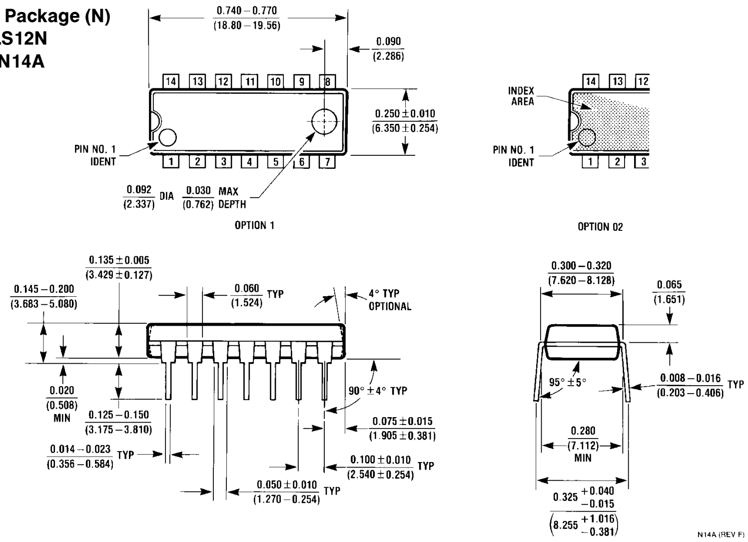
14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS12J
NS Package Number J14A



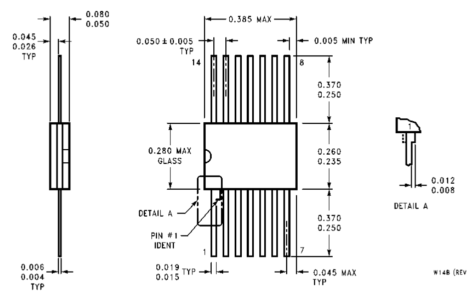
14-Lead Small Outline Molded Package (M)
Order Number DM74LS12M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)

14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS12N
NS Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS12W
NS Package Number W14B



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National Semiconductor

September 1992

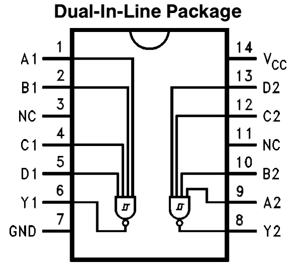
DM74LS13
Dual 4-Input Schmitt Trigger

General Description

This device contains two independent gates each of which perform the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/10166–1

Order Number DM74LS13M or DM74LS13N
See NS Package Number M14A or N14A

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	**B**	**C**	**D**	**Y**
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Level Logic

L = Low Level Logic

X = Either Low or High Level Logic

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS13			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max V_{IN} = GND			6.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max V_{IN} = OPEN			7.0	mA
V_{T+}	Positive-Going Threshold Voltage	V_{CC} = +5.0V	1.5		2.0	V
V_{T-}	Negative-Going Threshold Voltage	V_{CC} = +5.0V	0.6		1.1	V
$V_{T+} - V_{T-}$	Hysteresis Voltage	V_{CC} = +5.0V	0.4			V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = +5.0V, V_{IN} = V_{T+}		−0.14*		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = +5.0V, V_{IN} = V_{T-}		−0.18*		mA

*Typical Value

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

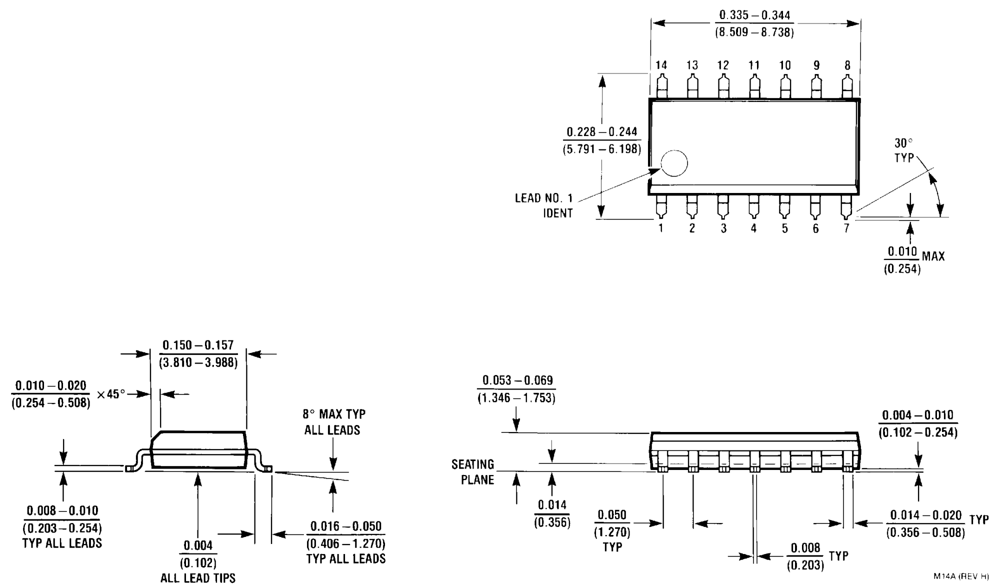
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

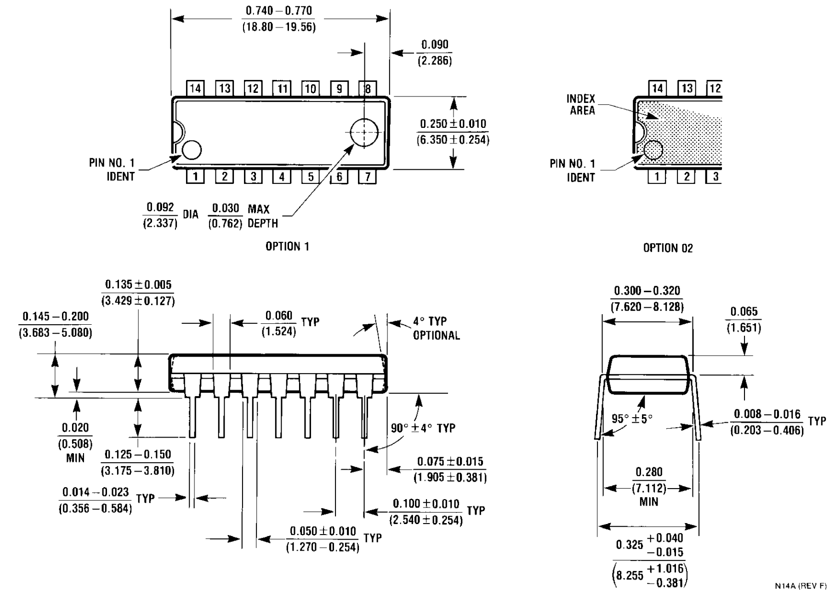
Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$ DM74LS13 Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		27	ns

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS13M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS13N
NS Package Number N14A

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March 1998

FAIRCHILD SEMICONDUCTOR™

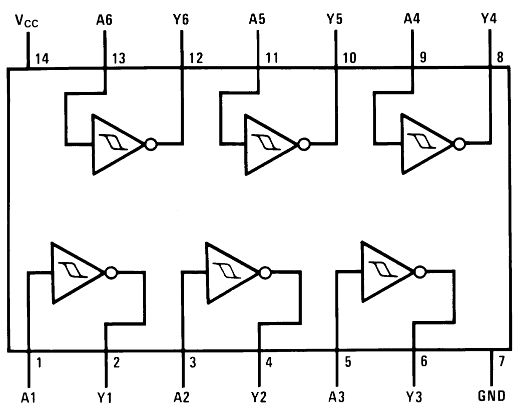
DM74LS14
Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



DS006353-1

Order Number 54LS14DMQB, 54LS14FMQB, 54LS14LMQB, DM74LS14M or DM74LS14N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	**Y**
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.6	0.8	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}	DM74		−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}	DM74		−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 2: V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25˚C.

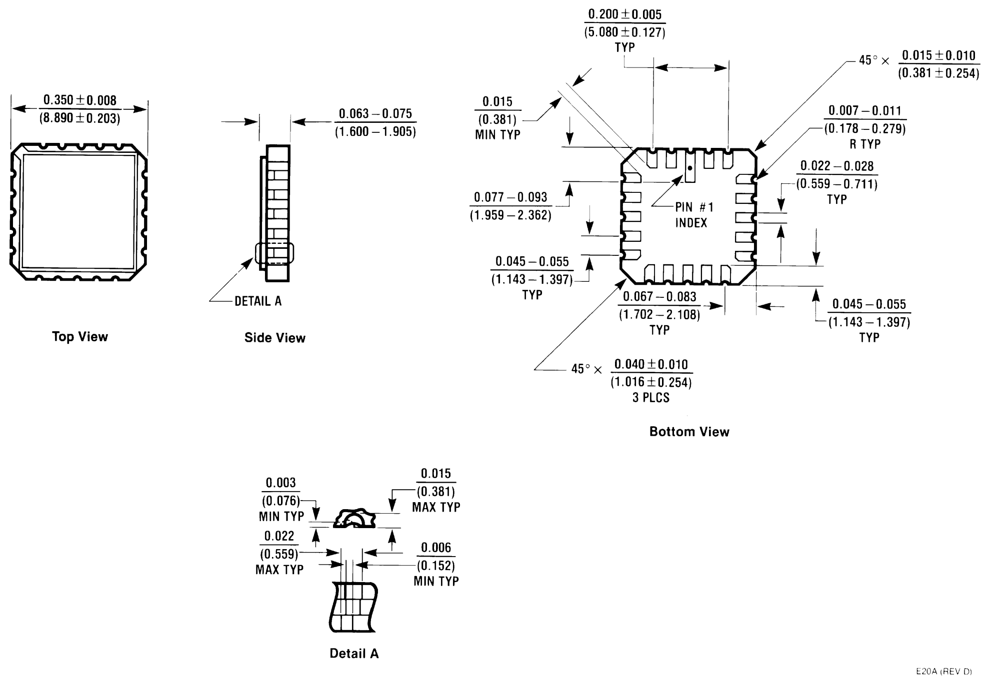
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

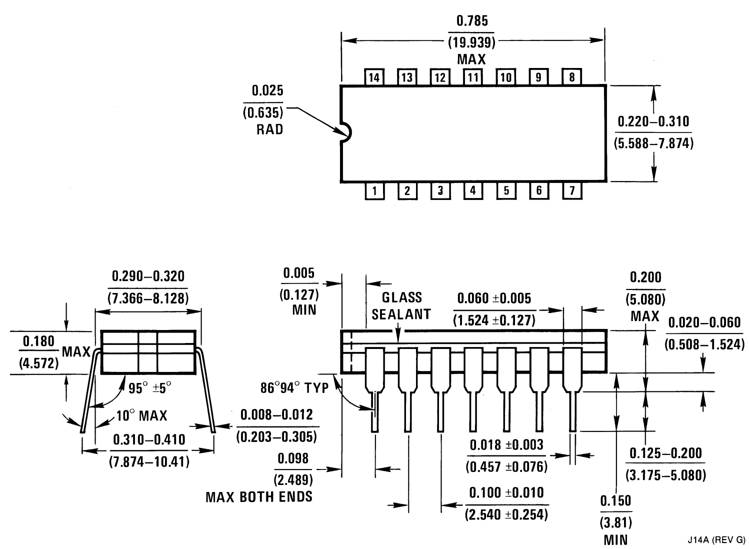
at V_{CC} = 5V and T_A = 25˚C (See for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

Physical Dimensions inches (millimeters) unless otherwise noted

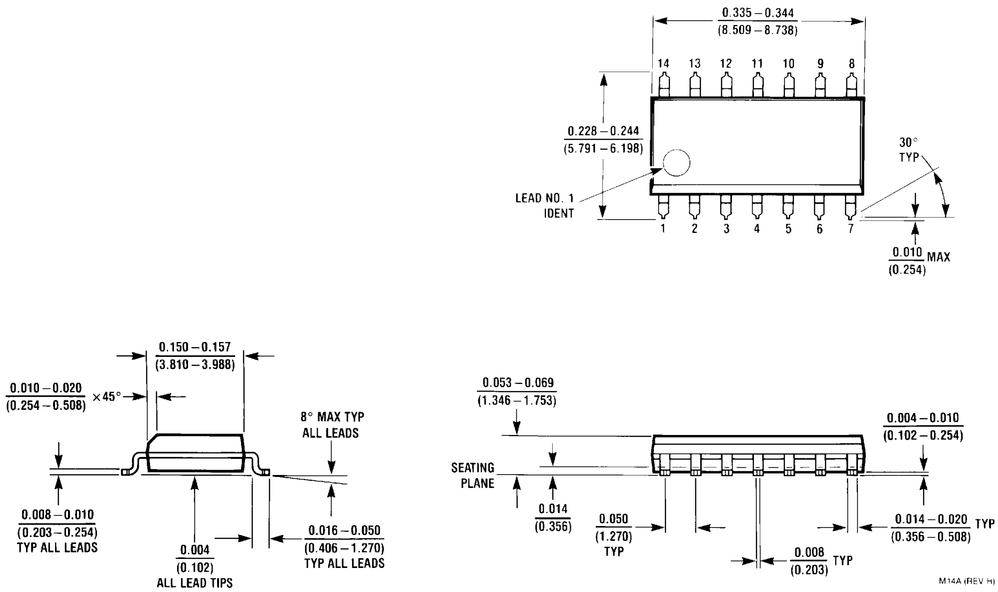


Ceramic Leadless Chip Carrier (E)
Order Number 54LS14LMQB
Package Number E20A

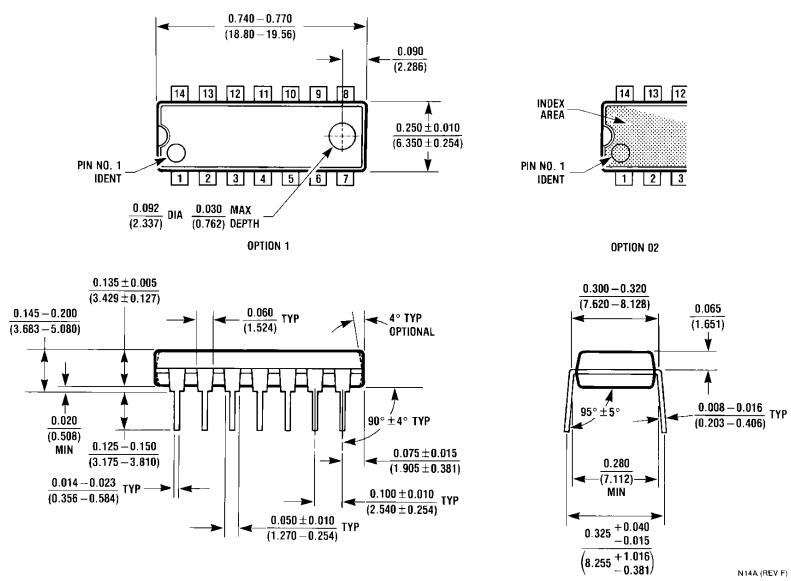


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS14DMQB
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

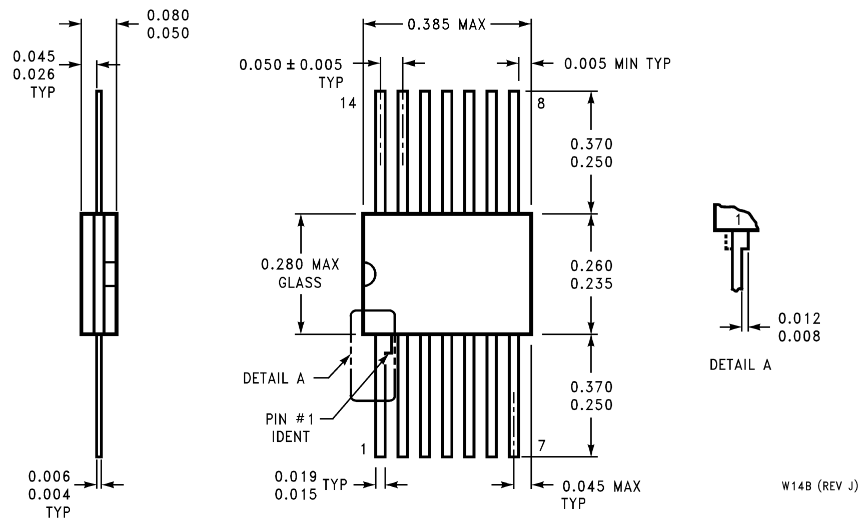


14-Lead Small Outline Molded Package (M)
Order Number DM74LS14M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS14N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS14FMQB
Package Number W14B

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National Semiconductor

May 1992

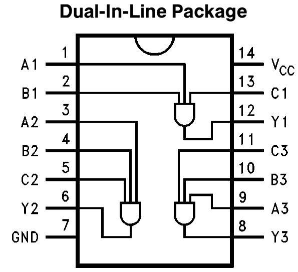
DM54LS15/DM74LS15 Triple 3-Input AND Gate with Open-Collector Outputs

General Description

This device contains three independent gates, each of which perform the logic AND function. The outputs are open-collector.

Connection Diagram

Dual-In-Line Package



TL/F/10167–1

Order Number DM54LS15J, DM54LS15W, DM74LS15M or DM74LS15N
See NS Package Number J14A, M14A, N14A or W14B

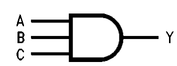
Function Table

(Each Gate)

Inputs			Output
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

Logic Diagram

(Each Gate)



TL/F/10167–1

Positive Logic

$Y = A \bullet B \bullet C$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C}}$

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions at V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	DM54LS15			DM74LS15			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

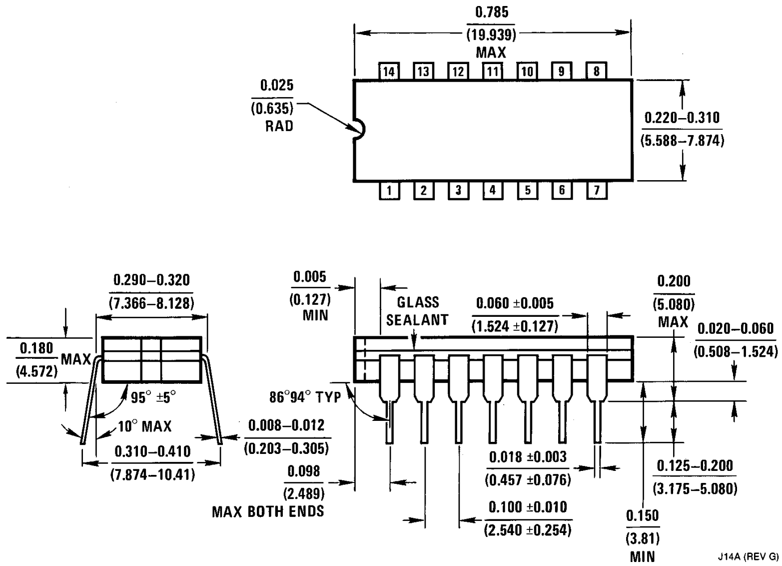
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (for DM54)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = OPEN				3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{IN} = GND				6.6	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

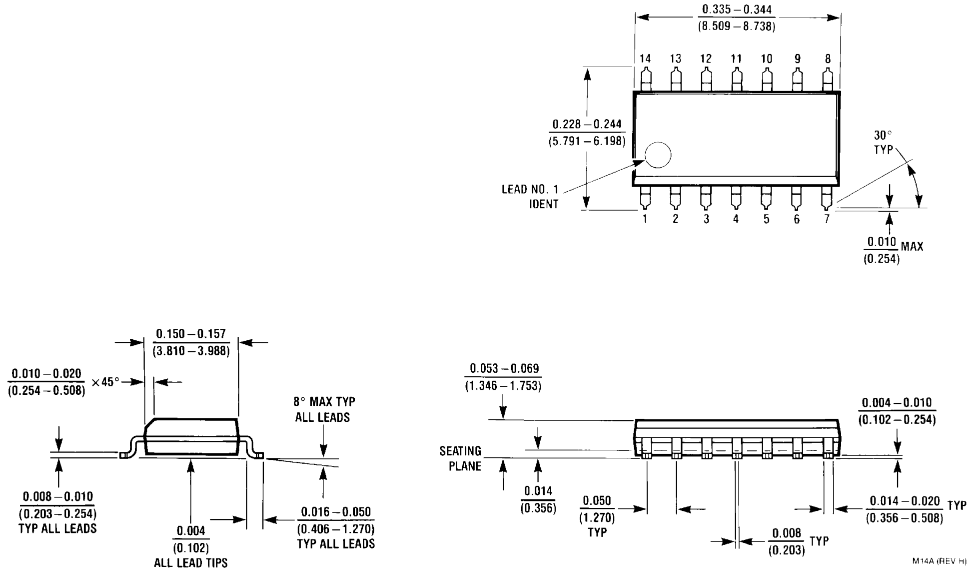
Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$ Max		Units
		DM54	DM74	
t_{PLH}	Propagation Delay Time Low to High Level Output	24	20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	18	15	ns

Physical Dimensions inches (millimeters)

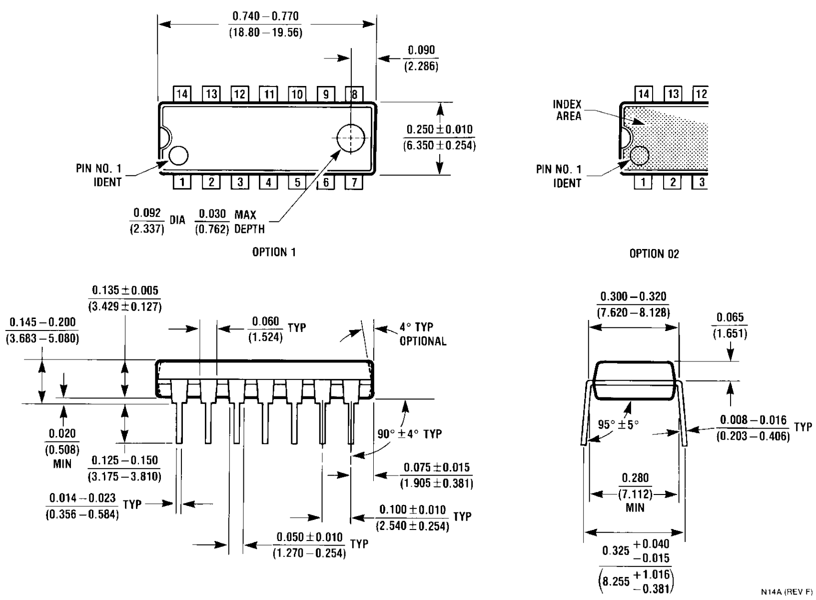


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS15J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

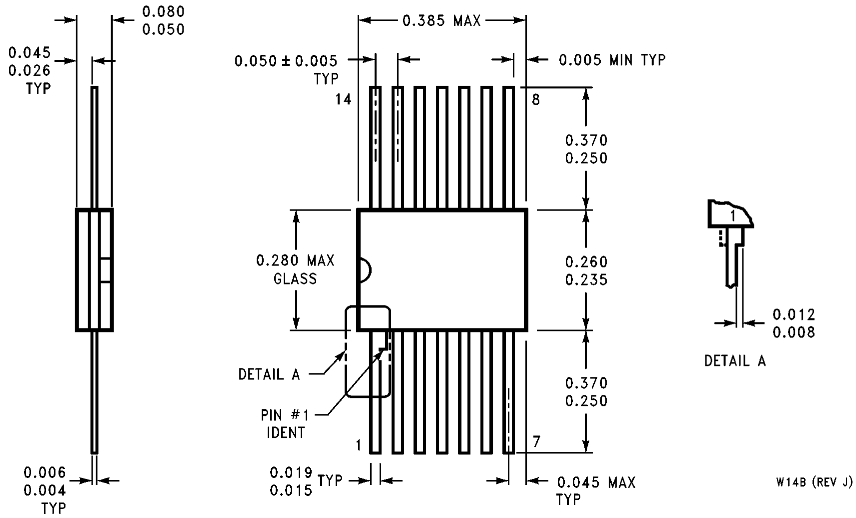


14-Lead Small Outline Molded Package (M)
Order Number DM74LS15M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS15N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS15W
NS Package Number W14B

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FAIRCHILD
SEMICONDUCTOR TM

March 1998

DM74LS20
Dual 4-Input NAND Gates

General Description

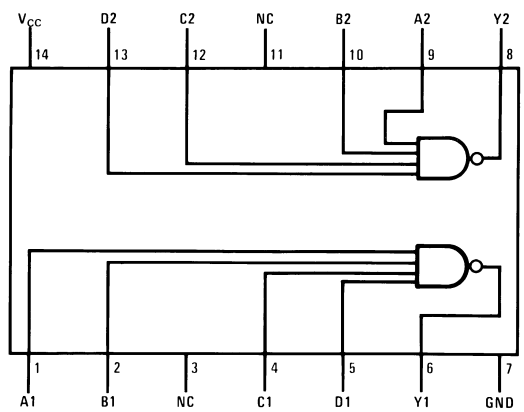
This device contains two independent gates each of which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS20) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



DS006355-1

Order Number 54LS20DMQB, 54LS20FMQB, 54LS20LMQB, DM54LS20J, DM54LS20W, DM74LS20M or DM74LS20N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

 DS006355

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS20			DM74LS20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.2	2.2	mA

Switching Characteristics

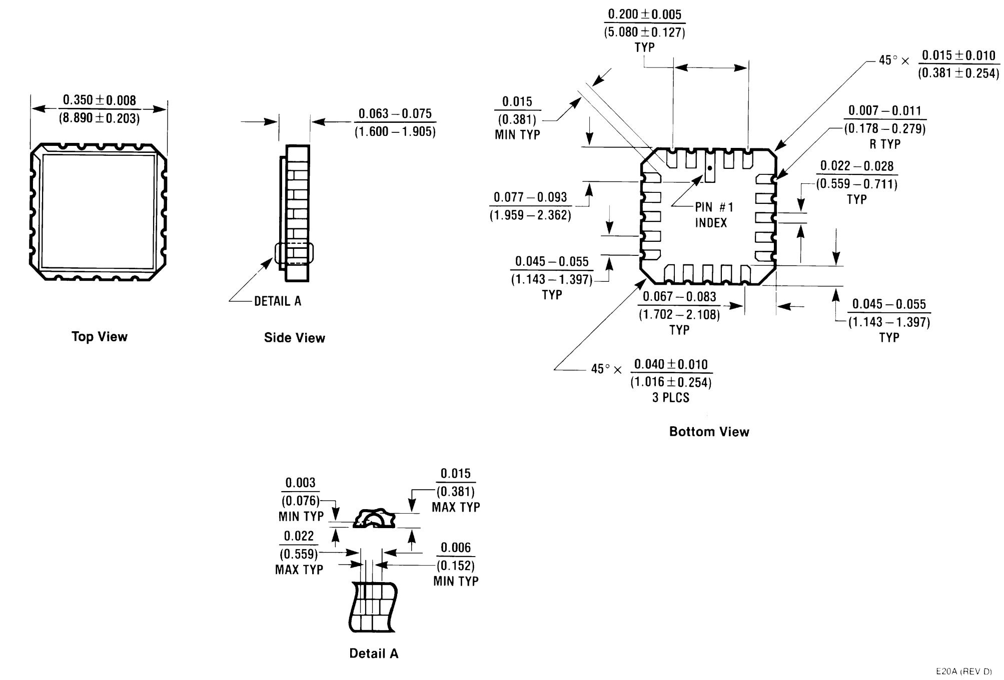
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

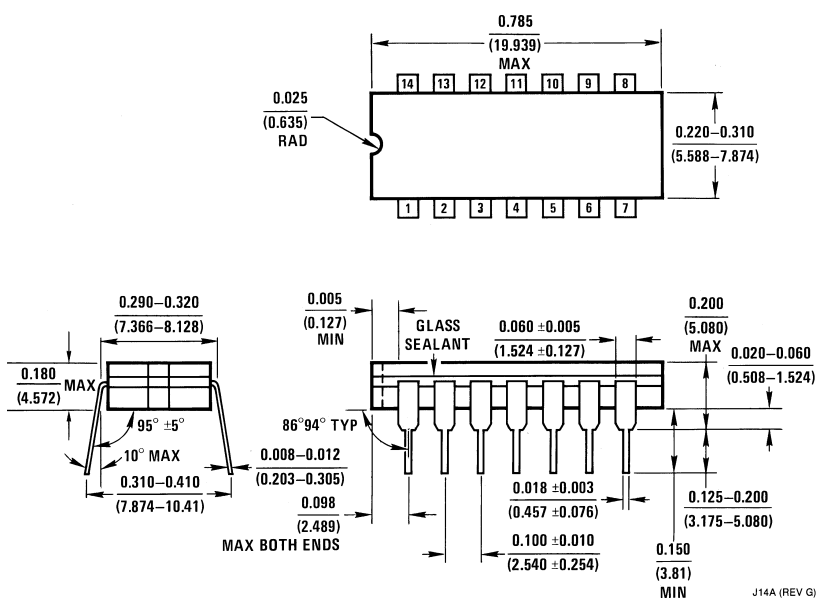
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

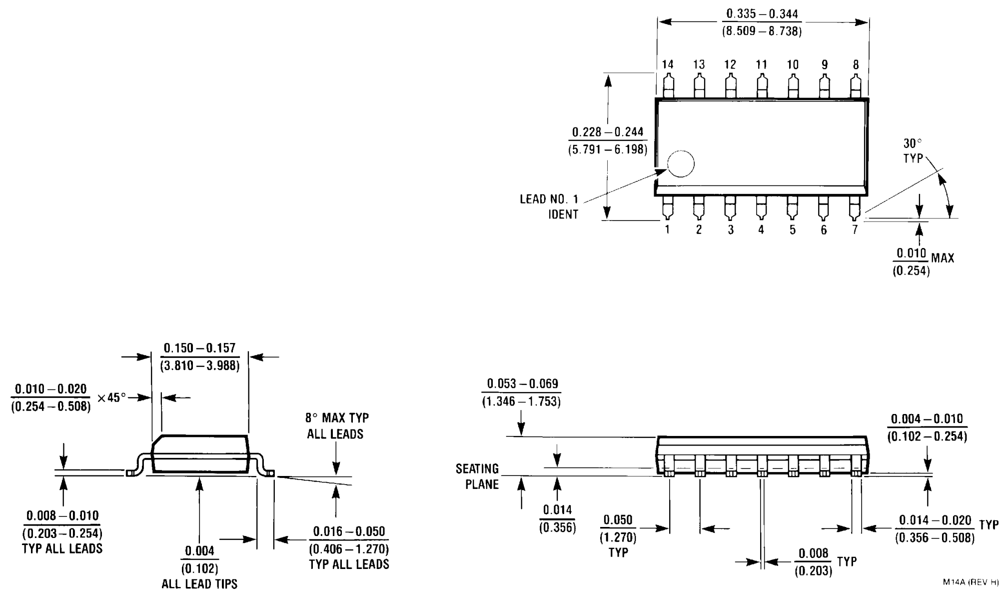


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS20LMQB
Package Number E20A

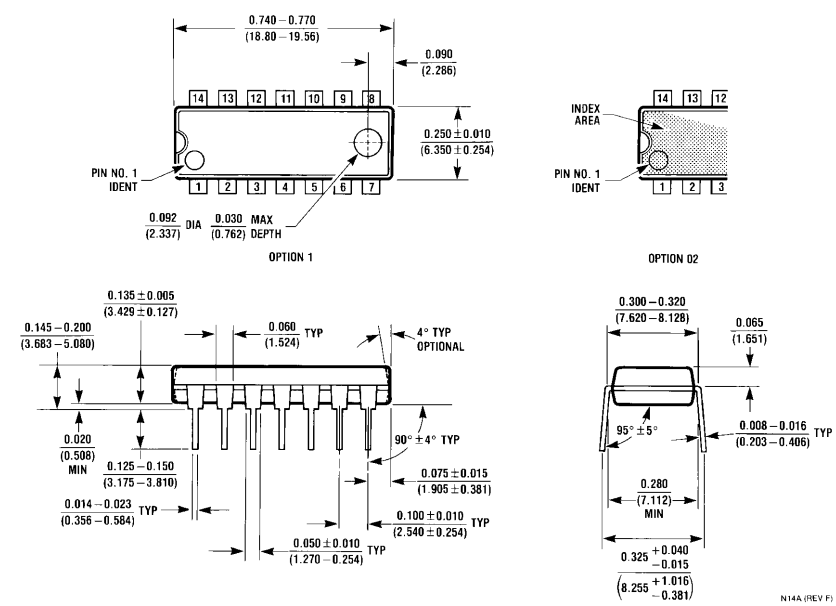


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS20DMQB or DM54LS20J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

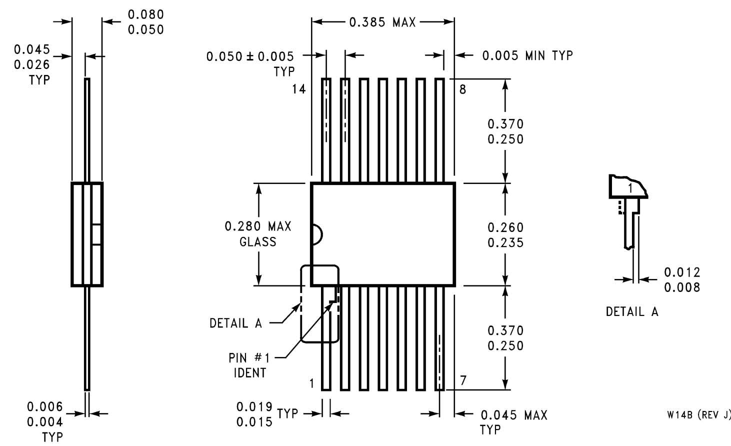


14-Lead Small Outline Molded Package (M)
Order Number DM74LS20M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS20N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS20FMQB or DM54LS20W
Package Number W14B

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National Semiconductor

June 1989

54LS21/DM54LS21/DM74LS21 Dual 4-Input AND Gates

General Description

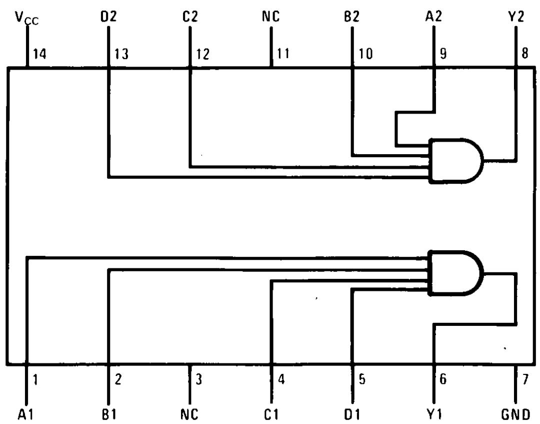
This device contains two independent gates each of which performs the logic AND function.

Features

- Alternate Military/Aerospace device (54LS21) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6356–1

Order Number 54LS21DMQB, 54LS21FMQB, 54LS21LMQB, DM54LS21J, DM54LS21W, DM74LS21M or DM74LS21N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = ABCD

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS21			DM74LS21			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.2	4.4	mA

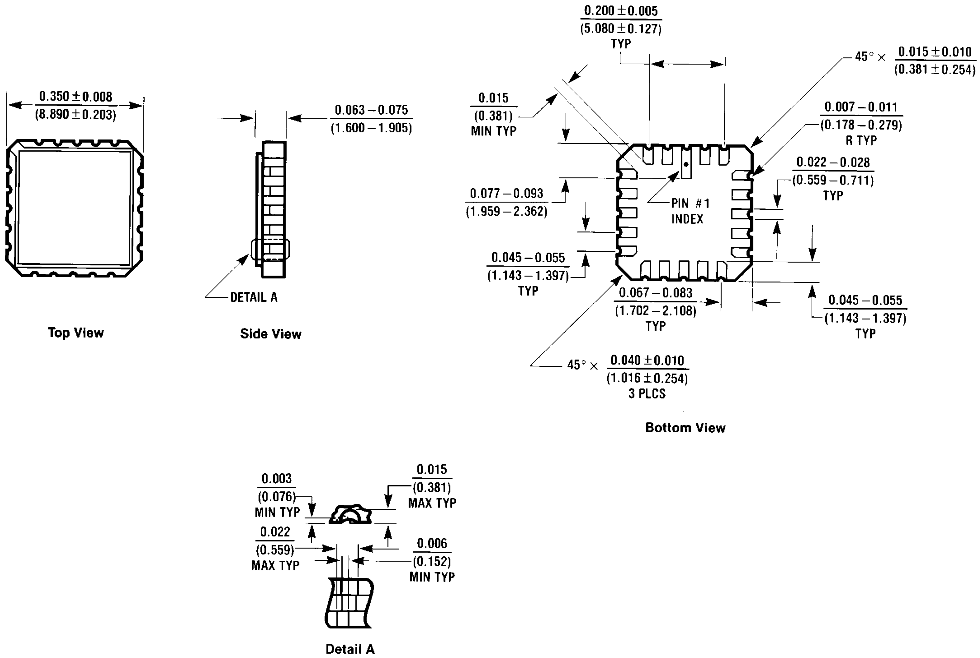
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

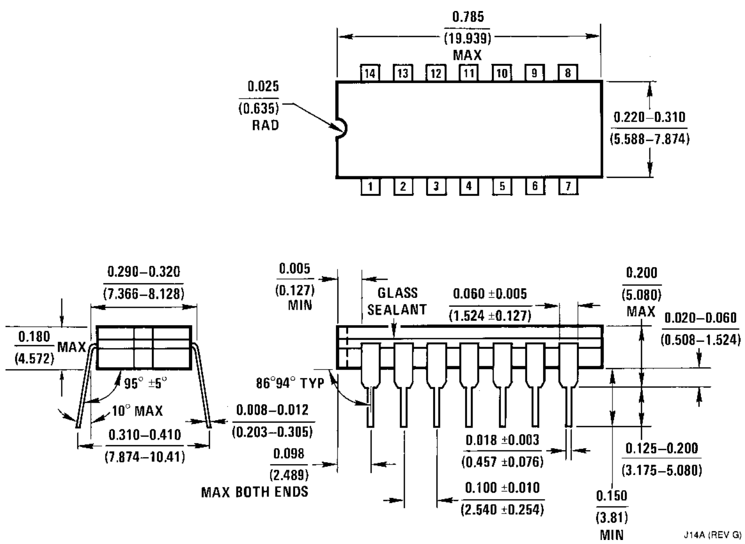
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters)

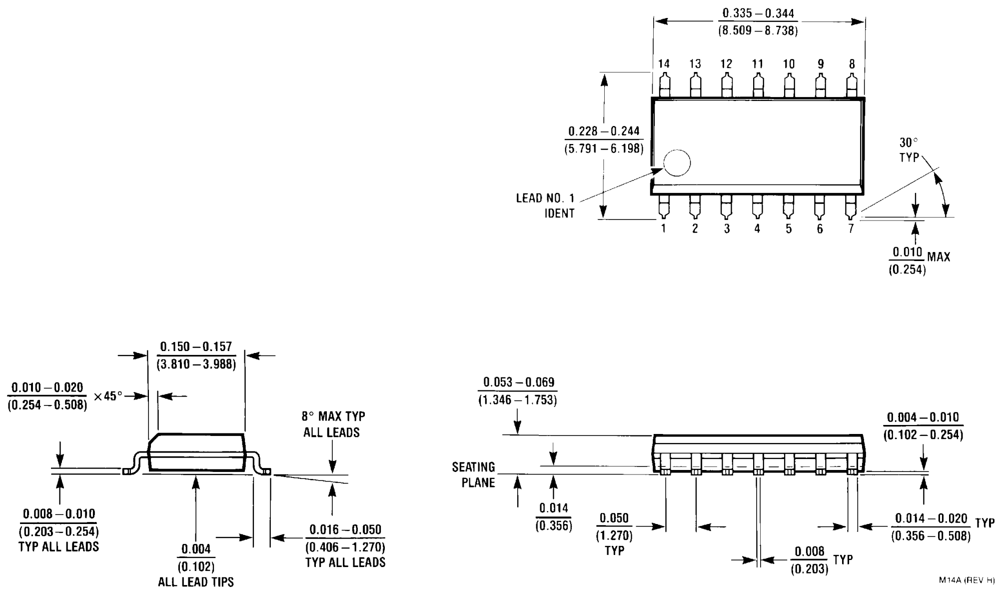


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS20LMQB
NS Package Number E20A

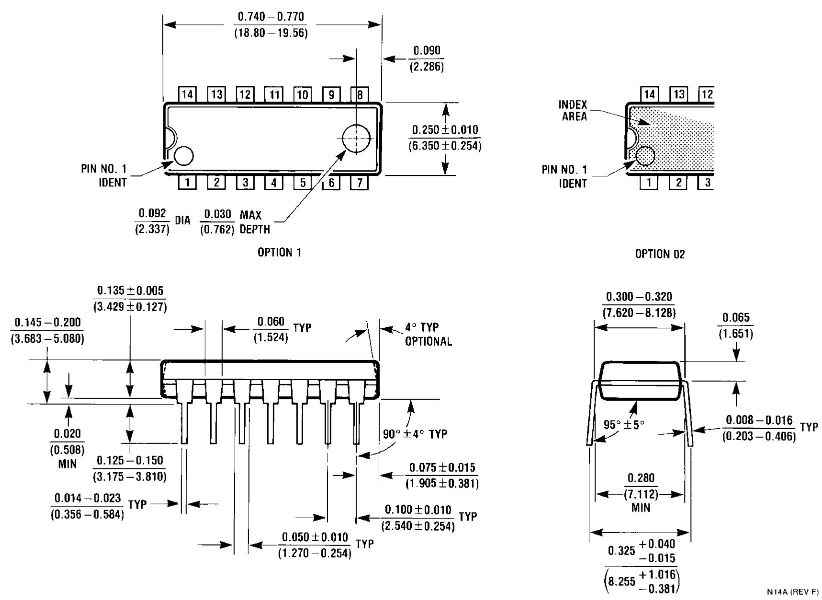


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS20DMQB or DM54LS21J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

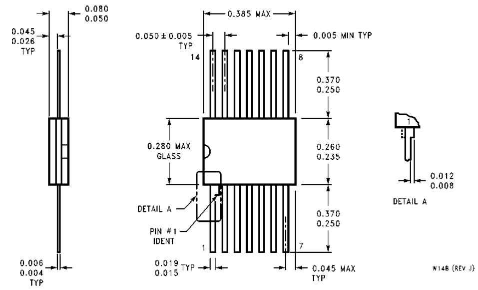


14-Lead Small Outline Molded Package (M)
Order Number DM74LS21M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS21N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS21FMQB or DM54LS21W
NS Package Number W14B

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National Semiconductor

February 1992

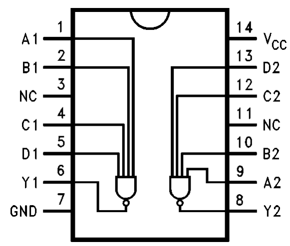
DM74LS22 Dual 4-Input NAND Gate with Open-Collector Output

General Description

The 'LS22 contains two independent NAND gates, each with four data inputs.

Connection Diagram

Dual-In-Line Package



TL/F/10168–1

Order Number DM74LS22M or DM74LS22N
See NS Package Number M14A or N14A

Truth Table

$Y = \overline{ABCD}$

Inputs				Outputs
A	**B**	**C**	**D**	**Y**
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

 TL/F/10168

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS22			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM74			0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply Current Outputs High	V_{CC} = Max, V_{IN} = GND				0.8	mA
I_{CCL}	Supply Current Outputs Low	V_{CC} = Max, V_{IN} = Open				2.2	mA

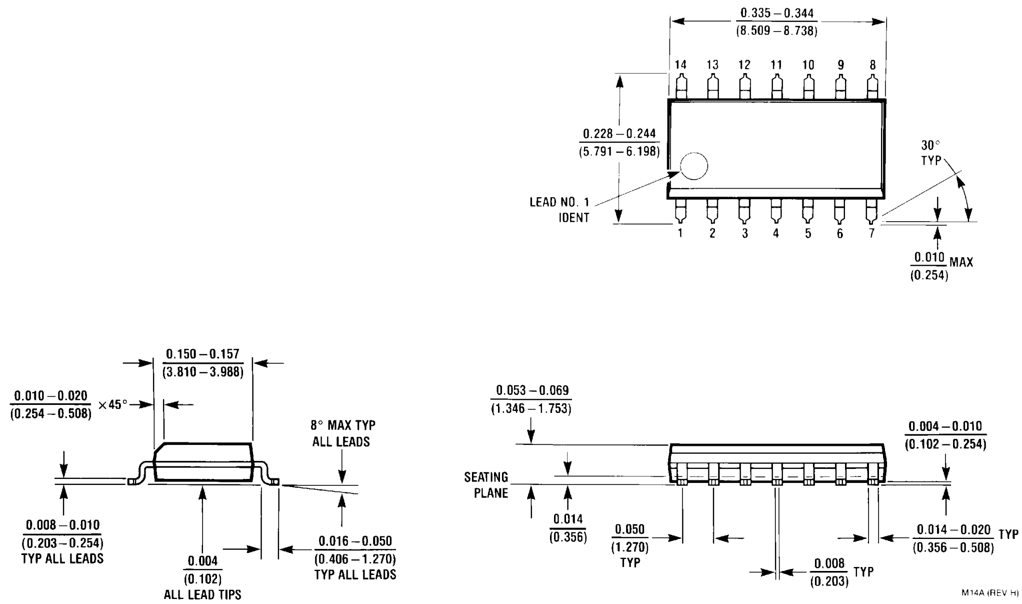
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

at $V_{CC} = +5.0V$, $T_A = +25°C$

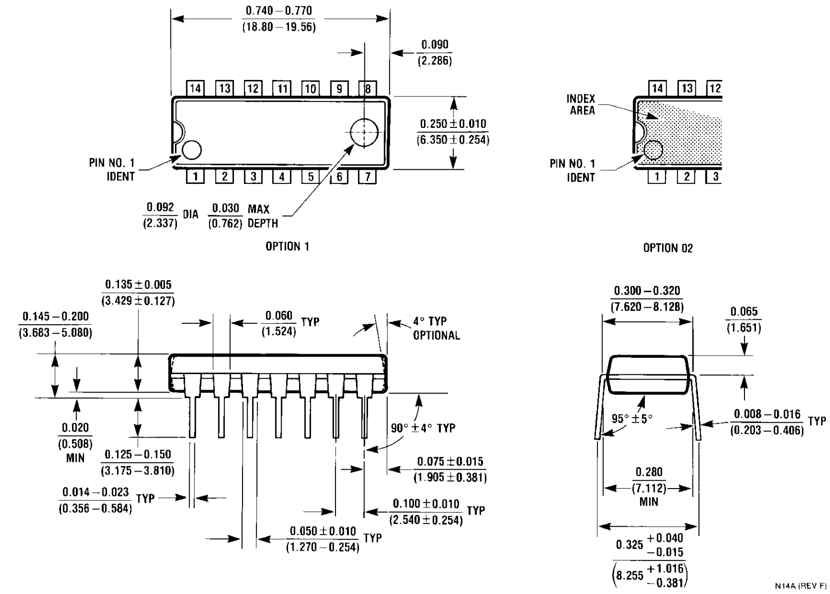
Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		24	ns

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS22M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS22N
NS Package Number N14A

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FAIRCHILD
SEMICONDUCTOR TM

March 1998

DM74LS26
Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

These gates feature high-voltage output ratings (up to 15V) for interfacing with 12V systems. Although the outputs are rated for 15V, the device supply is still rated for 5V.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\ (\text{Min}) - V_{OH}}{N_1\ (I_{OH}) + N_2\ (I_{IH})}$$

$$R_{MIN} = \frac{V_O\ (\text{Max}) - V_{OL}}{I_{OL} - N_3\ (I_{IL})}$$

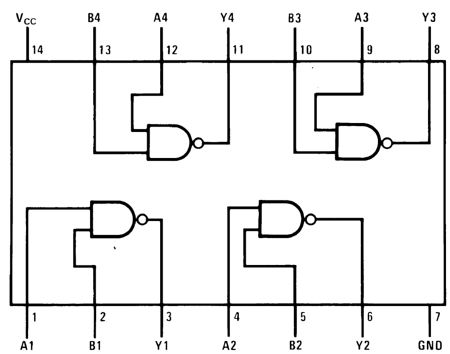
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



DS006358-1

Order Number DM54LS26J, DM74LS26M, DM74LS26N or DM54LS26W
See Package Number J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

DM74LS26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS26			DM74LS26			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min	V_O = 15V			1000	µA
		V_{IL} = Max	V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54			0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 5.5V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	DM54			−0.40	mA
			DM74			−0.36	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

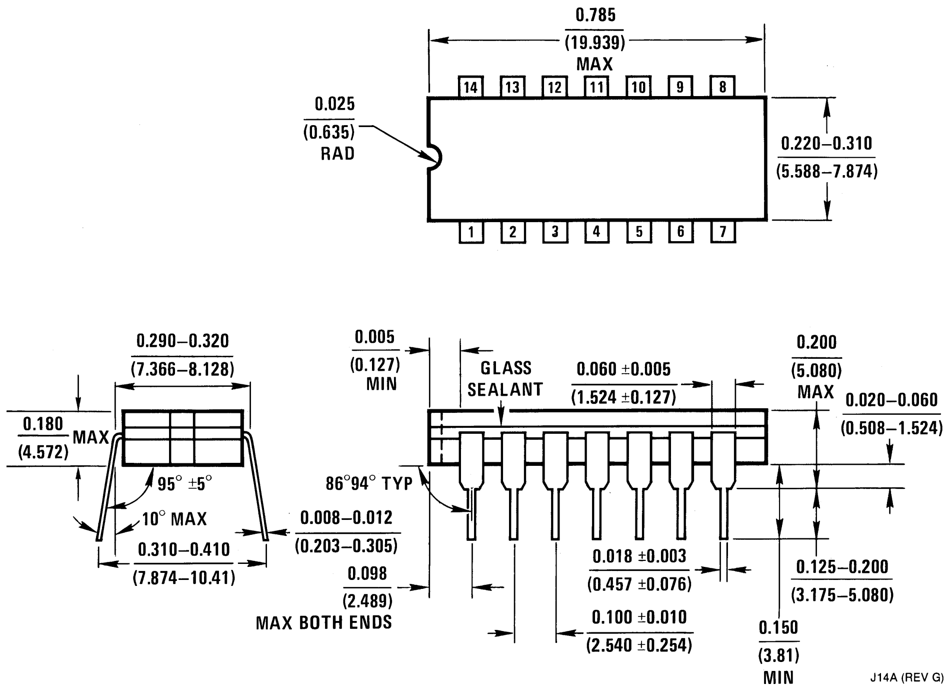
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	DM54		DM74				Units
		R_L = 2 kΩ		R_L = 2 kΩ				
		C_L = 15 pF		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		27		20		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		15		20	ns

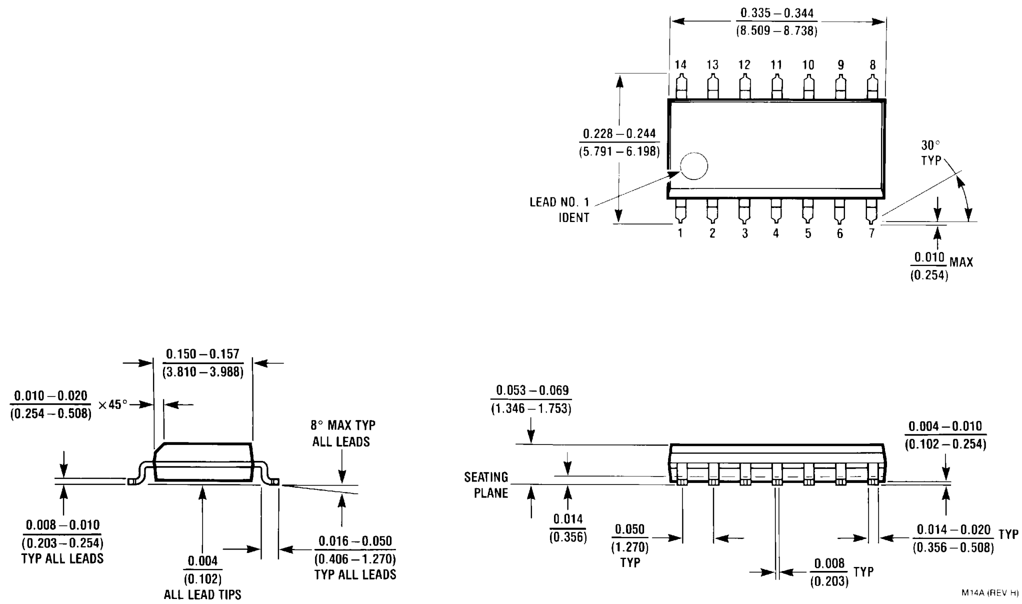
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Physical Dimensions inches (millimeters) unless otherwise noted

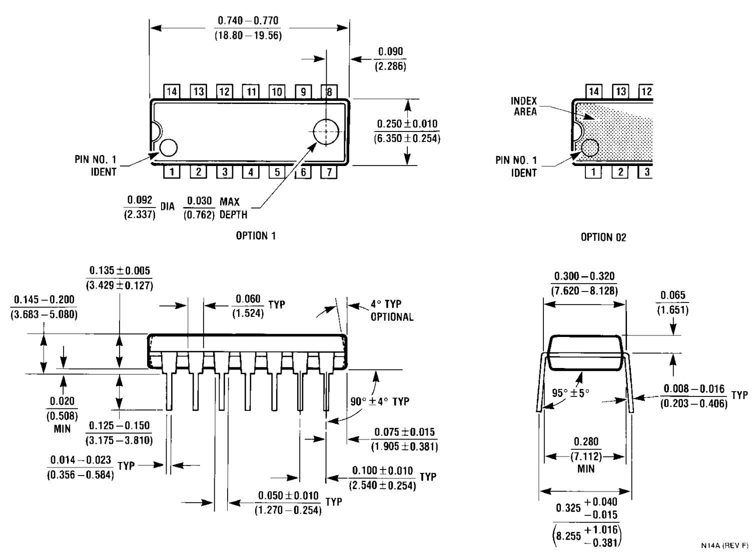


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS26J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

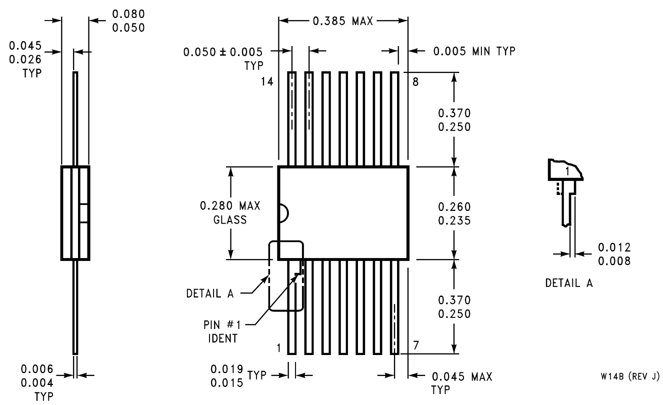


14-Lead Small Outline Molded Package (M)
Order Number DM74LS26M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS26N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS26W
Package Number W14B

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FAIRCHILD SEMICONDUCTOR™

March 1998

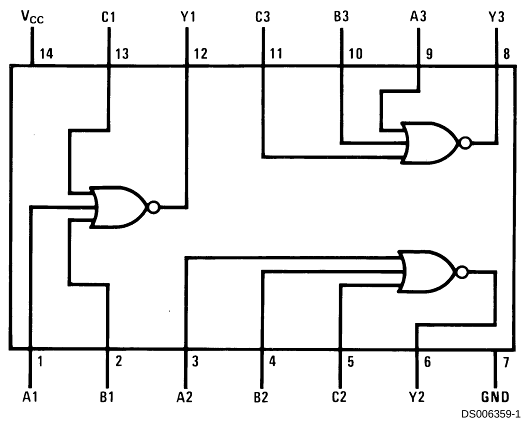
DM74LS27
Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS27J, DM54LS27W, DM54LS27E, DM74LS27M or DM74LS27N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	**B**	**C**	**Y**
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS27			DM74LS27			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.4	6.8	mA

Switching Characteristics

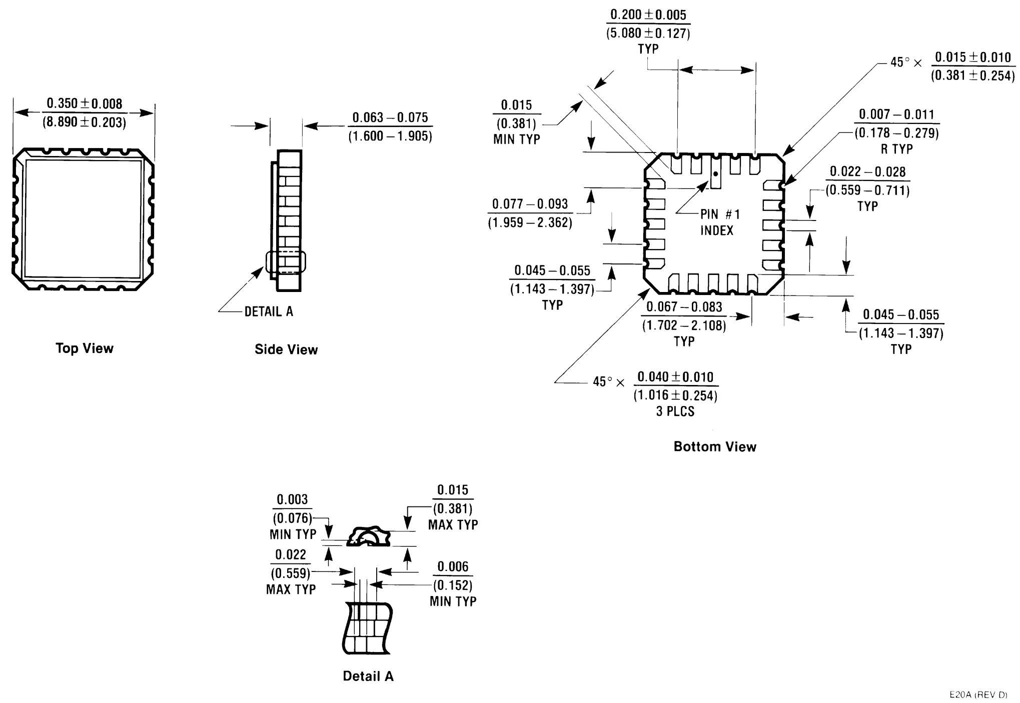
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	DM54		DM74				Units
		R_L = 2 kΩ						
		C_L = 15 pF		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	13	3	13	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	13	3	10	4	15	ns

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

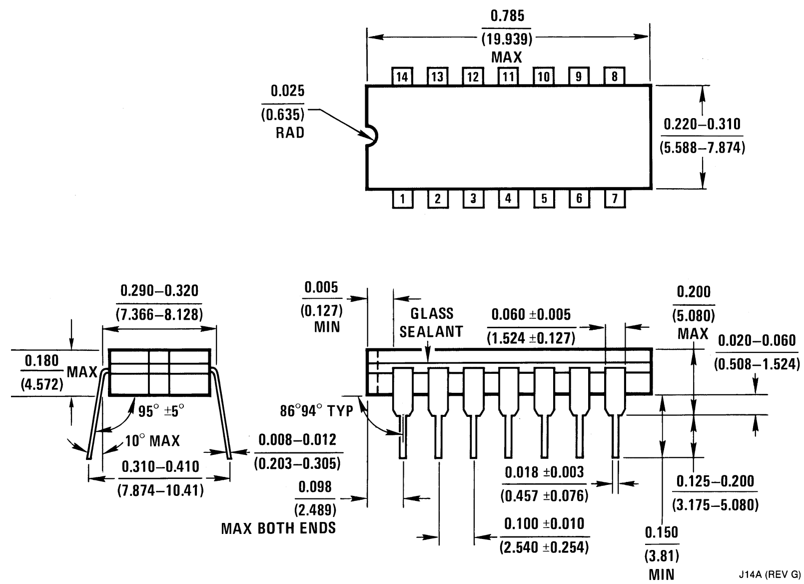
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

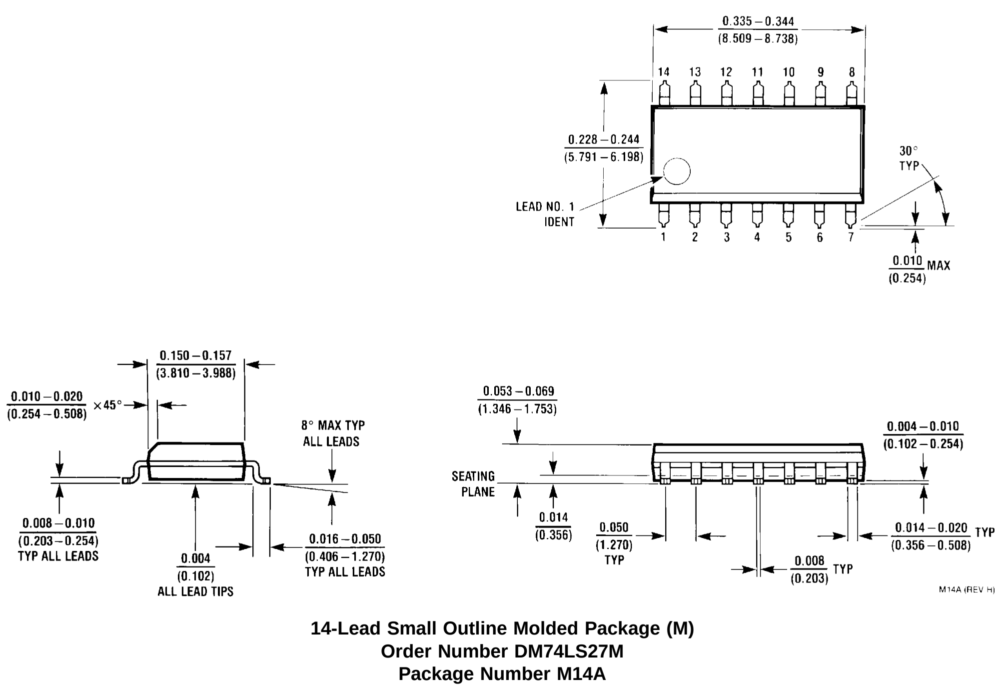


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS27E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

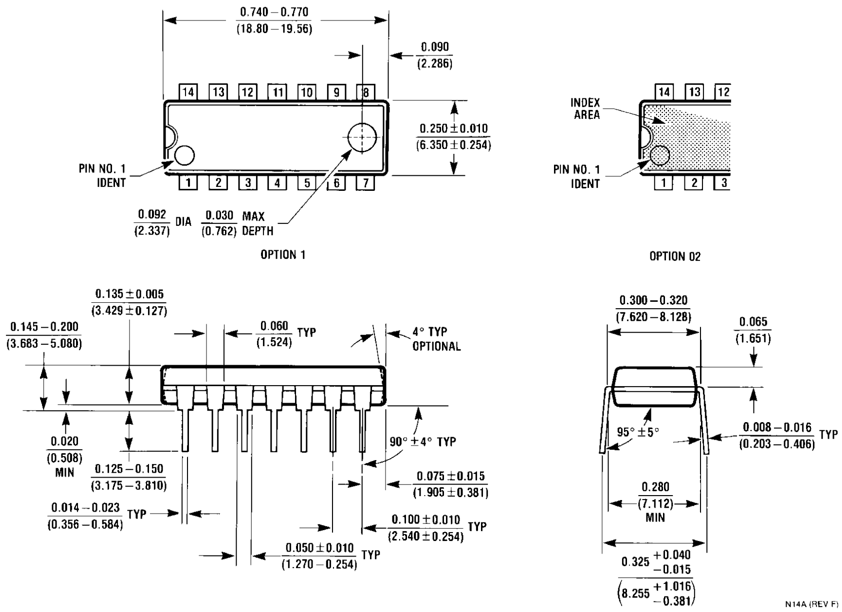


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS27J
Package Number J14A

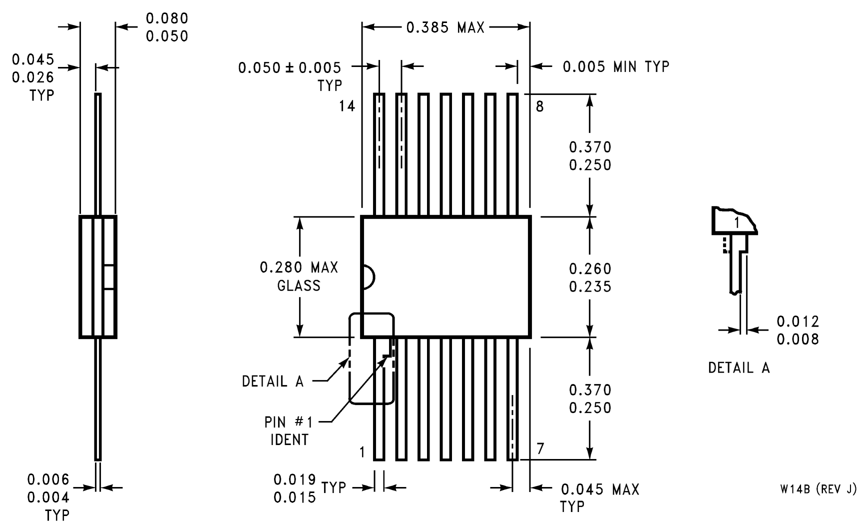


14-Lead Small Outline Molded Package (M)
Order Number DM74LS27M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS27N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS27W
Package Number W14B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR™

April 1998

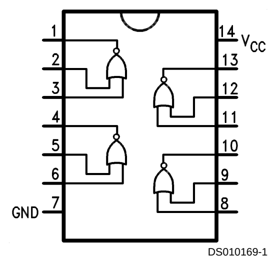
DM74LS28 Quad 2-Input NOR Buffer

General Description

The ’LS28 contains four independent gates each of which perform the logic NOR function.

Connection Diagram

Dual-In-Line Package



Order Number DM74LS28M or DM74LS28N
See Package Number M14A or N14A

Truth Table

$$Y = \overline{A+B}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High logic level
L = Low logic level

 DS010169

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.7	V
I_{OH}	High Level Output Current			−1.2	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 12 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−30		−130	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			13.8	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

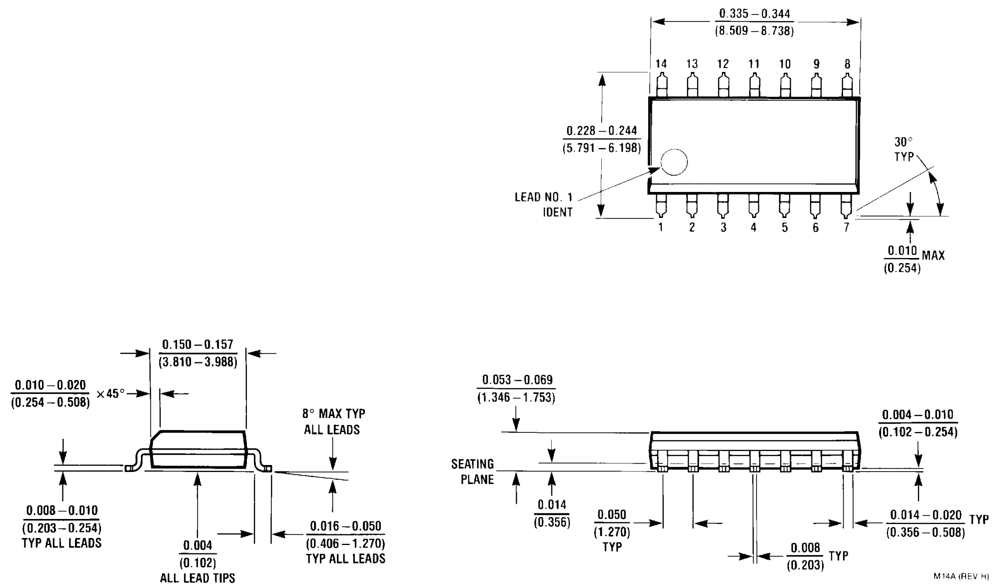
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

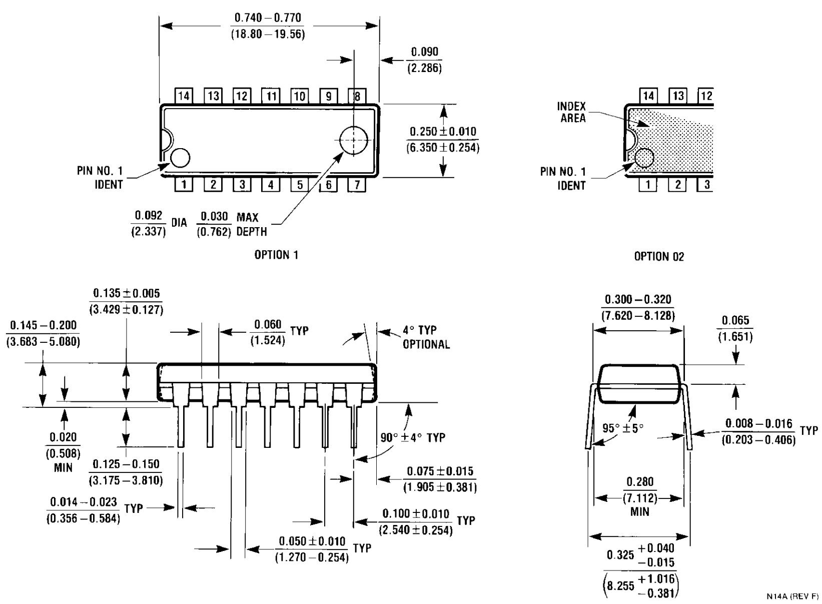
V_{CC} = +5.0V, T_A = +25˚C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		20	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS28M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS28N
Package Number N14A

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March 1998

DM74LS30
8-Input NAND Gate

General Description

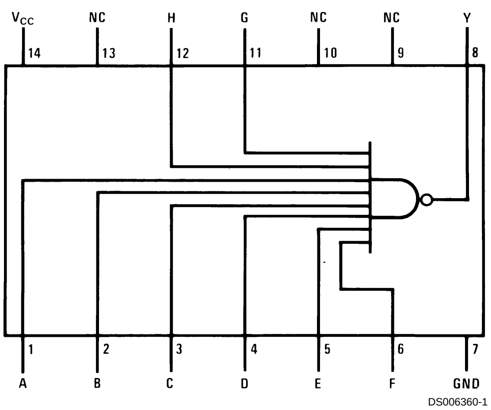
This device contains a single gate which performs the logic NAND function.

Features

- Alternate Military/Aerospace device (54LS30) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS30DMQB, 54LS30FMQB, 54LS30LMQB, DM54LS30J, DM54LS530W, DM74LS30M or DM74LS30N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{ABCDEFGH}$

Inputs	Output
A thru H	**Y**
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS30			DM74LS30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.35	0.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			0.6	1.1	mA

Switching Characteristics

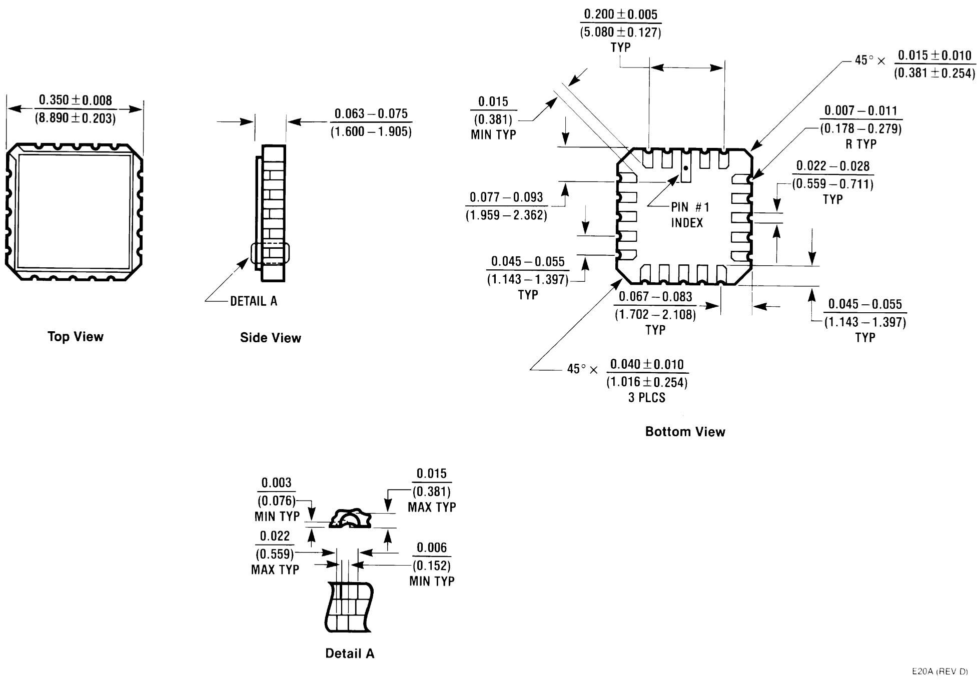
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	12	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	5	20	ns

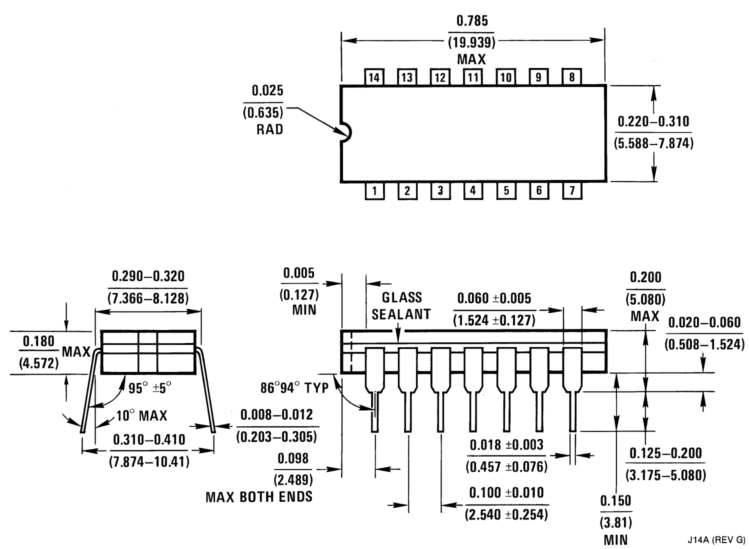
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted

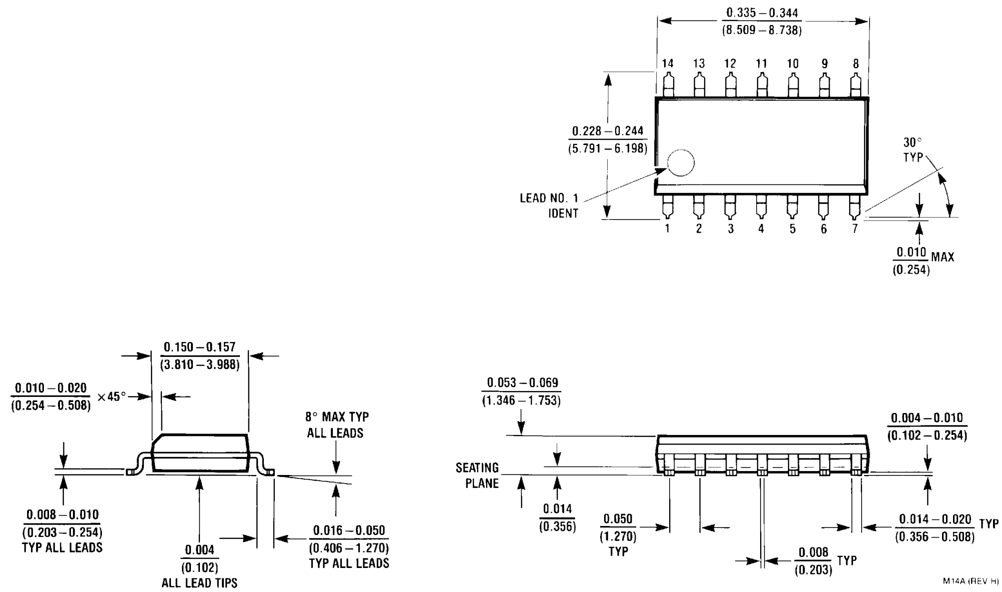


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS30LMQB
Package Number E20A

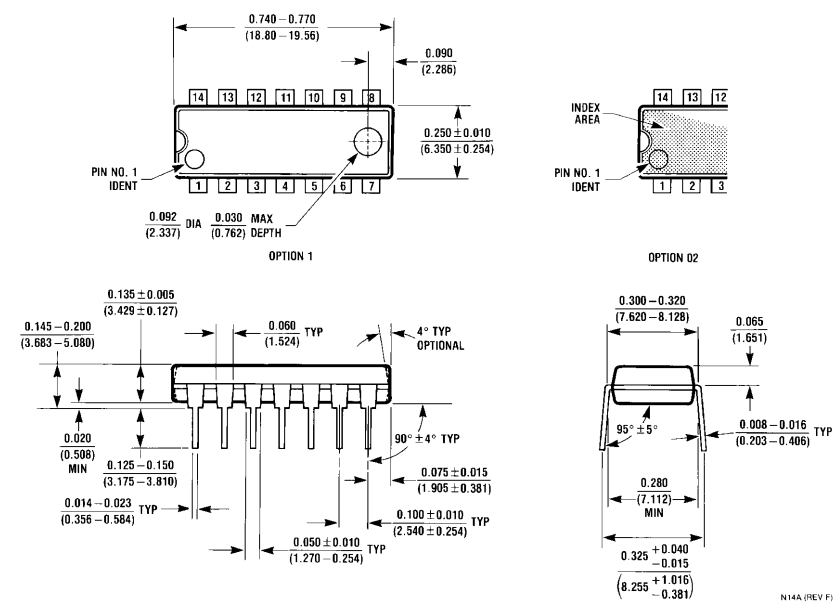


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS30DMQB or DM54LS30J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

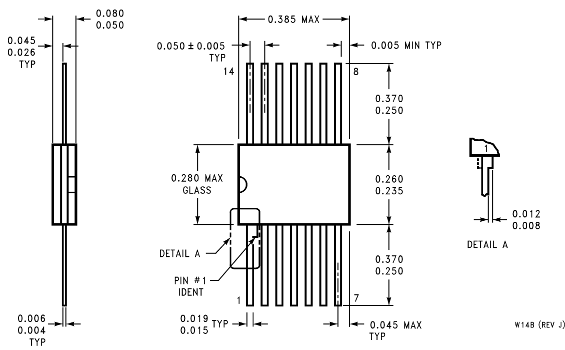


14-Lead Small Outline Molded Package (M)
Order Number DM74LS30M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS30N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS30FMQB or DM54LS30W
Package Number W14B

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DM74LS32
Quad 2-Input OR Gates

General Description

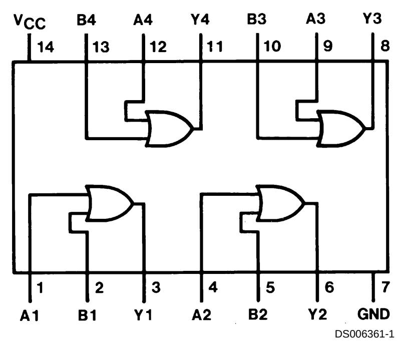
This device contains four independent gates each of which performs the logic OR function.

Features

- Alternate Military/Aerospace device (54LS32) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line-Package



Order Number 54LS32DMQB, 54LS32FMQB, 54LS32LMQB, DM54LS32J, DM54LS32W, DM74LS32M or DM74LS32N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics

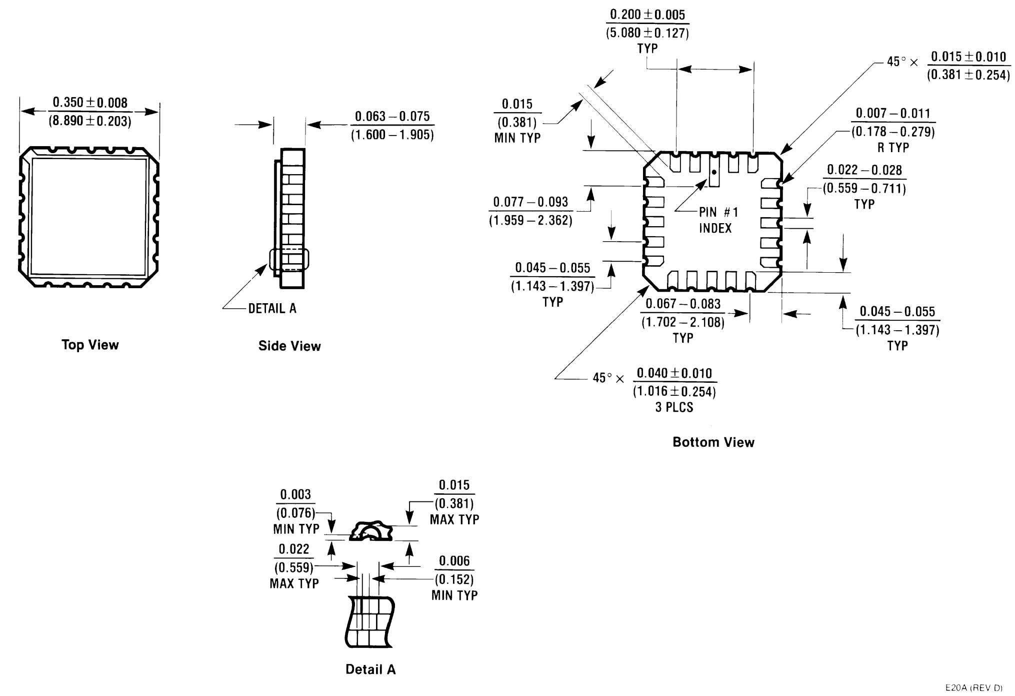
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

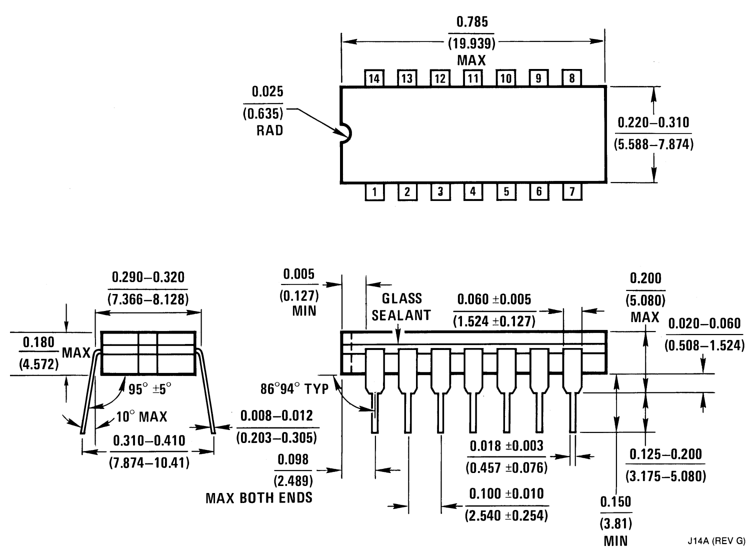
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

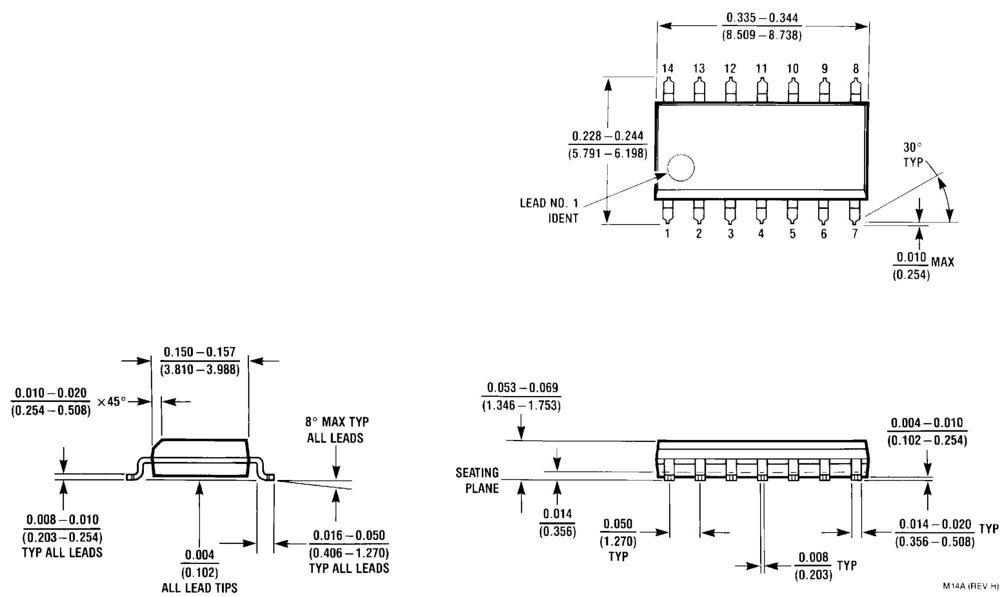
Physical Dimensions inches (millimeters) unless otherwise noted



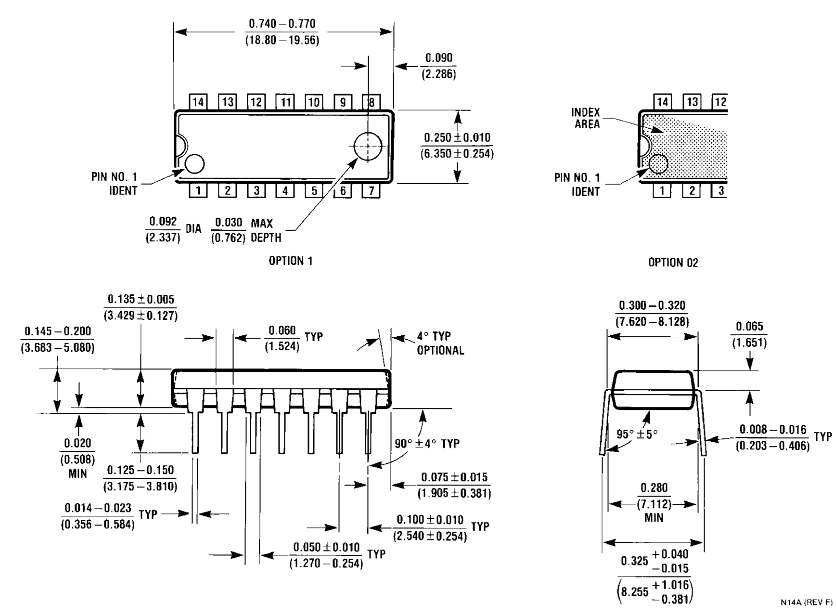
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS32LMQB
Package Number E20A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

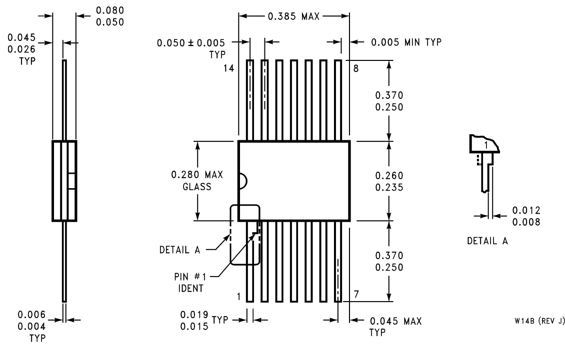


14-Lead Small Outline Molded Package (M)
Order Number DM74LS32M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS32N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS32FMQB or DM54LS32W
Package Number W14B

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FAIRCHILD
SEMICONDUCTOR ™

April 1998

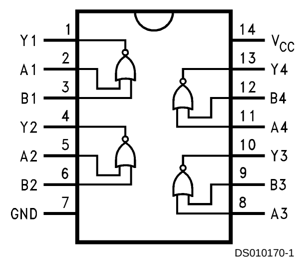
DM74LS33
Quad 2-Input NOR Buffer with Open-Collector Outputs

General Description

This device contains four independent gates each of which perform the logic NOR function. Outputs are open-collector.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS33J, DM54LS33W DM74LS33M or DM74LS33N
See Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS33			DM74LS33			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation .*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				13.8	mA

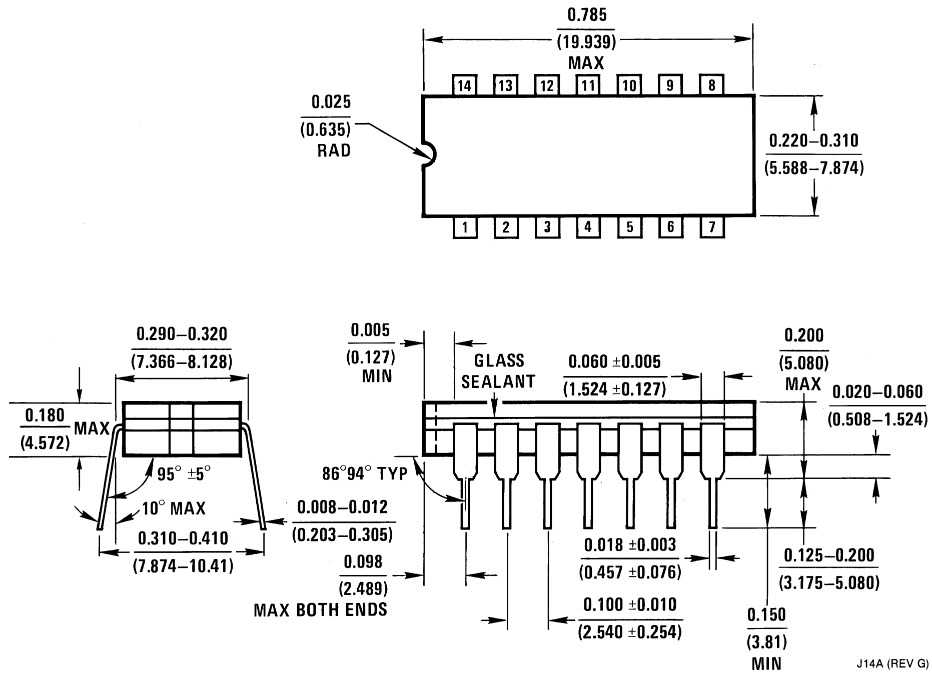
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Switching Characteristics

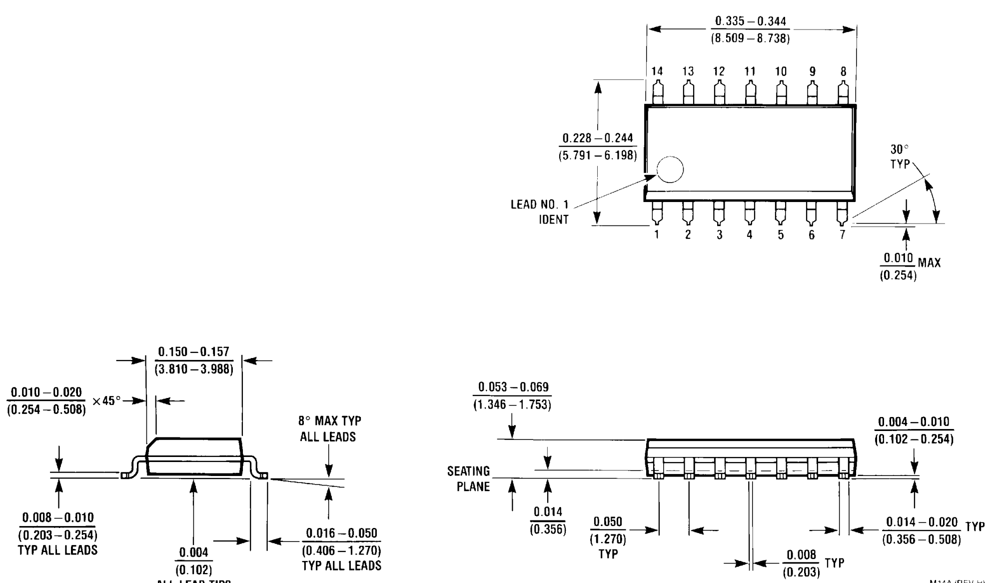
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22	ns

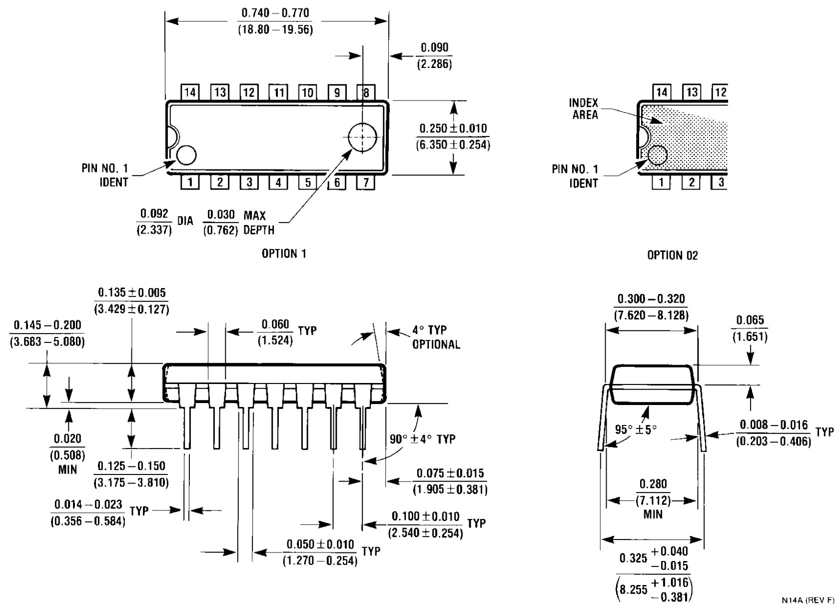
Physical Dimensions inches (millimeters) unless otherwise noted



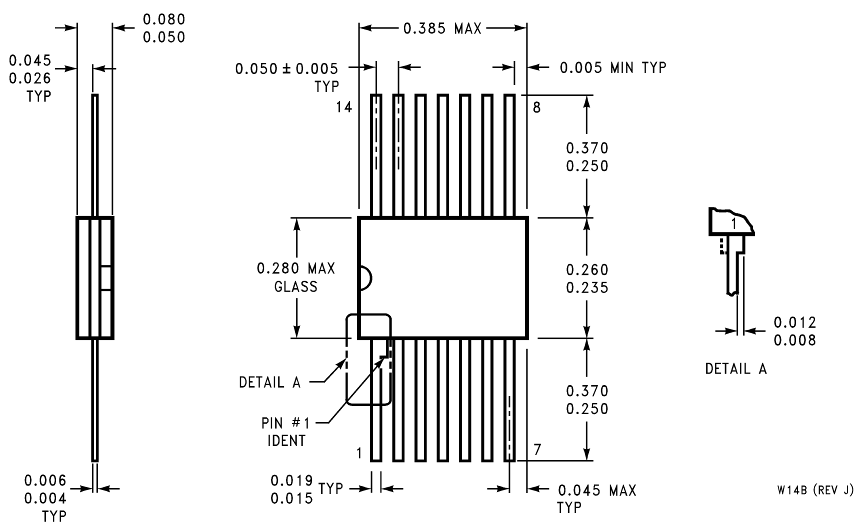
14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS33J
Package Number J14A



14-Lead Small Outline Molded Package (M)
Order Number DM74LS33M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS33N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS33W
Package Number W14B

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National Semiconductor

February 1992

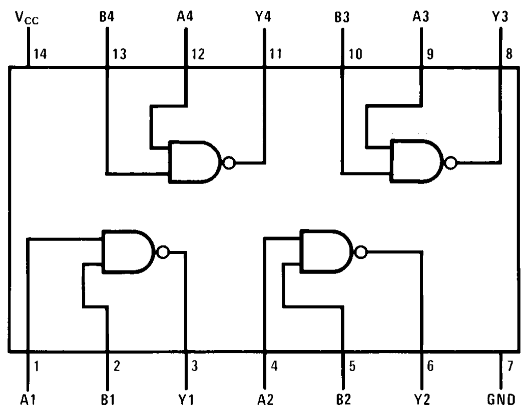
DM74LS37 Quad 2-Input NAND Buffers

General Description

This device contains four independent buffer gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6362–1

Order Number DM74LS37M or DM74LS37N
See NS Package Number M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1.2	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		6	12	mA

Switching Characteristics

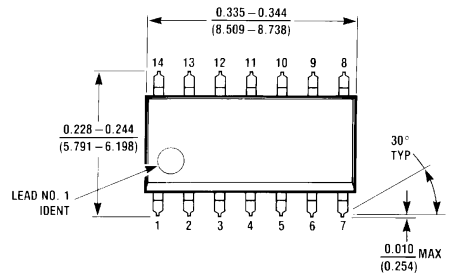
at V_{CC} = 5V and T_A = 25°C

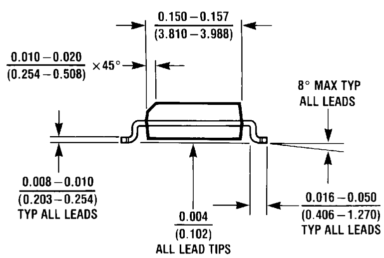
Symbol	Parameter	C_L = 50 pF, R_L = 667Ω		C_L = 150 pF, R_L = 667Ω		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	15	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	21	ns

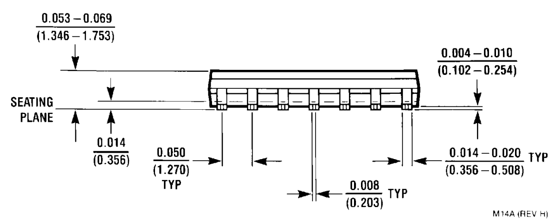
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters)

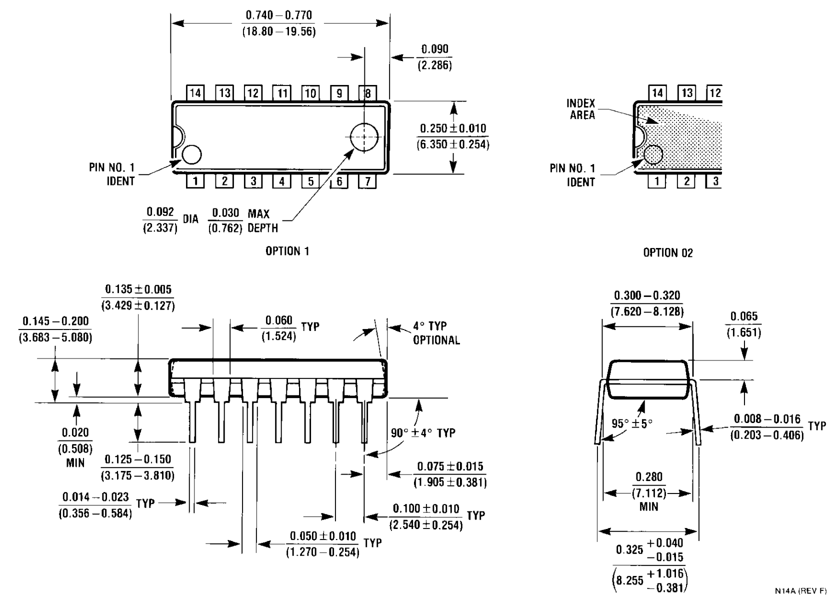






14-Lead Small Outline Molded Package (M)
Order Number DM74LS37M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS37N
NS Package Number N14A

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FAIRCHILD
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March 1998

DM74LS38
Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Features

- Alternate Military/Aerospace device (54LS38) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(\text{Min}) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(\text{Max}) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

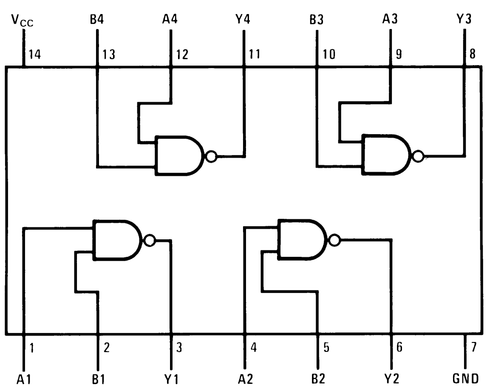
Where: N_1 (I_{OH}) = total maximum output high current for all outputs tied to pull-up resistor

N_2 (I_{IH}) = total maximum input high current for all inputs tied to pull-up resistor

N_3 (I_{IL}) = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



Order Number 54LS38DMQB, 54LS38FMQB, 54LS38LMQB, DM54LS38J, DM74LS38M or DM74LS38N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{AB}$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS38			DM74LS38			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	12	mA

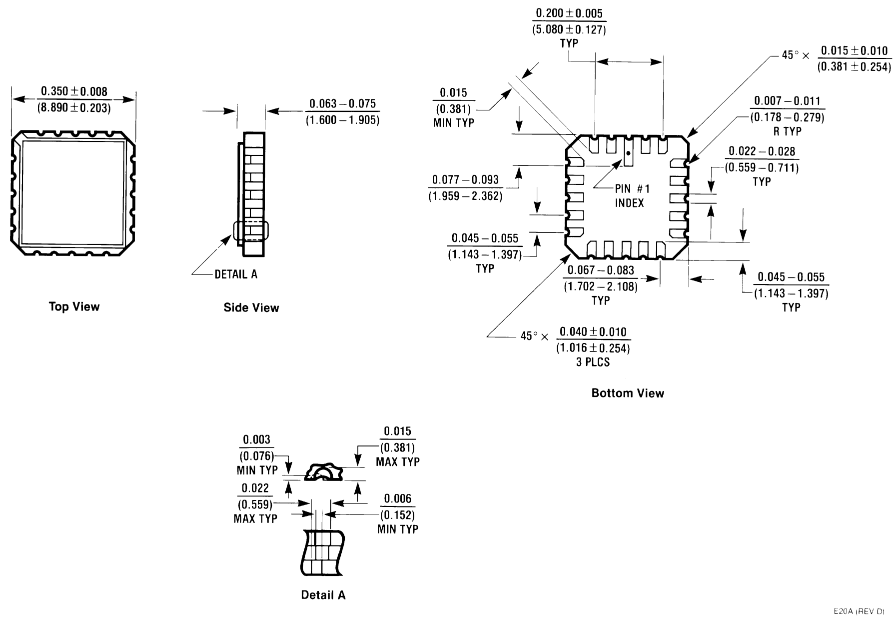
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22		29	ns

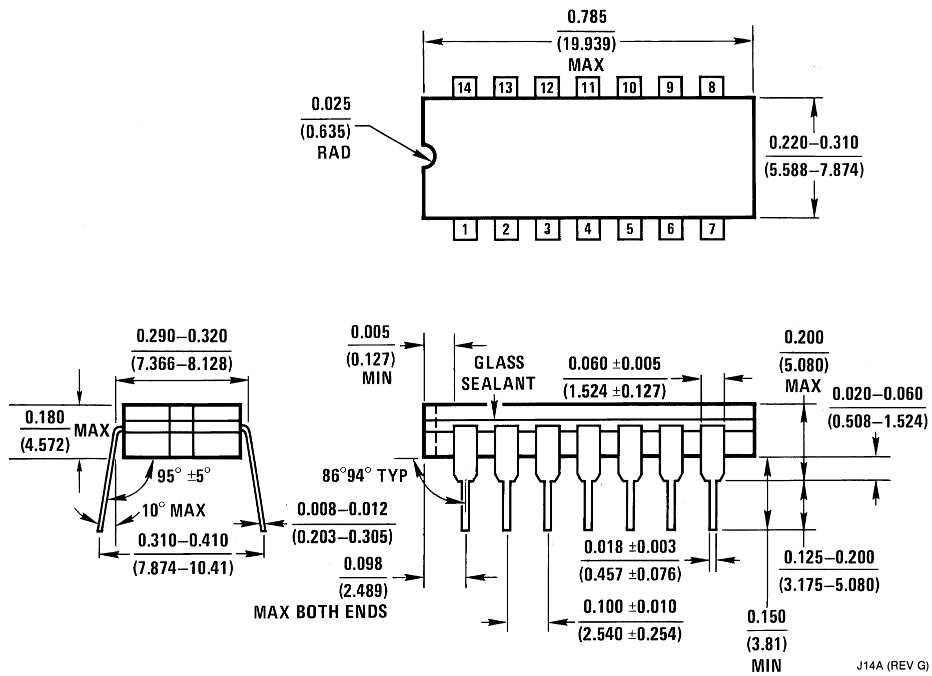
Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Physical Dimensions inches (millimeters) unless otherwise noted



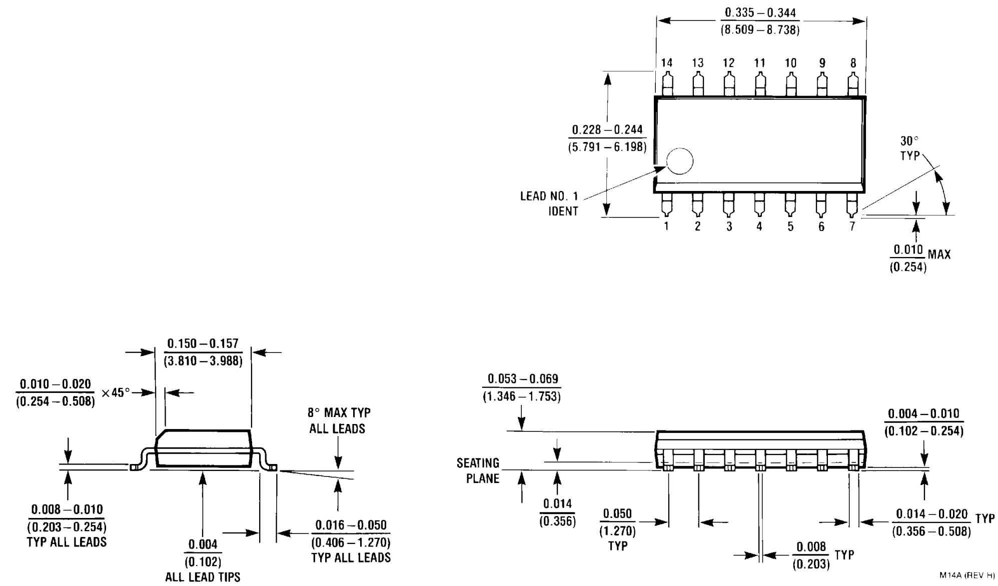
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS38LMQB
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

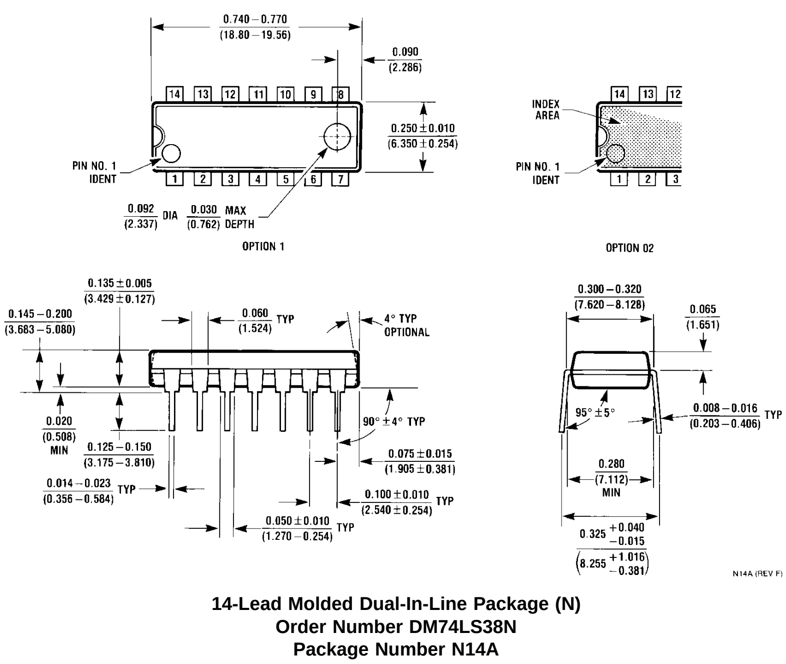


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS538DMQB or DM54LS38J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

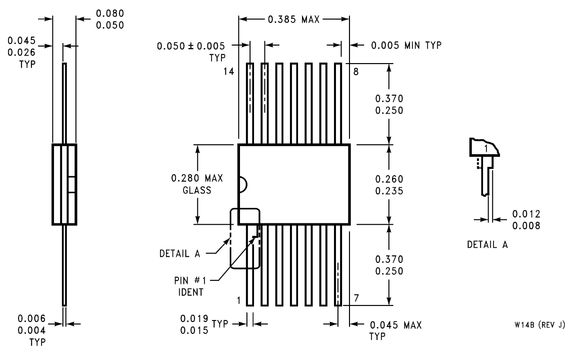


14-Lead Small Outline Molded Package (M)
Order Number DM74LS38M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS38N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (N)
Order Number 54LS538DMQB or DM54LS38W
Package Number W14B

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

February 1992

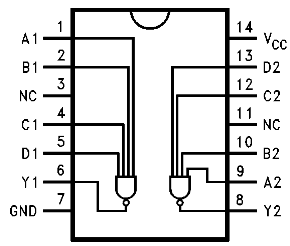
DM74LS40
Dual 4-Input NAND Buffer

General Description

This device contains two independent gates each of which perform the logic NAND function.

Connection Diagrams

Dual-In-Line Package



TL/F/10171–1

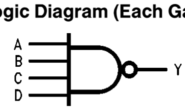
Order Number DM74LS40M or DM74LS40N
See NS Package Number M14A or N14A

Function Table

(Each Gate)

Inputs				Outputs
A	**B**	**C**	**D**	**Y**
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H

Logic Diagram (Each Gate)



TL/F/10171–2

Positive Logic

$Y = \overline{A \bullet B \bullet C \bullet D}$ or $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS40			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−1.2	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 12 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−130	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND			1.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = OPEN			6.0	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

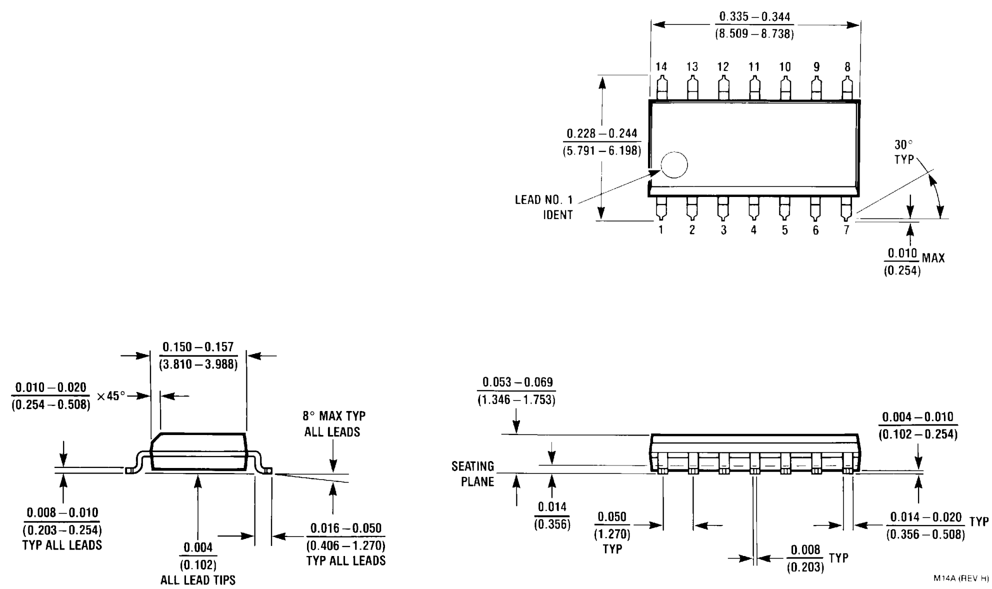
Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

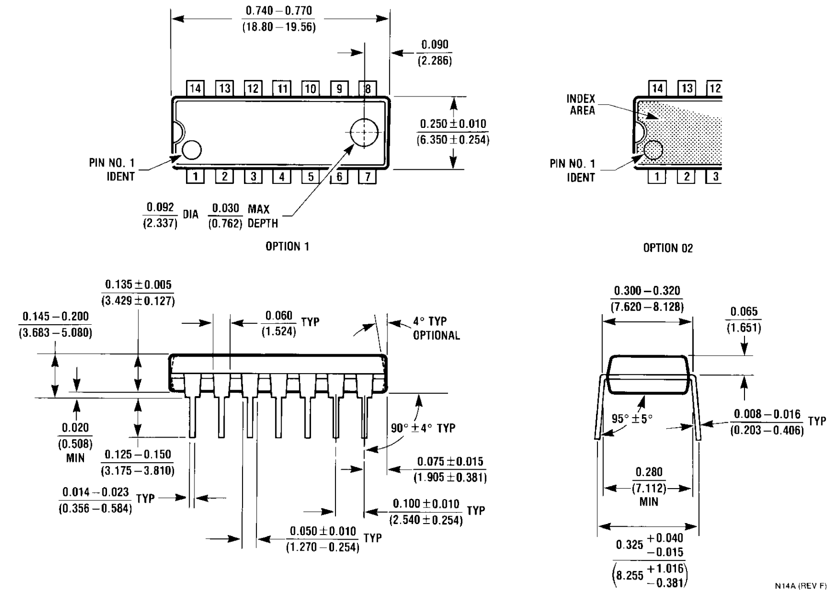
Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		24	ns

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS40M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS40N
NS Package Number N14A

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National Semiconductor

June 1989

54LS42/DM54LS42/DM74LS42 BCD/Decimal Decoders

General Description

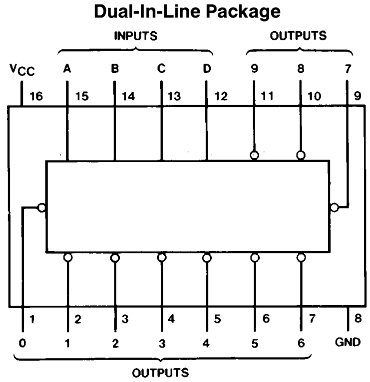
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

Features

- Diode clamped inputs
- Also for applications as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Alternate Military/Aerospace device (54LS42) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6365–1

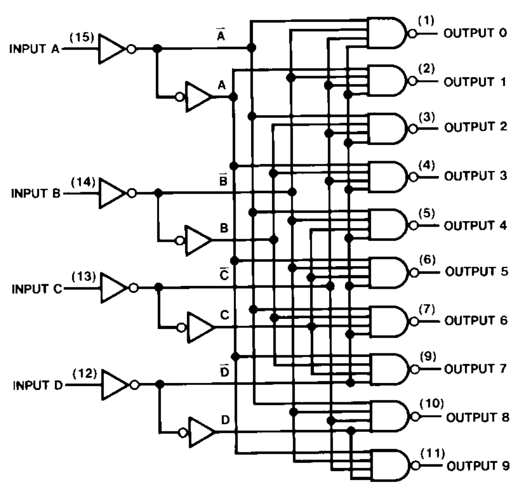
Order Number 54LS42DMQB, 54LS42FMQB, DM54LS42J, DM54LS42W, DM74LS42M or DM74LS42N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Logic Diagram



TL/F/6365–2

 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS42			DM74LS42			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

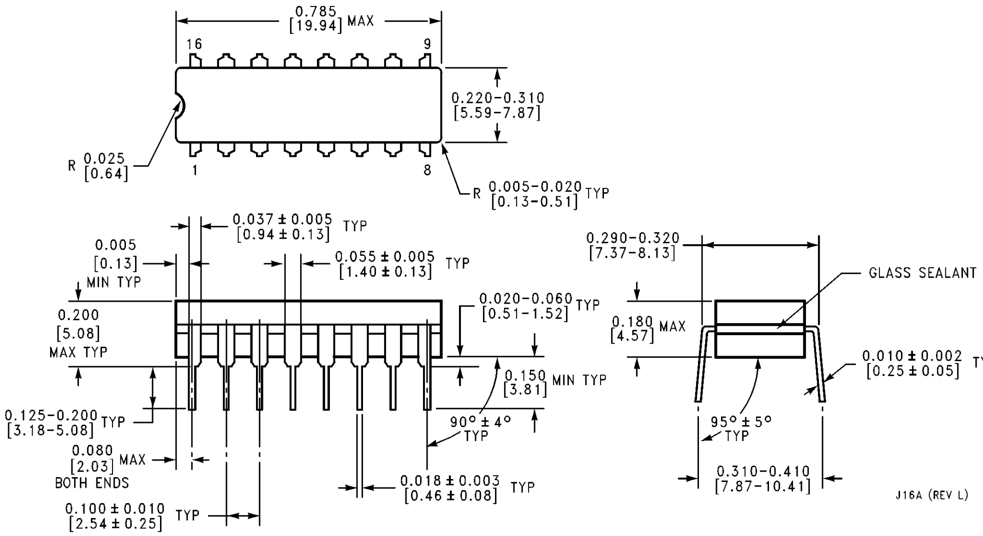
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

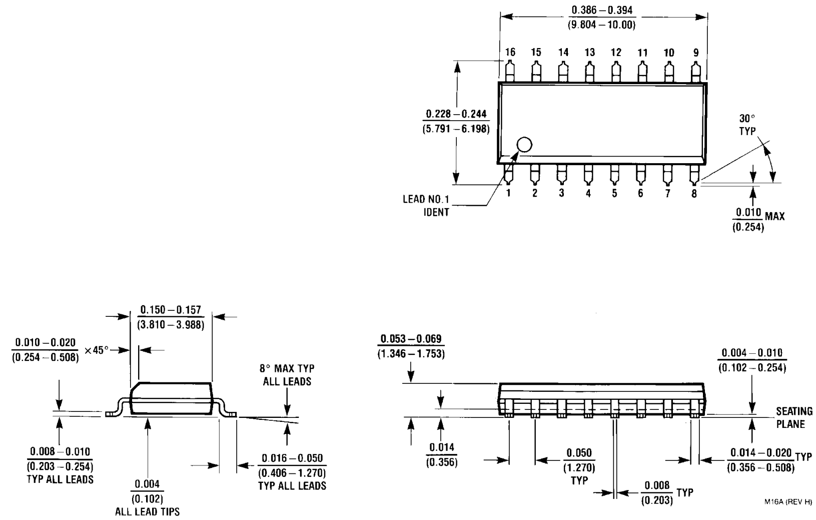
Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns

Physical Dimensions inches (millimeters)

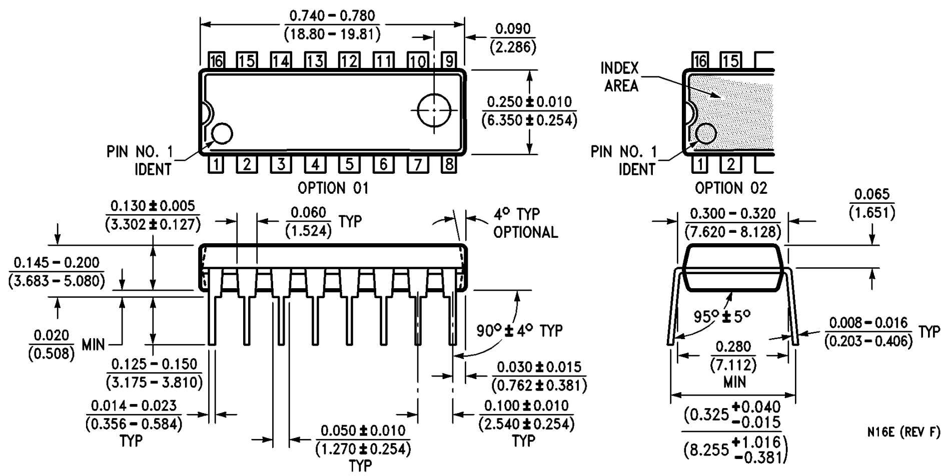


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS42DMQB or DM54LS42J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

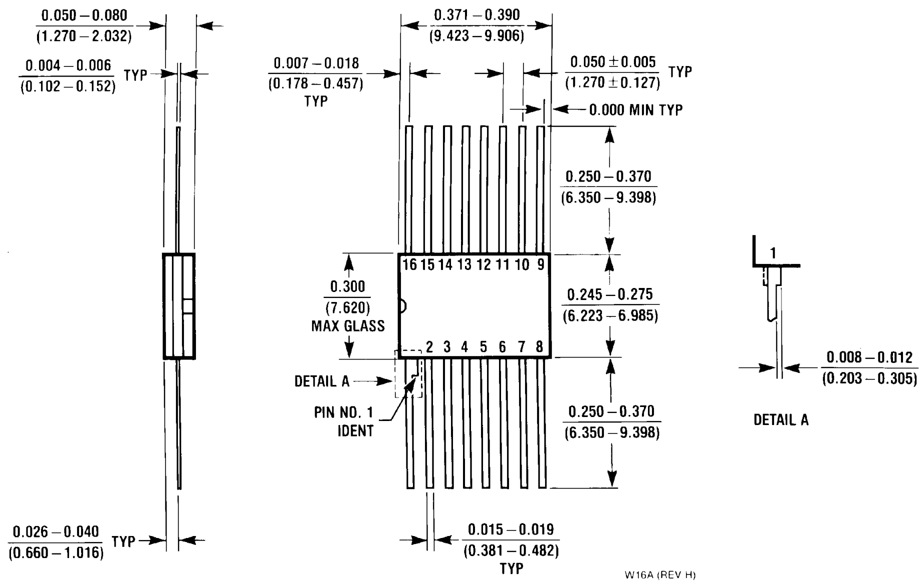


16-Lead Small Outline Molded Package (M)
Order Number DM74LS42M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS42N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS42FMQB or DM54LS42W
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR ™

March 1998

DM74LS47
BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

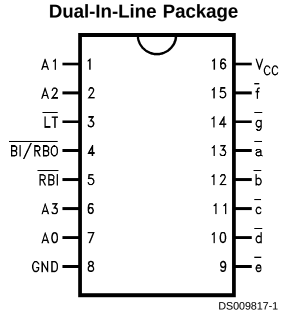
The 'LS47 accepts four lines of BCD (8421) input data, generates their complements internally and decodes the data with seven AND/OR gates having open-collector outputs to drive indicator segments directly. Each segment output is guaranteed to sink 24 mA in the ON (LOW) state and withstand 15V in the OFF (HIGH) state with a maximum leakage current of 250 µA. Auxiliary inputs provided blanking, lamp test and cascadable zero-suppression functions.

Features

- Open-collector outputs
- Drive indicator segments directly
- Cascadable zero-suppression capability
- Lamp test input

Connection Diagram

Dual-In-Line Package



Order Number DM54LS47J, DM54LS47W, DM74LS47M or DM74LS47N
See Package Number J16A, M16A, N16E or W16A

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or
	Ripple Blanking Output (Active LOW)
$\overline{a}$ – $\overline{g}$	*Segment Outputs (Active LOW)

Note 1: *OC—Open Collector

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS47			DM74LS47			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current $\overline{a} - \overline{g}$ @ 15V = V_{OH} (Note 3)			−50			−250	µA
I_{OH}	High Level Output Current $\overline{BI}$ /$\overline{RBO}$						−50	µA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: OFF state at $\overline{a}$–$\overline{g}$.

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, $\overline{BI}$ /$\overline{RBO}$	DM54	2.4			V
			DM74	2.7	3.4		
I_{OFF}	Output High Current Segment Outputs	V_{CC} = 5.5V, V_O = 15V $\overline{a} - \overline{g}$				250	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, $\overline{a} - \overline{g}$	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 3.2 mA, $\overline{BI}$ /$\overline{RBO}$	DM74			0.5	
		I_{OL} = 12 mA, $\overline{a} - \overline{g}$	DM74		0.25	0.4	
		I_{OL} = 1.6 mA, $\overline{BI}$ /$\overline{RBO}$	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			100	µA
		V_{CC} = Max, V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5) , I_{OS} at $\overline{BI/RBO}$	DM54	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at $V_{CC} = +5.0V$, $T_A = +25^{\circ}C$

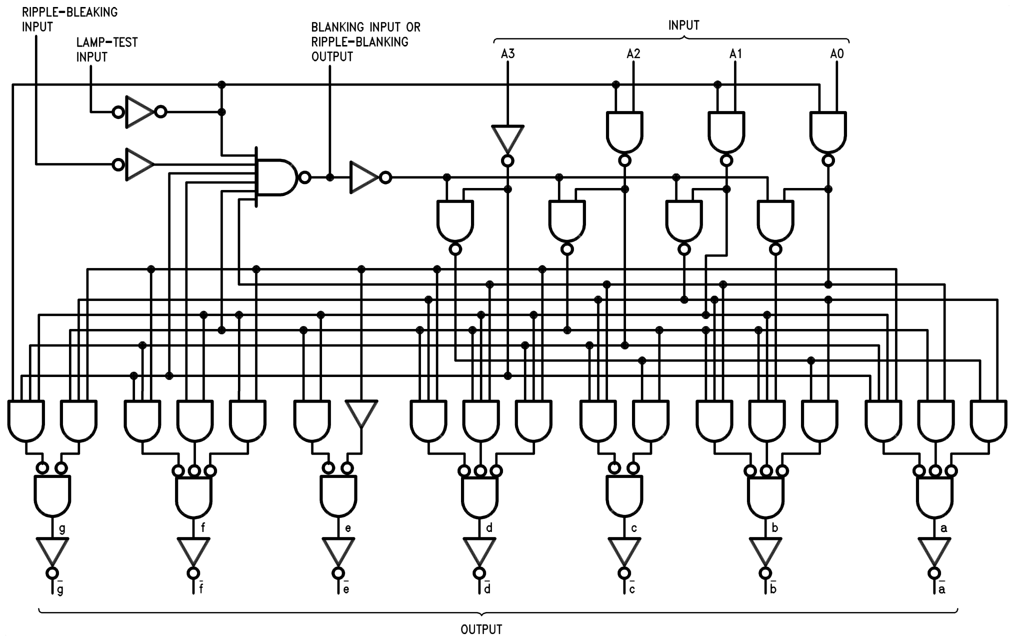
Symbol	Parameter	Conditions	$R_L = 665\Omega$, $C_L = 15$ pF Min	$R_L = 665\Omega$, $C_L = 15$ pF Max	Units
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	An to $\overline{a}$ – $\overline{g}$			100	
t_{PLH}	Propagation Delay			100	ns
t_{PHL}	$\overline{RBI}$ to $\overline{a}$ – $\overline{g}$ (Note 6)			100	

Note 6: $\overline{LT}$ = HIGH, A0–A3 = LOW

Functional Description

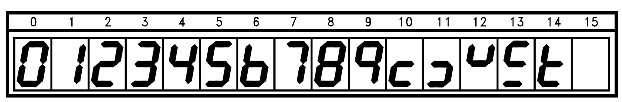
The 'LS47 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration. If the input data is decimal zero, a LOW signal applied to the $\overline{RBI}$ blanks the display and causes a multidigit display. For example, by grounding the $\overline{RBI}$ of the highest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next lowest order decoder, etc., leading zeros will be suppressed. Similarly, by grounding $\overline{RBI}$ of the lowest order decoder and connecting its $\overline{BI/RBO}$ to $\overline{RBI}$ of the next highest order decoder, etc., trailing zeros will be suppressed. Leading and trailing zeros can be suppressed simultaneously by using external gates, i.e.: by driving $\overline{RBI}$ of a intermediate decoder from an OR gate whose inputs are $\overline{BI/RBO}$ of the next highest and lowest order decoders. $\overline{BI/RBO}$ also serves as an unconditional blanking input. The internal NAND gate that generates the $\overline{RBO}$ signal has a resistive pull-up, as opposed to a totem pole, and thus $\overline{BI/RBO}$ can be forced LOW by external means, using wired-collector logic. A LOW signal thus applied to $\overline{BI/RBO}$ turns off all segment outputs. This blanking feature can be used to control display intensity by varying the duty cycle of the blanking signal. A LOW signal applied to $\overline{LT}$ turns on all segment outputs, provided that $\overline{BI/RBO}$ is not forced LOW.

Logic Diagram



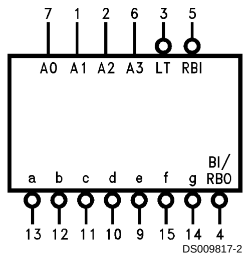
DS009817-3

Numerical Designations—Resultant Displays



DS009817-4

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	(Note 7)
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	(Note 7)
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(Note 8)
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(Note 9)
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(Note 10)

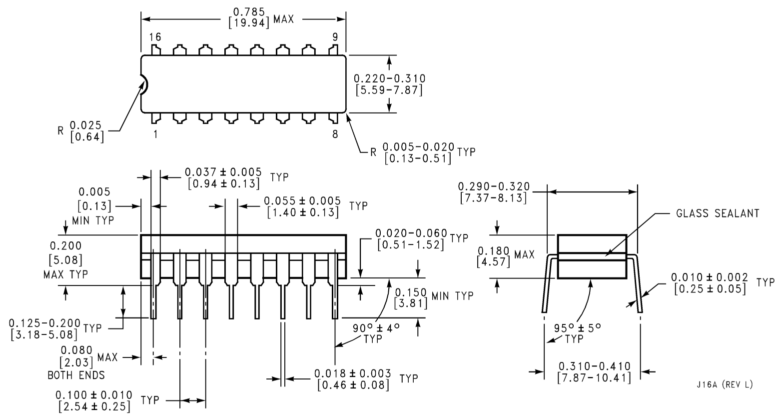
Note 7: $\overline{BI/RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking or a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 8: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a HIGH level regardless of the state of any other input condition.

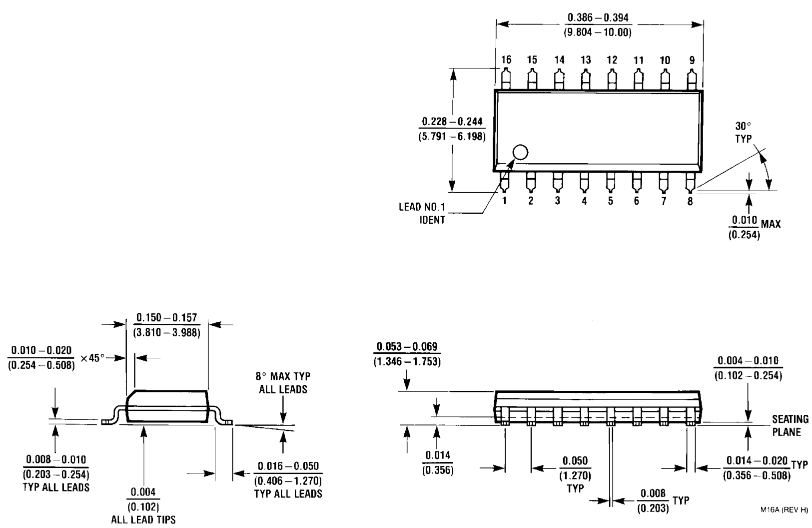
Note 9: When ripple-blanking input ($\overline{RBI}$) and inputs A0, A1, A2 and A3 are LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 10: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

Physical Dimensions inches (millimeters) unless otherwise noted

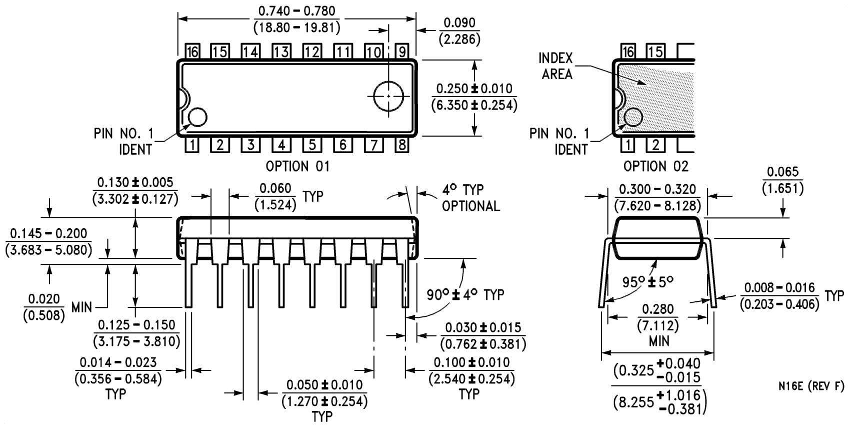


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS47J
Package Number J16A

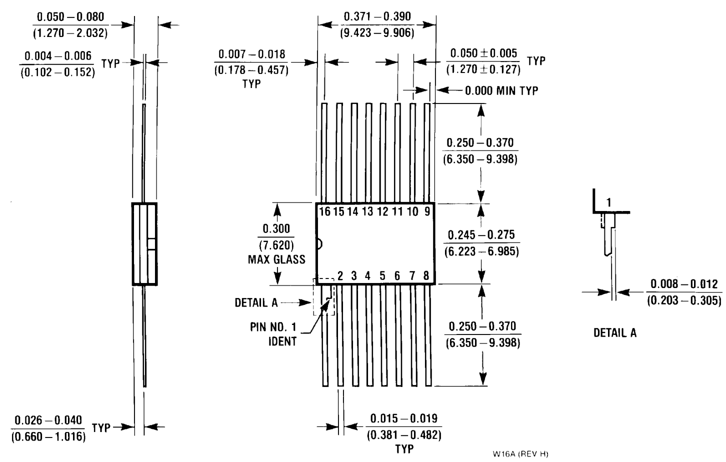


16-Lead Small Outline Molded Package (M)
Order Number DM74LS47M
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS47N
Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS47W
Package Number W16A

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National Semiconductor

January 1992

DM74LS48 BCD to 7-Segment Decoder

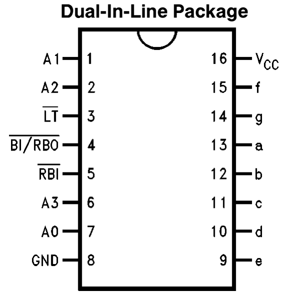
General Description

The 'LS48 translates four lines of BCD (8421) input data into the 7-segment numeral code and provides seven corresponding outputs having pull-up resistors, as opposed to totem pole pull-ups. These outputs can serve as logic signals, with a HIGH output corresponding to a lighted lamp segment, or can provide a 1.3 mA base current to npn lamp driver transistors. Auxiliary inputs provide lamp test, blanking and cascadable zero-suppression functions.

The 'LS48 decodes the input data in the pattern indicated in the Truth Table and the segment identification illustration.

Connection Diagram

Dual-In-Line Package



TL/F/10172–1

Order Number DM74LS48M or DM74LS48N
See NS Package Number M16A or N16E

DM74LS48 BCD to 7-Segment Decoder

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS48			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−50	μA
I_{OL}	Low Level Output Current			6.0	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} Min, I_{OH} = Max, V_{IL} = Max	2.4			V
I_{OFF}	Output High Current Segment Outputs	V_{CC} = Min, V_O = 0.85V	−1.3			mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 2.0 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_O = 0V at $\overline{BI}/\overline{RBO}$ (Note 2)	−0.3		−2	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_{IN} = 4.5V			38	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

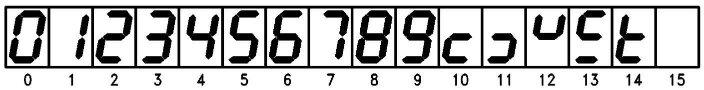
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time A_n to a−g		100 100	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{RBI}$ to a−f		100 100	ns

Note: $\overline{LT}$ = HIGH, A_0–A_3 = HIGH.

Numerical Designations—Resultant Displays



TL/F/10172–4

Truth Table

Decimal Or Function	Inputs							Outputs						
	$\overline{LT}$	$\overline{RBI}$	A_3	A_2	A_1	A_0	$\overline{BI}/\overline{RBO}$	a	b	c	d	e	f	g
0 (Note 1)	H	H	L	L	L	L	H	H	H	H	H	H	H	L
1 (Note 1)	H	X	L	L	L	H	H	L	H	H	L	L	L	L
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L
$\overline{BI}$ (Note 2)	X	X	X	X	X	X	L	L	L	L	L	L	L	L
$\overline{RBI}$ (Note 3)	H	L	L	L	L	L	L	L	L	L	L	L	L	L
$\overline{LT}$ (Note 4)	L	X	X	X	X	X	H	H	H	H	H	H	H	H

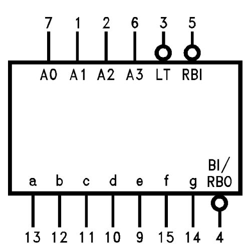
Note 1: $\overline{BI}/\overline{RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

Note 3: When ripple-blanking input ($\overline{RBI}$) and inputs A_0, A_1, A_2, and A_3 are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a LOW level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

Note 4: When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

Logic Symbol

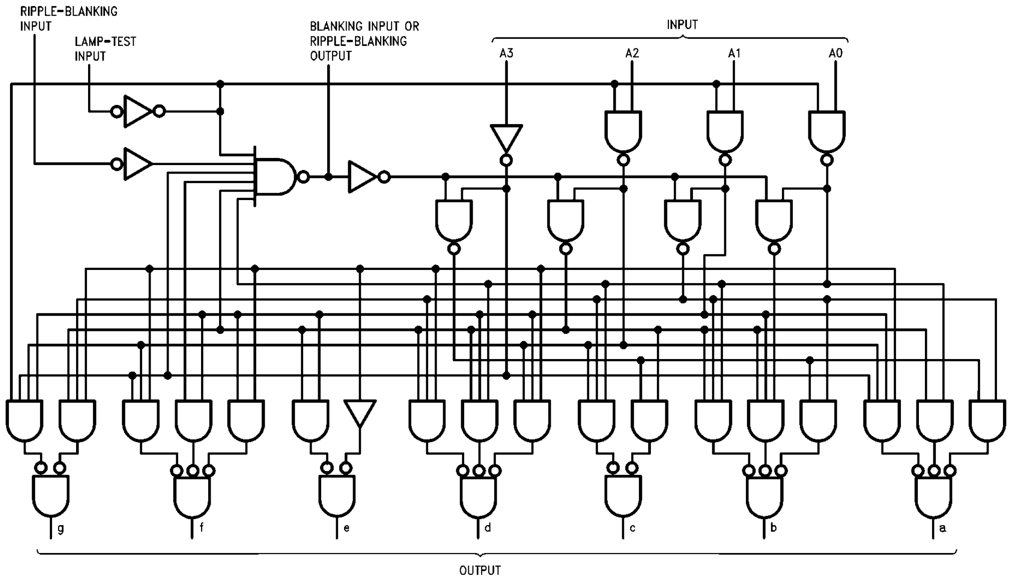


TL/F/10172–2

V_{CC} = Pin 16

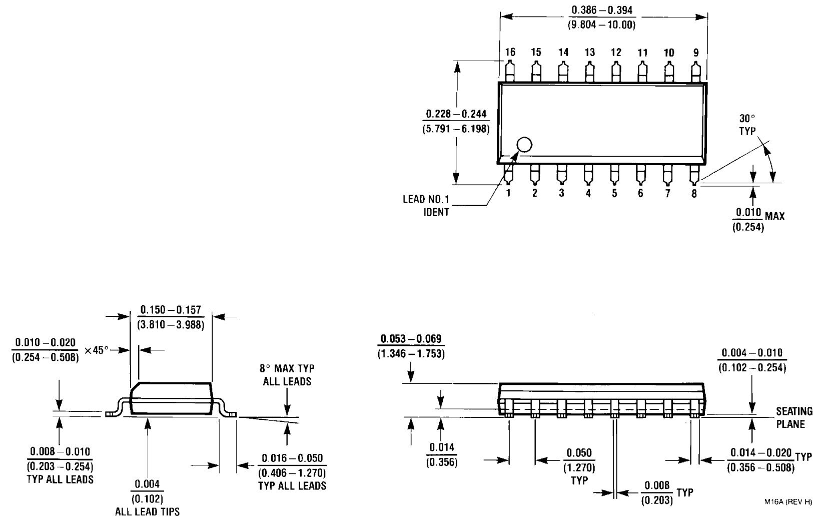
GND = Pin 8

Logic Diagram



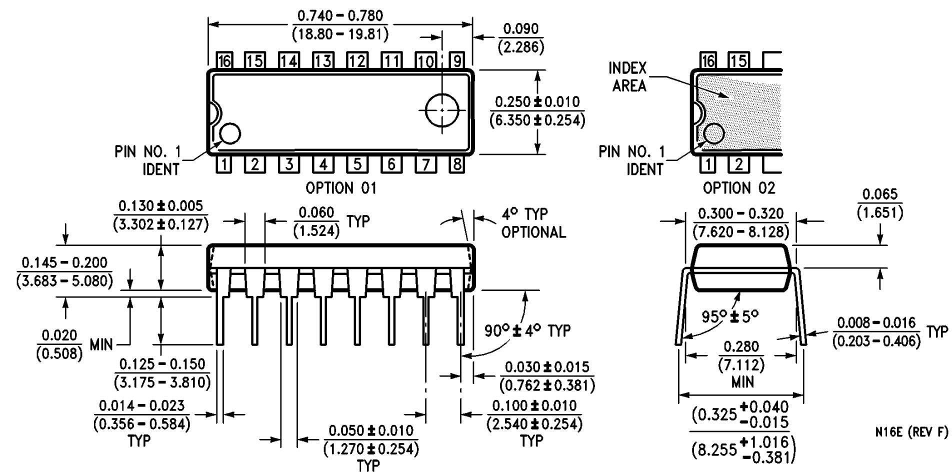
TL/F/10172-3

Physical Dimensions inches (millimeters)



16-Lead Small Outline Molded Package (M)
Order Number DM74LS48M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS48N
NS Package Number N16E

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FAIRCHILD SEMICONDUCTOR TM

March 1998

DM74LS51
Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

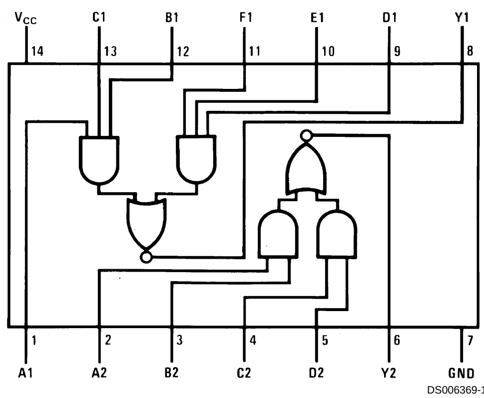
General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

Each package contains one 2-wide 2-input and one 2-wide 3-input AND-OR-INVERT gates.

Connection Diagram

Dual-In-Line Package



Order Number 54LS51DMQB, 54LS51FMQB, 54LS51LMQB, DM74LS51M or DM74LS51N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$$Y1 = \overline{(A1)\ (B1)\ (C1) + (D1)\ (E1)\ (F1)}$$

Inputs						Output
A1	**B1**	**C1**	**D1**	**E1**	**F1**	**Y1**
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{((A2)\ (B2) + (C2)\ (D2))}$$

Inputs				Output
A2	**B2**	**C2**	**D2**	**Y2**
H	H	X	X	L
X	X	H	H	L
Other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

 DS006369

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	54LS51			DM74LS51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V (54LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	54LS			−0.40	mA
			DM74			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.4	2.8	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

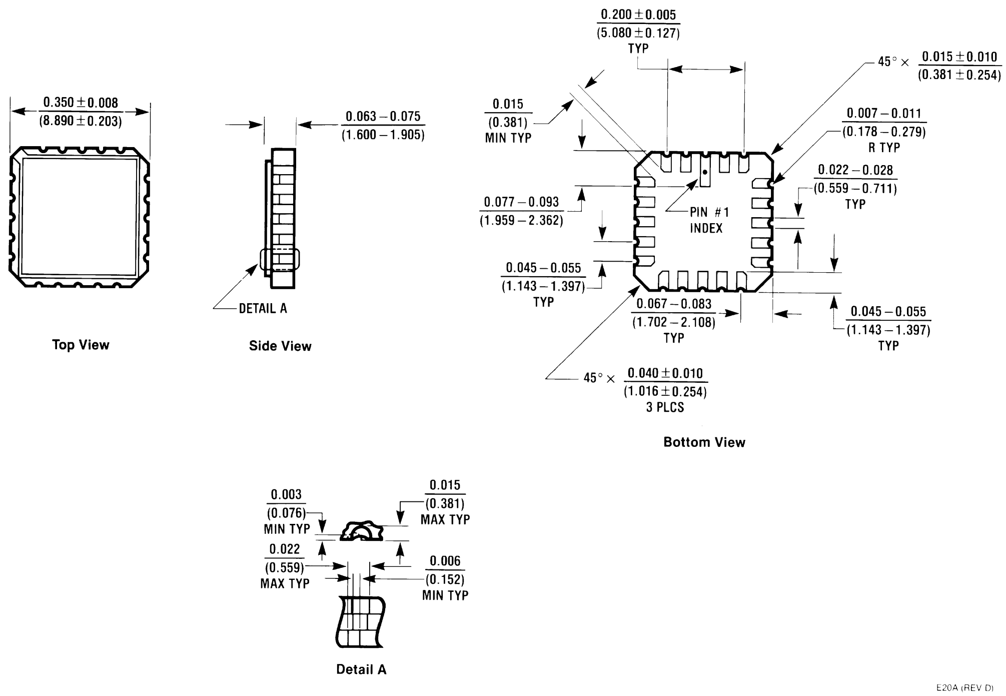
Symbol	Parameter	54LS51 C_L = 15 pF, R_L = 2 kΩ		DM74LS51 C_L = 50 pF, R_L = 2 kΩ		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		20	4	18	ns

Switching Characteristics (Continued)

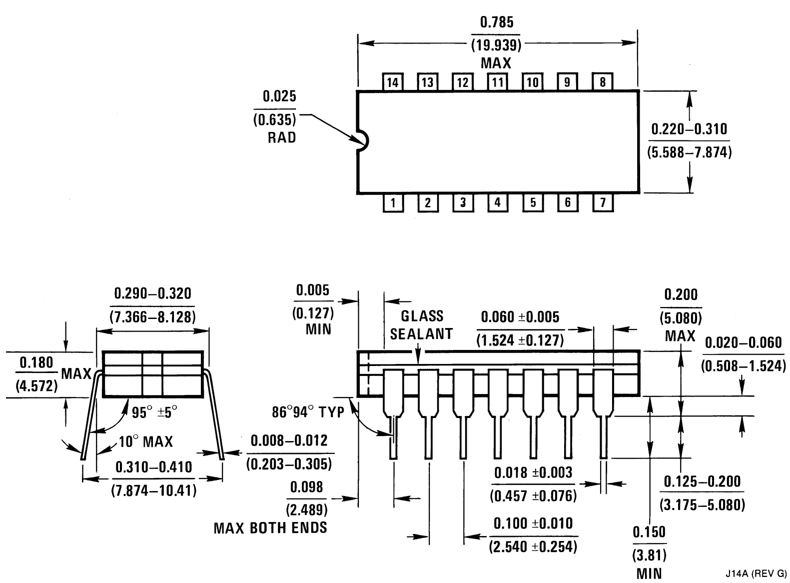
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	54LS51 C_L = 15 pF, R_L = 2 kΩ		DM74LS51 C_L = 50 pF, R_L = 2 kΩ		Units
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output		20	3	15	ns

Physical Dimensions inches (millimeters) unless otherwise noted

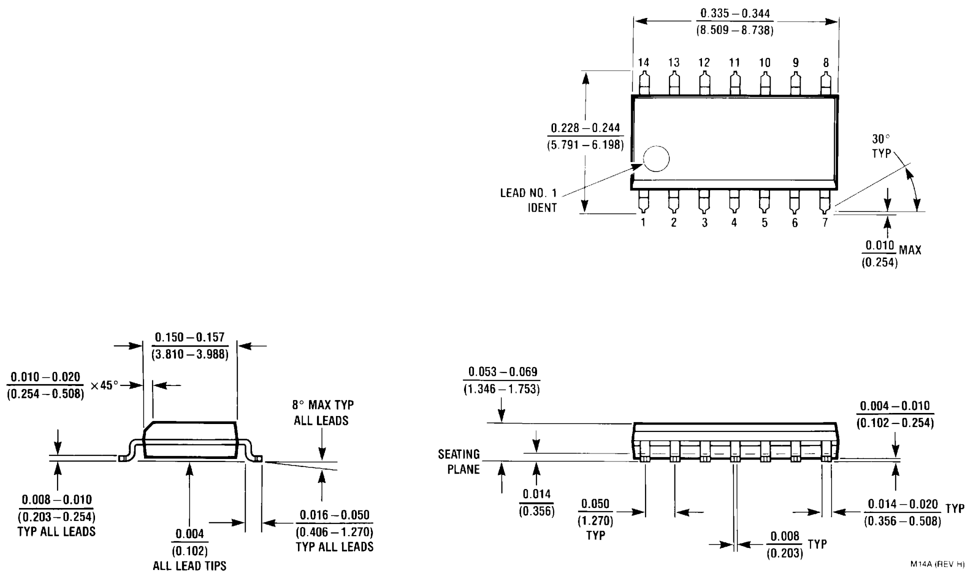


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS51LMQB
Package Number E20A

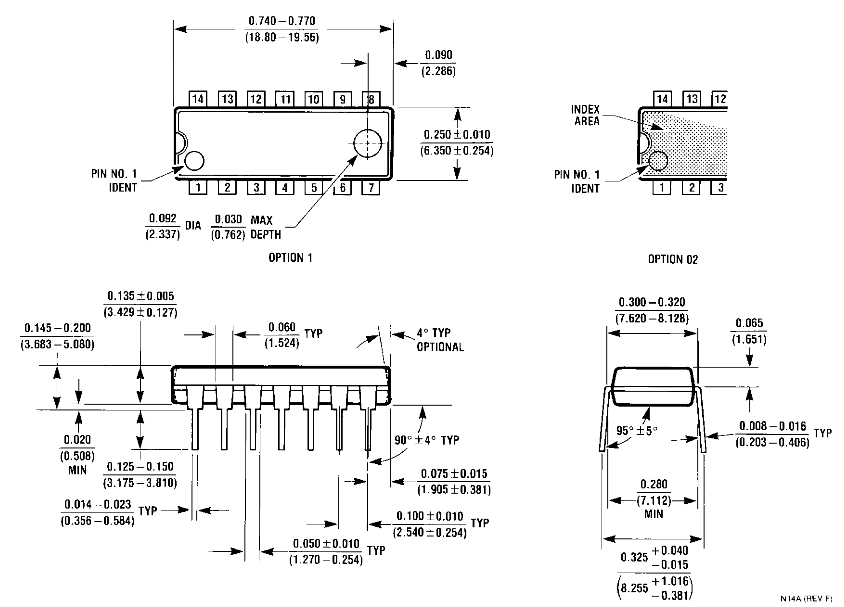


Ceramic Dual-In-Line Package (J)
Order Number 54LS51DMQB
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

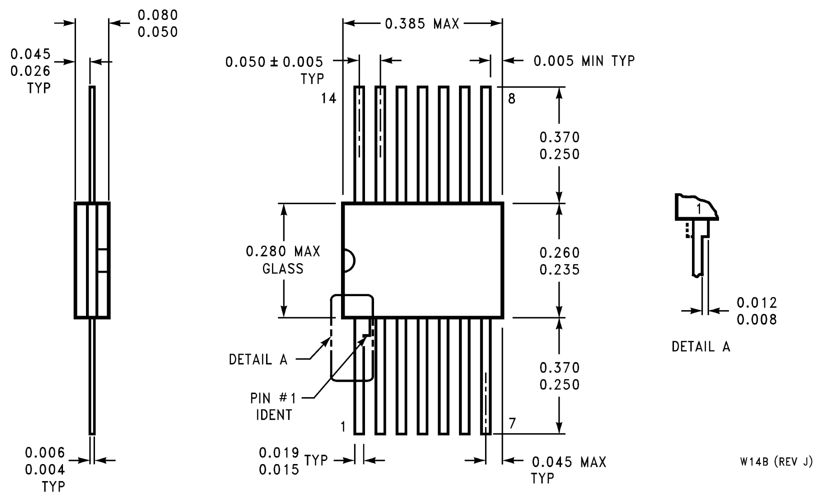


14-Lead Small Outline Molded Package (M)
Order Number DM74LS51M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS51N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS51FMQB
Package Number W14B

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National Semiconductor

January 1993

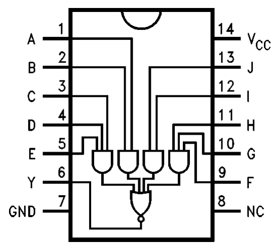
DM54LS54/DM74LS54
4-WIDE, 2-Input AND-OR-INVERT Gate

General Description

This device contains a combination of four, two input AND gates whose outputs are connected to a four input NOR Gate.

Connection Diagram

Dual-In-Line Package



TL/F/10173–1

Order Number DM54LS54J, DM54LS54W, DM74LS54M or DM74LS54N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{AB + CDE + FGH + IJ}$$

Inputs										Output
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**Y**
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	H	X	L
All Other Combinations										H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS54			DM74LS54			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54LS	2.5			V
			DM74LS	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54LS			0.4	V
			DM74LS			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74LS			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74LS			0.1	mA
		V_I = 10V	DM54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54LS	−20		−100	mA
			DM74LS	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				2.0	mA

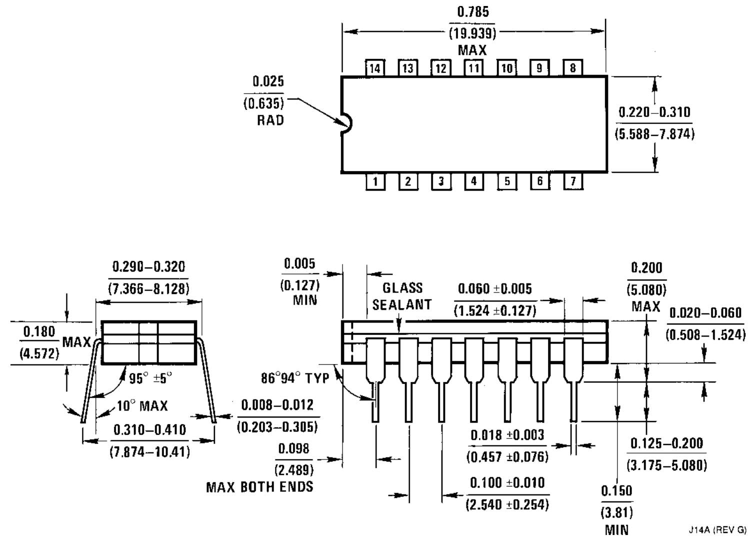
Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	C_L = 15 pF, R_L = 2 kΩ		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

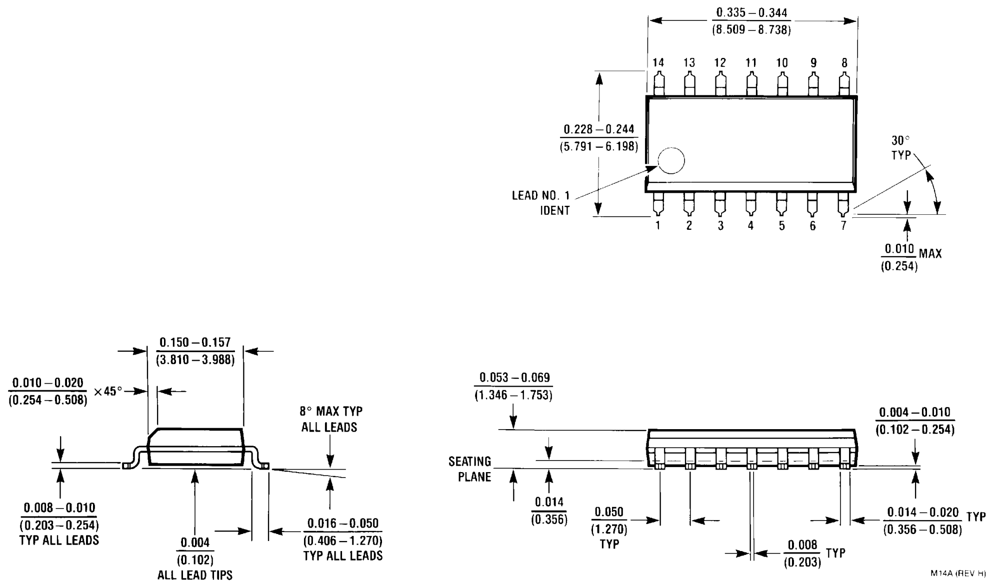
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters)

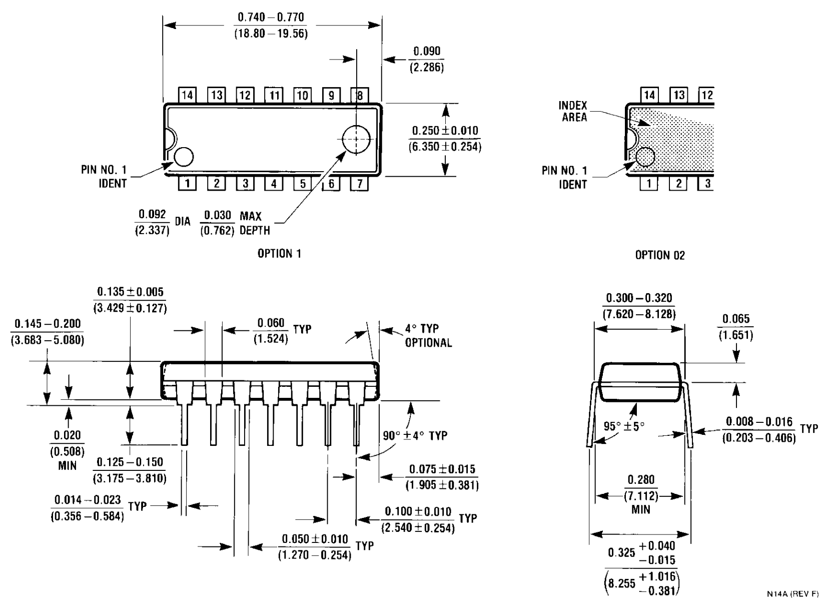


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS54J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

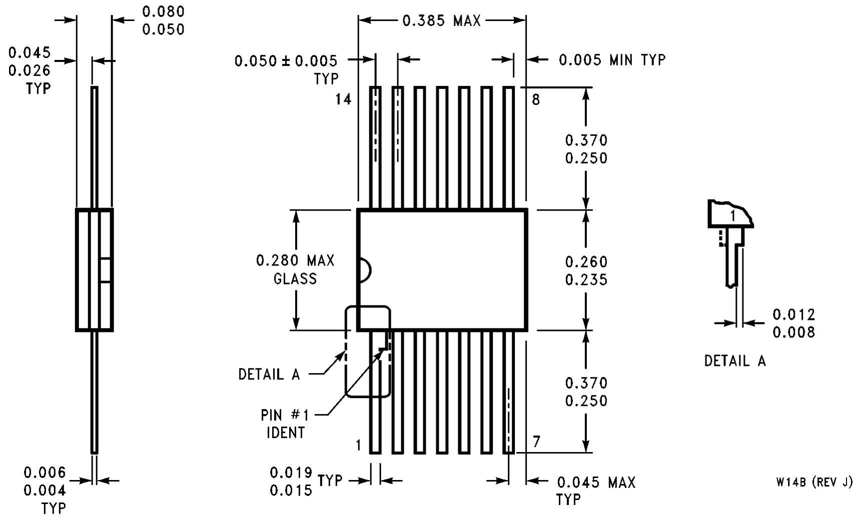


14-Lead Small Outline Molded Package (M)
Order Number DM74LS54M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS54N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS54W
NS Package Number W14B

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National Semiconductor

April 1992

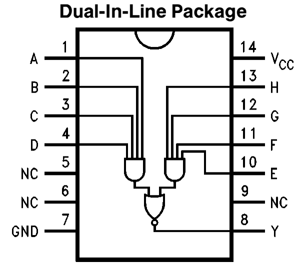
DM54LS55/DM74LS55
2-Wide, 4-Input AND-OR-INVERT Gate

General Description

This device contains a combination of AND-OR-INVERT functions. The internal gates are configured as two, four-input AND gates with their outputs connected to a two-input NOR gate.

Connection Diagram

Dual-In-Line Package



TL/F/10174–1

Order Number DM54LS55J, DM54LS55W, DM74LS55M or DM74LS55N
See NS Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{ABCD + EFGH}$$

Inputs								Output
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**Y**
H	H	H	H	X	X	X	X	L
X	X	X	X	H	H	H	H	L
All Other Combinations								H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

 TL/F/10174

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS55			DM74LS55			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (DM54)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				1.3	mA

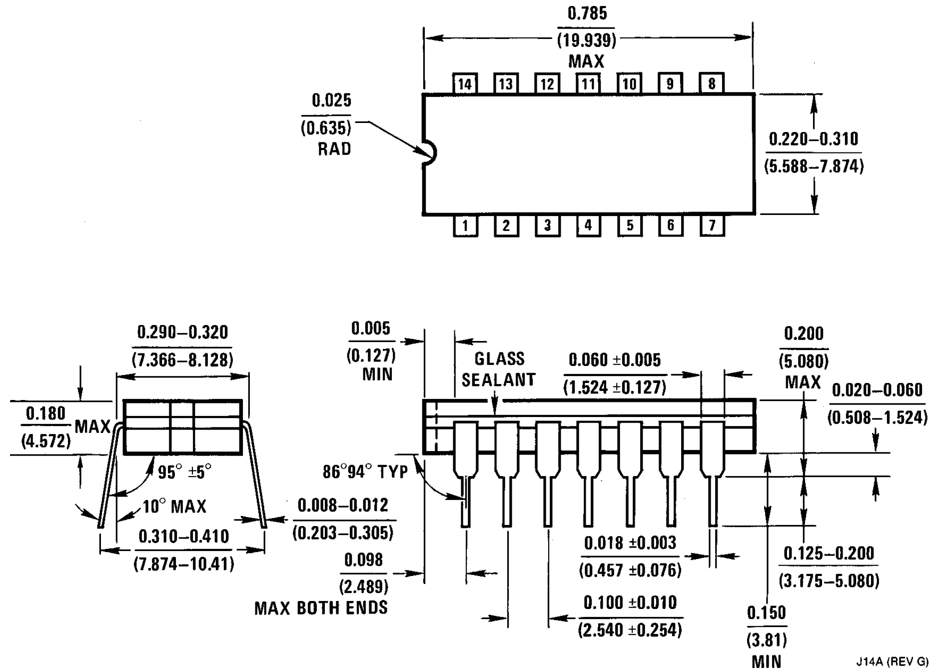
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C

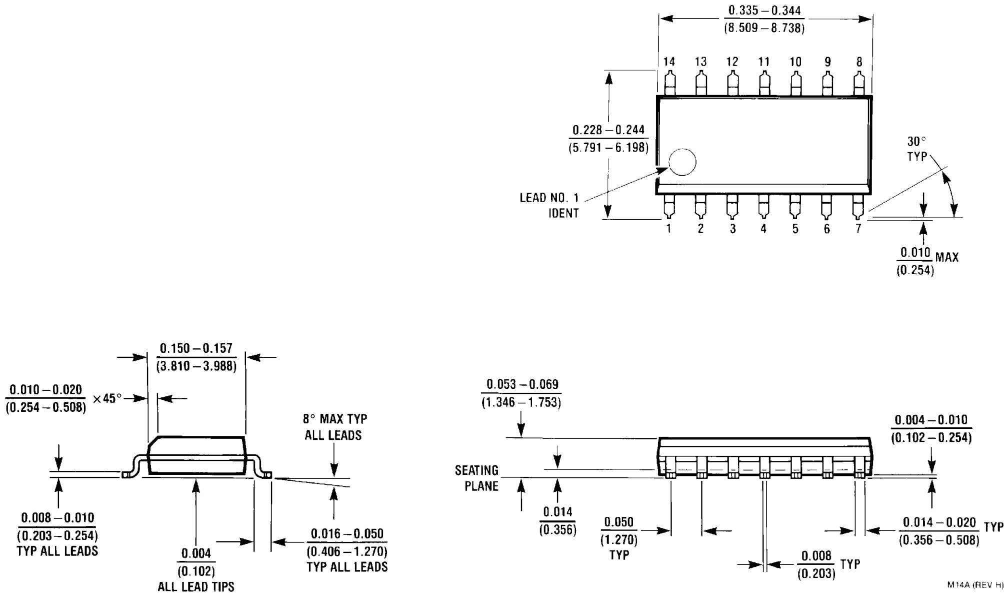
Symbol	Parameter	C_L = 15 pF, R_L = 2 kΩ		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Time		15 15	ns

Physical Dimensions inches (millimeters)

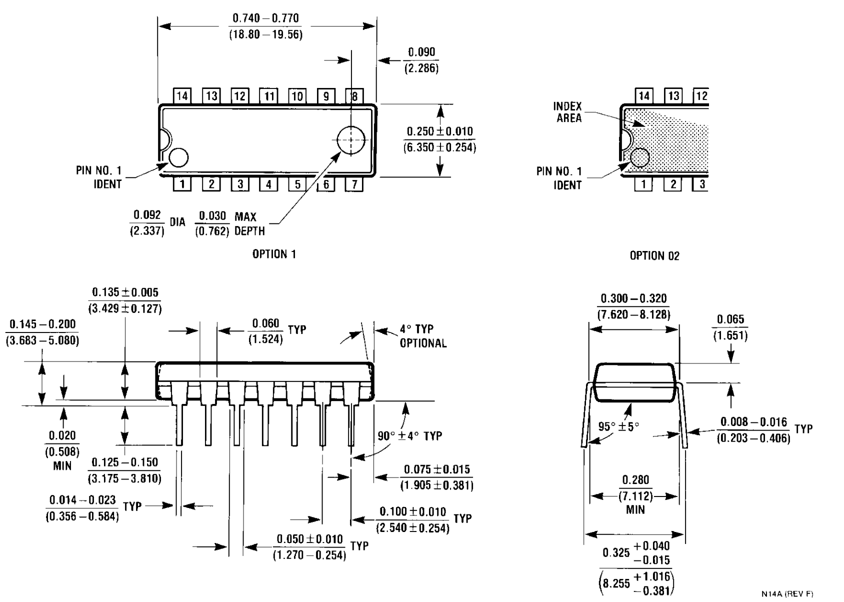


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS55J
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

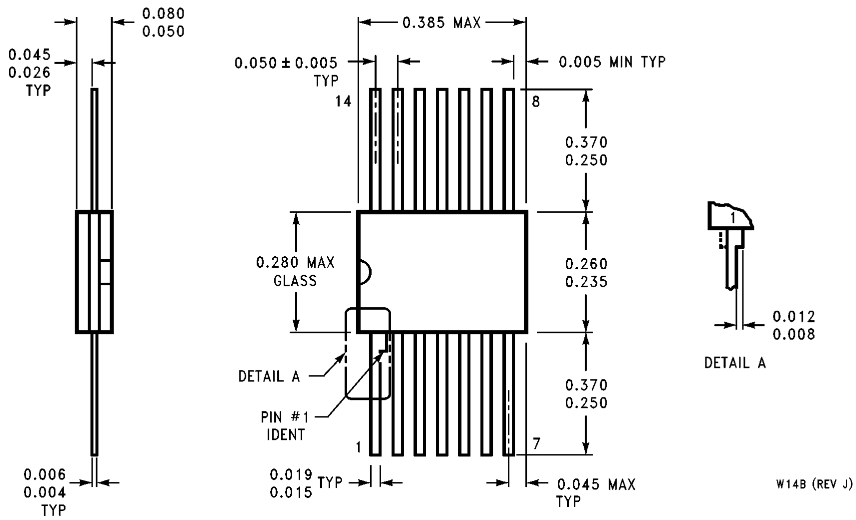


14-Lead Small Outline Molded Package (M)
Order Number DM74LS55M
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS55N
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS55W
NS Package Number W14B

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FAIRCHILD
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March 1998

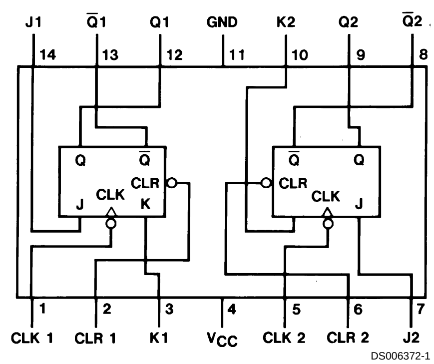
DM74LS73A
Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS73A			DM74LS73A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 3)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 4)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 2, 3)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 2, 4)		25↓			25↓			ns
t_H	Hold Time (Notes 2, 3)		0↓			0↓			ns
t_H	Hold Time (Notes 2, 4)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 3: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	J, K			0.1	mA
		V_I = 7V	Clear			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max	J, K			20	μA
		V_I = 2.7V	Clear			60	
			Clock			80	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			4	6	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

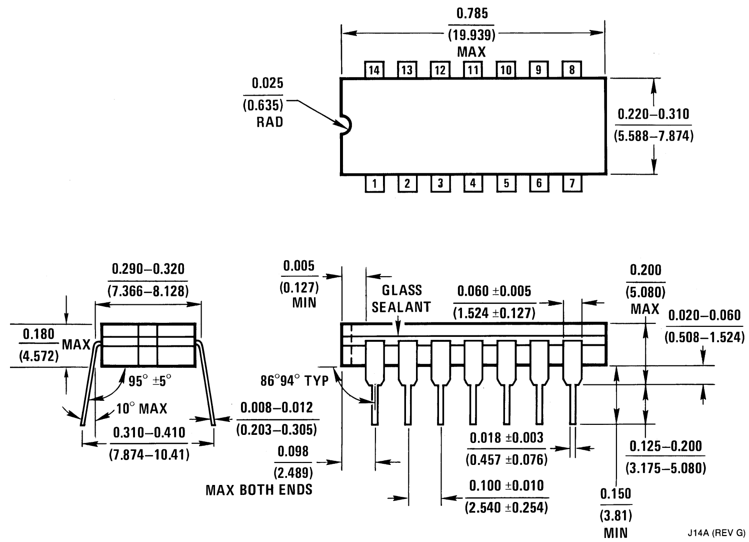
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

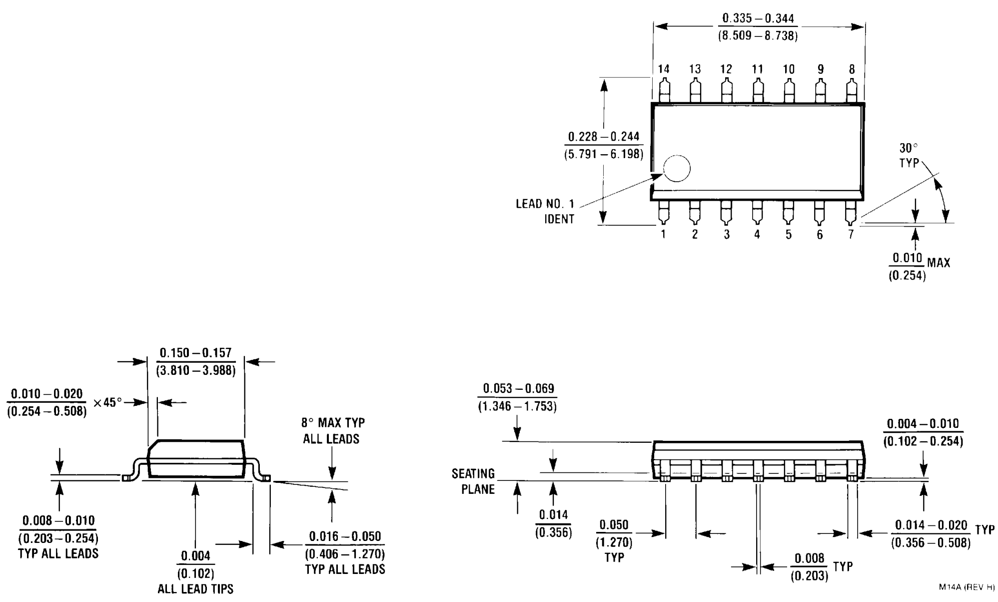
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 7: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Physical Dimensions inches (millimeters) unless otherwise noted

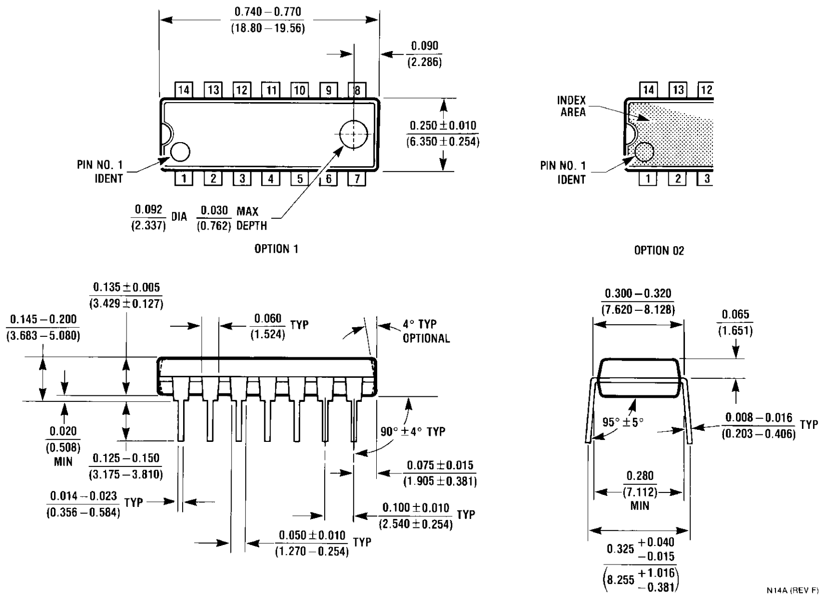


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS73AJ
Package Number J14A

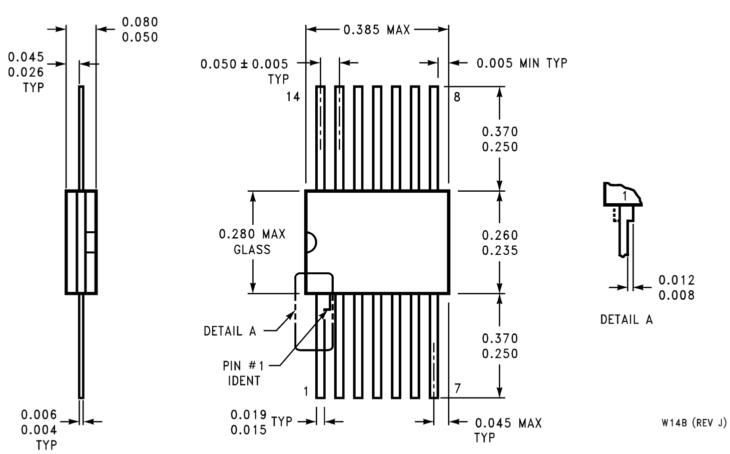


14-Lead Small Outline Molded Package (M)
Order Number DM74LS73AM
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS73AN
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS73AW
Package Number W14B

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS74A
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

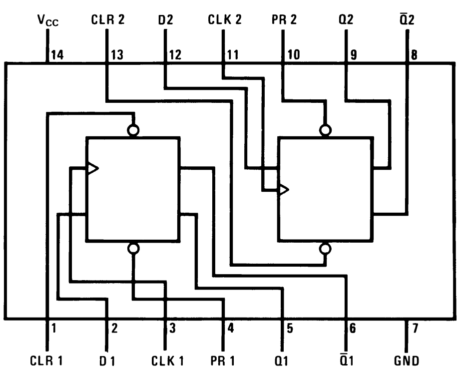
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate military/aerospace device (54LS74) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006373-1

Order Number 54LS74DMQB, 54LS74FMQB, 54LS74LMQB, DM54LS74AJ, DM54LS74AW, DM74LS74AM or DM74LS74AN
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
PR	**CLR**	**CLK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 5)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 5)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 3, 4)		20↑			20↑			ns
t_{SU}	Setup Time (Notes 3, 5)		25↑			25↑			ns
t_H	Hold Time (Notes 3, 6)		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 4: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 6: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Data			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Data			20	μA
			Clock			20	
			Clear			40	
			Preset			40	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Data			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 8)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 9)			4	8	mA

Note 7: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

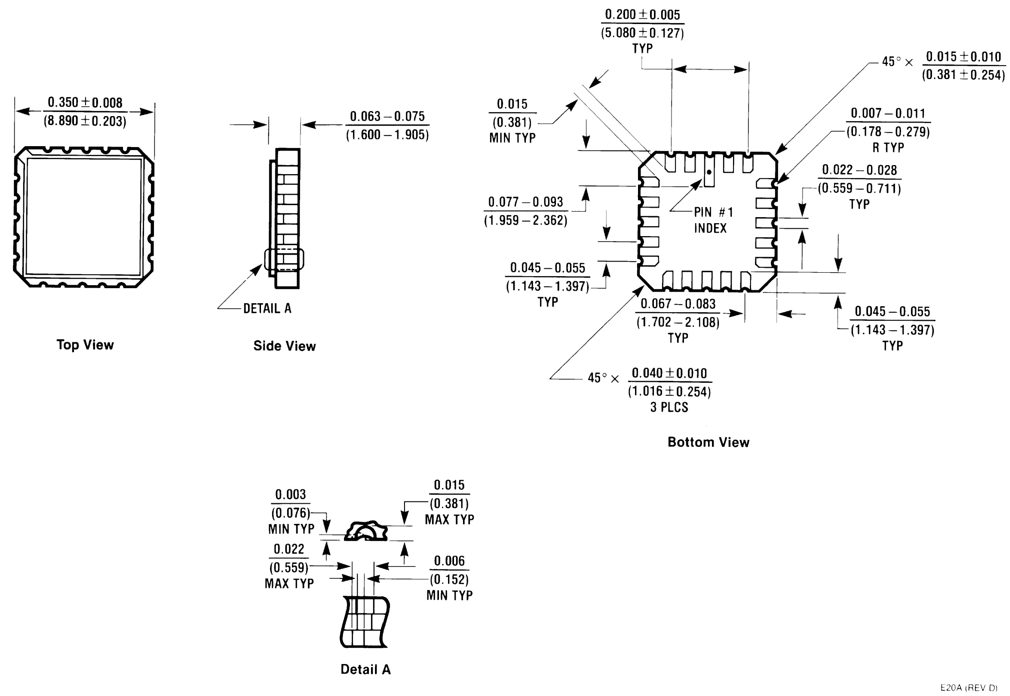
Note 9: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Switching Characteristics

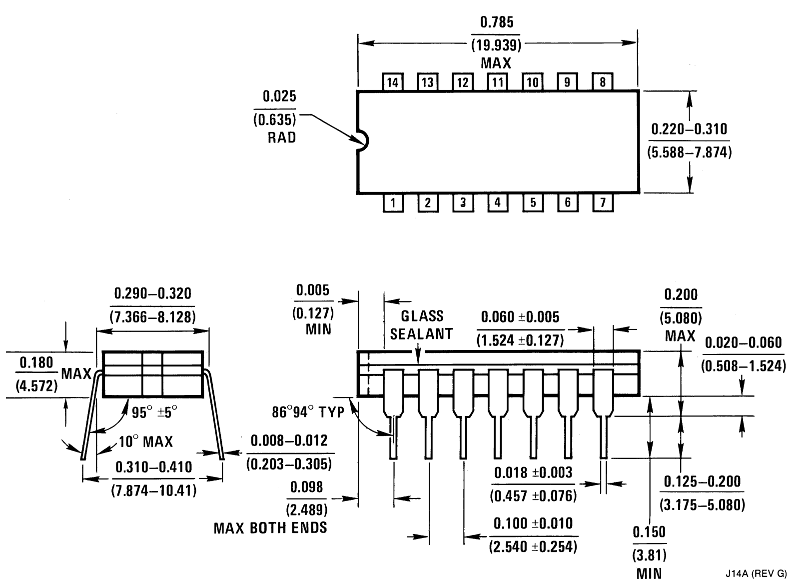
at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns

Physical Dimensions inches (millimeters) unless otherwise noted

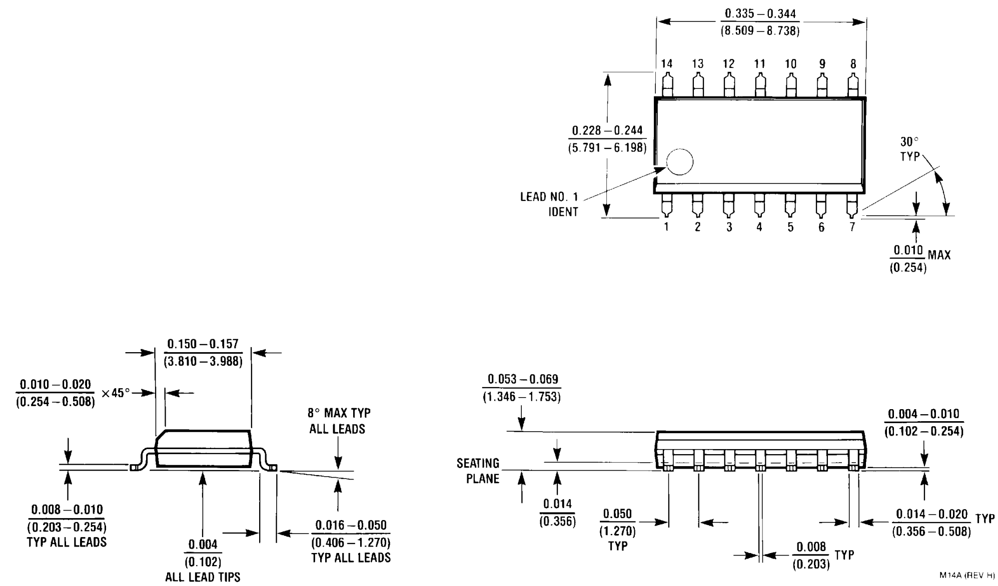


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS74LMQB
Package Number E20A

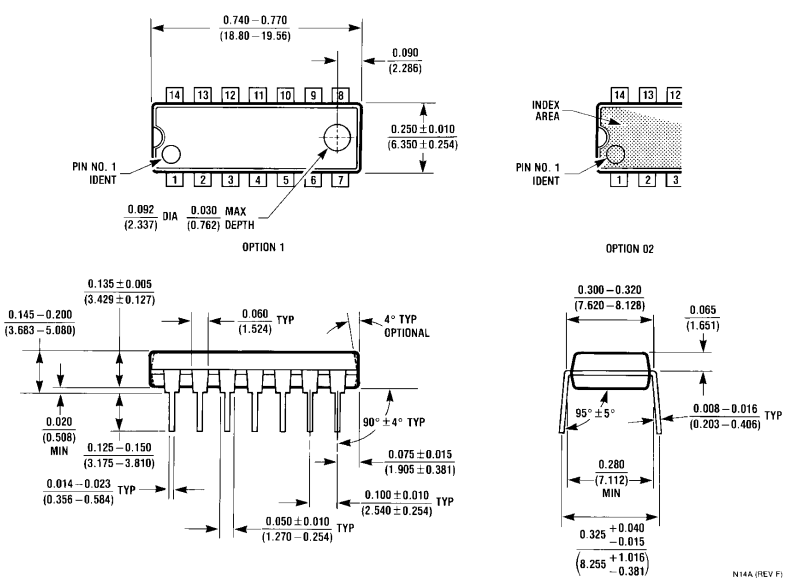


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS74DMQB or DM54LS74AJ
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

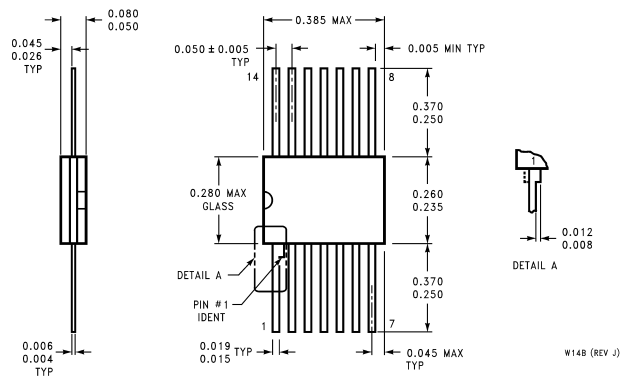


14-Lead Small Outline Molded Package (M)
Order Number DM74LS74AM
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS74AN
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS74FMQB or DM54LS74AW
Package Number W14B

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS75
Quad Latches

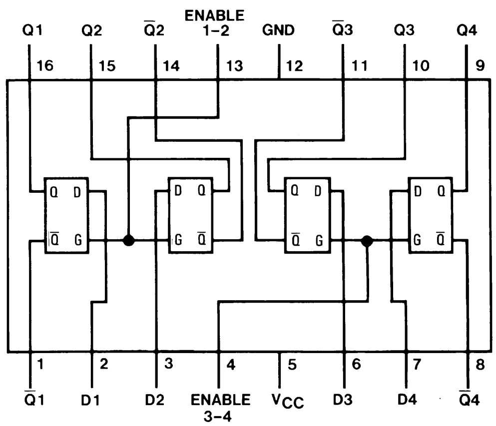
General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occured) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Connection Diagram

Dual-In-Line Package



DS006374-1

Order Number DM54LS75J, DM54LS75W, DM74LS75M or DM74LS75N
See Package Number J16A, M16A, N16A or W16A

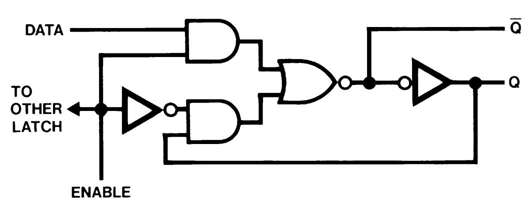
Function Table

(Each Latch)

Inputs		Outputs	
D	**Enable**	**Q**	**$\overline{Q}$**
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care
Q_0 = The Level of Q Before the High-to-Low Transition of ENABLE

Logic Digram (Each Latch)



DS006374-2

 DS006374

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS75			DM74LS75			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width (Note 5)	20			20			ns
t_{SU}	Setup Time (Note 5)	20			20			ns
t_H	Hold Time (Note 5)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.5		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			Enable			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	μA
			Enable			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			Enable			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

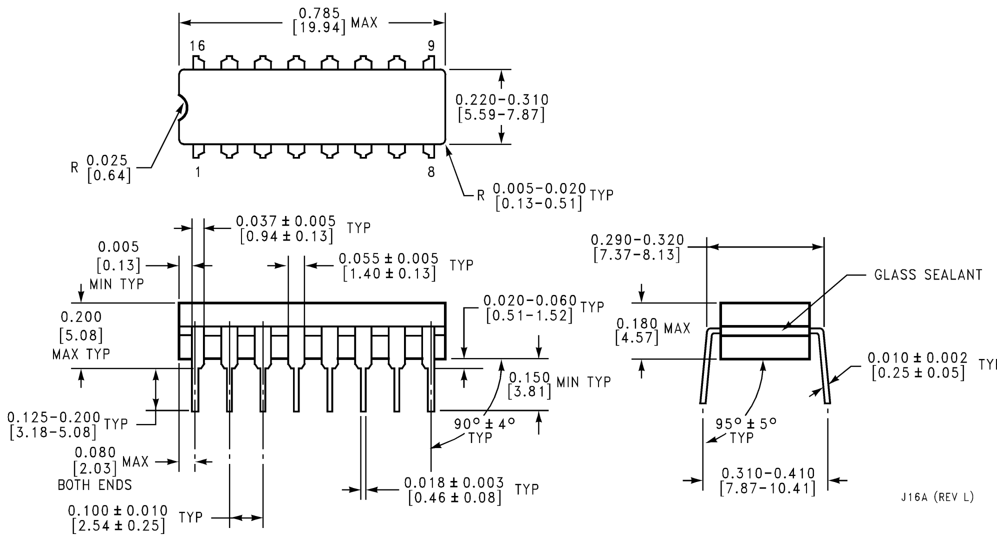
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics

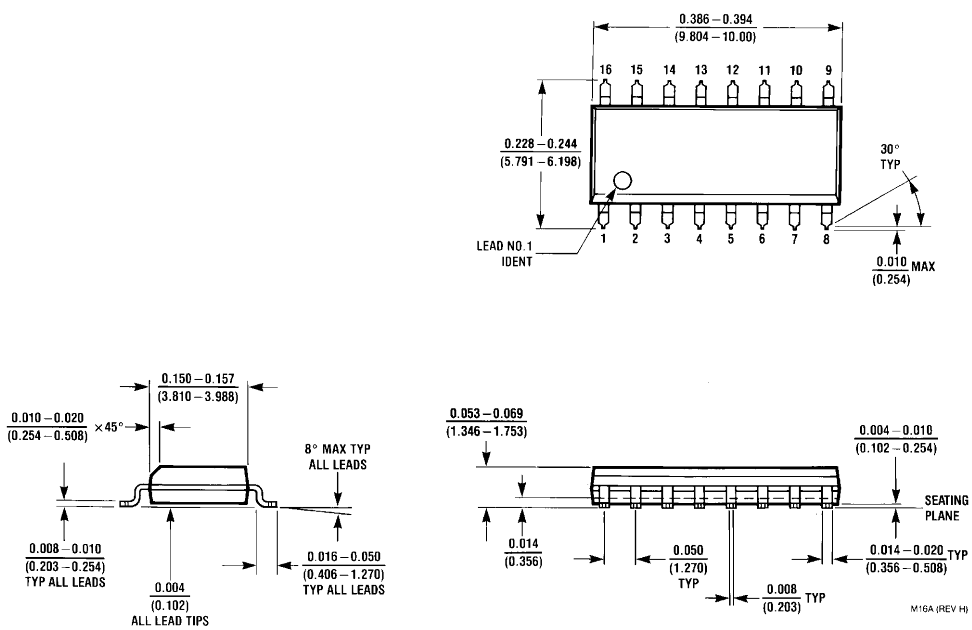
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to $\overline{Q}$		30		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to $\overline{Q}$		15		20	ns

Physical Dimensions inches (millimeters) unless otherwise noted

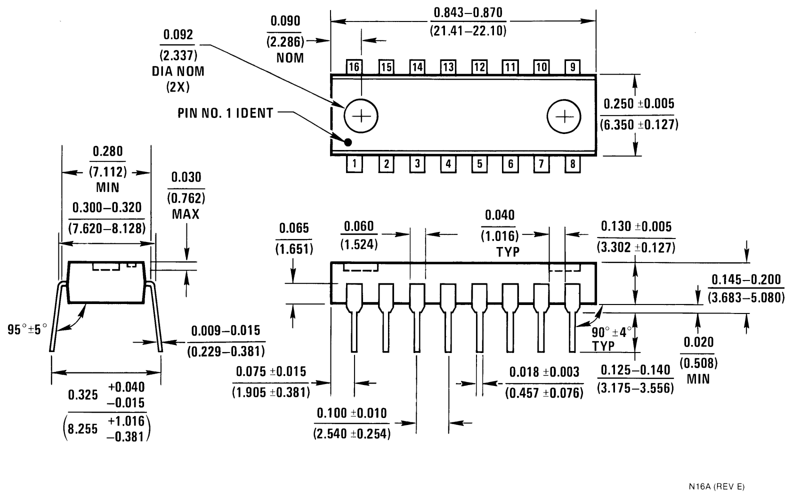


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS75J
Package Number J16A

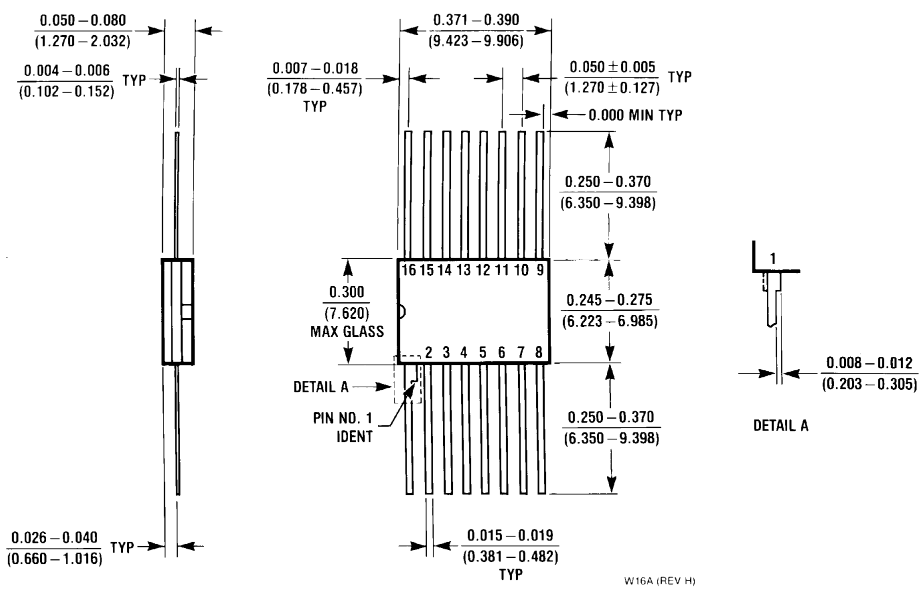


16-Lead Small Outline Molded Package (M)
Order Number DM74LS75M
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS75N
Package Number N16A



16-Lead Ceramic Flat Package (W)
Order Number DM54LS75W
Package Number W16A

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March 1998

DM74LS83A
4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

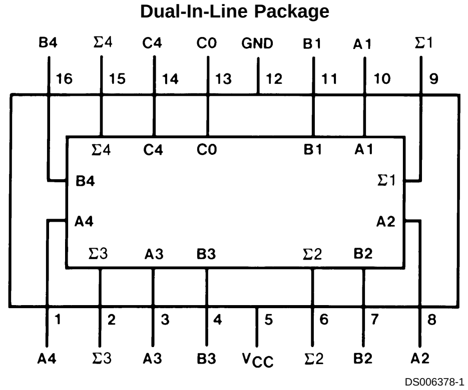
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS83A) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS83ADMQB, 54LS83AFMQB, DM54LS83AJ, DM54LS83AW, DM74LS83AWM or DM74LS83AN
See Package Number J16A, M16B, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS83A			DM74LS83A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max	A or B			0.2	mA
	Input Voltage	V_I = 7V	C0			0.1	
I_{IH}	High Level Input	V_{CC} = Max	A or B			40	μA
	Current	V_I = 2.7V	C0			20	
I_{IL}	Low Level Input	V_{CC} = Max	A or B			−0.8	mA
	Current	V_I = 0.4V	C0			−0.4	
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 3)	DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 4)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 5)			22	39	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 5: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to C4		17		26	ns

Truth Table

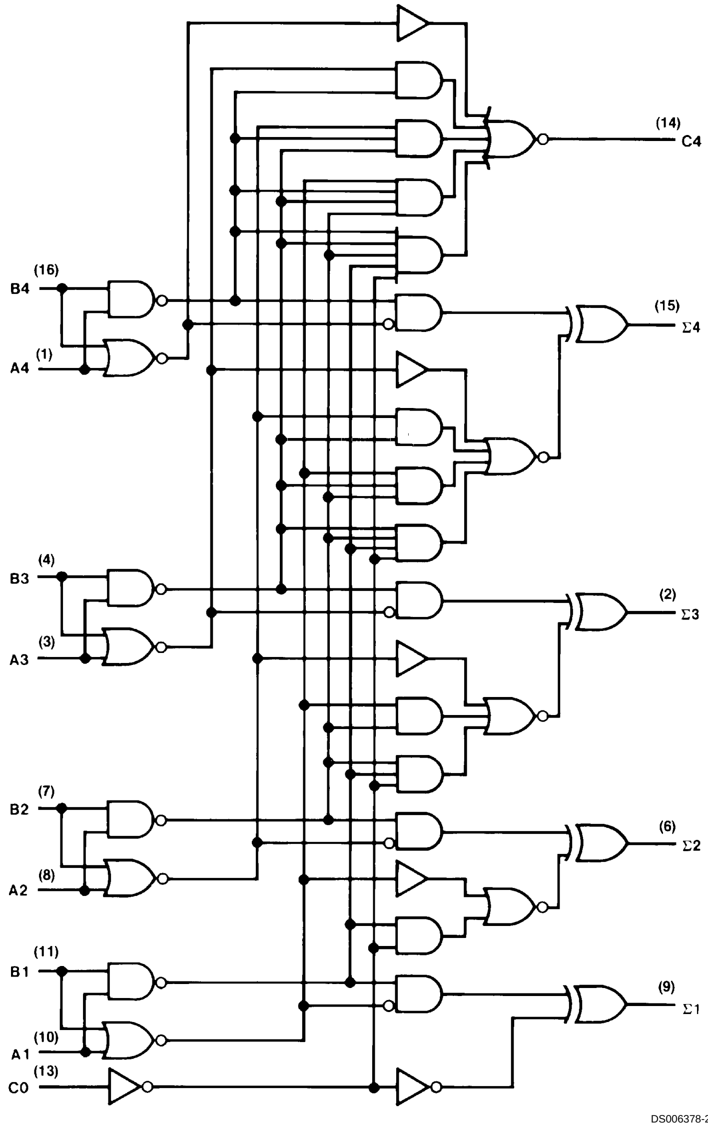
Inputs				Outputs					
				When C0 = L / When C2 = L			When C0 = H / When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

DS006378-3

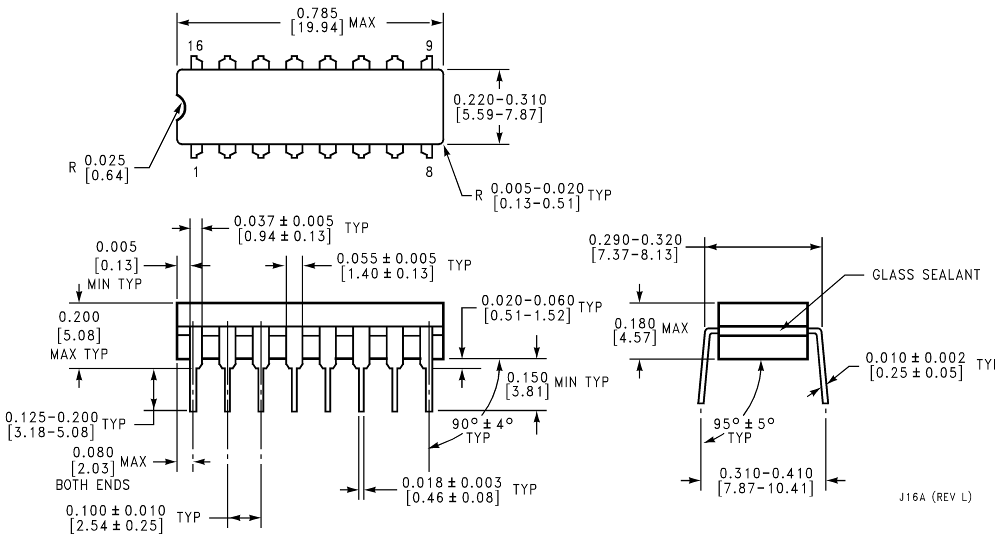
H = High Level, L = Low Level

Note 6: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

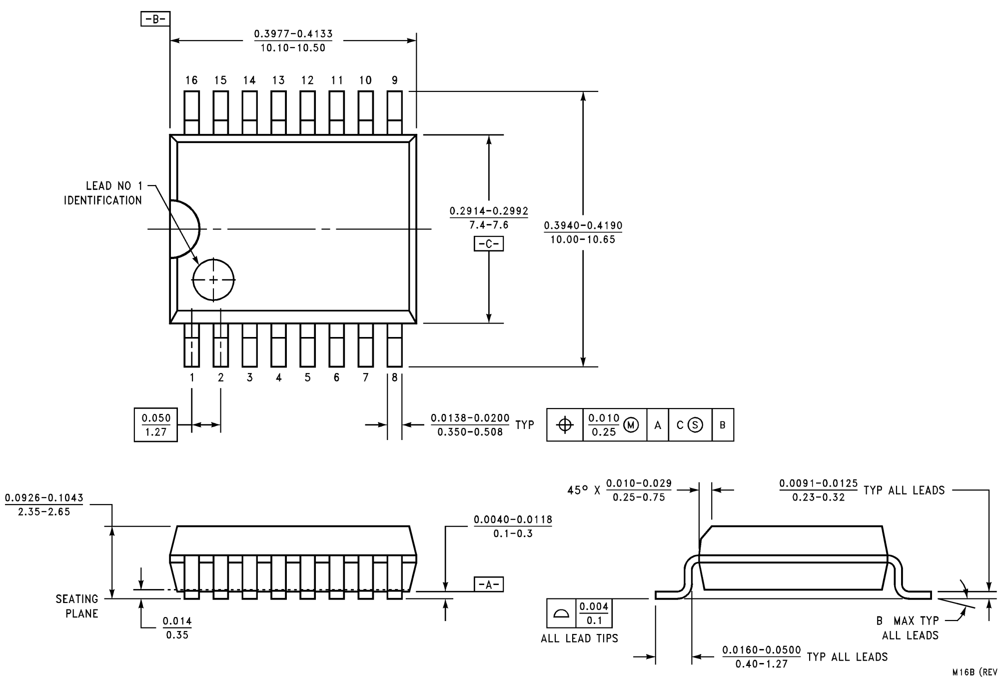
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

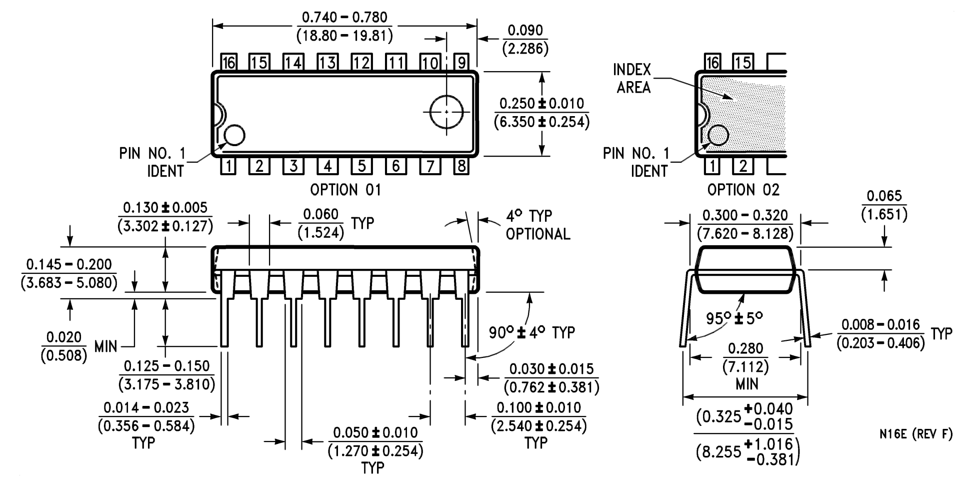


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS83ADMQB or DM54LS83AJ
Package Number J16A

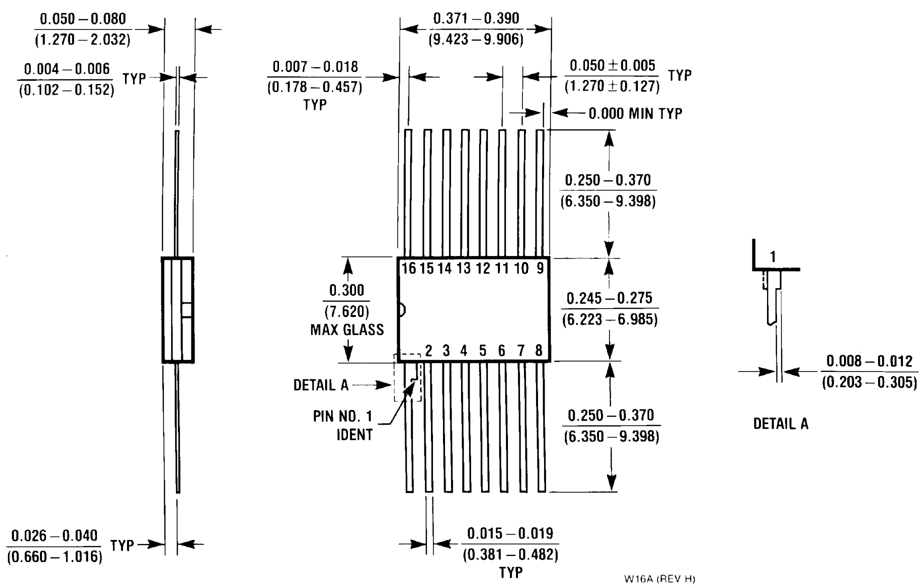


16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS83AWM
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS83AN
Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number 54LS83AFMQB or DM54LS83AW
Package Number W16A

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March 1998

DM74LS85
4-Bit Magnitude Comparators

General Description

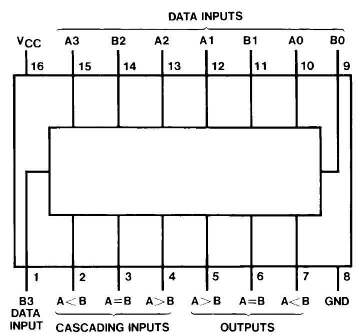
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns
- Alternate Military/Aerospace device (54LS85) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006379-1

Order Number 54LS85DMQB, 54LS85FMQB, 54LS85LMQB, DM54LS85J, DM54LS85W, DM74LS85M or DM74LS85N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	A < B			0.1	mA
		V_I = 7V	A > B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max	A < B			20	μA
		V_I = 2.7V	A > B			20	
			Others			60	
I_{IL}	Low Level Input Current	V_{CC} = Max	A < B			−0.4	mA
		V_I = 0.4V	A > B			−0.4	
			Others			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			10	20	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

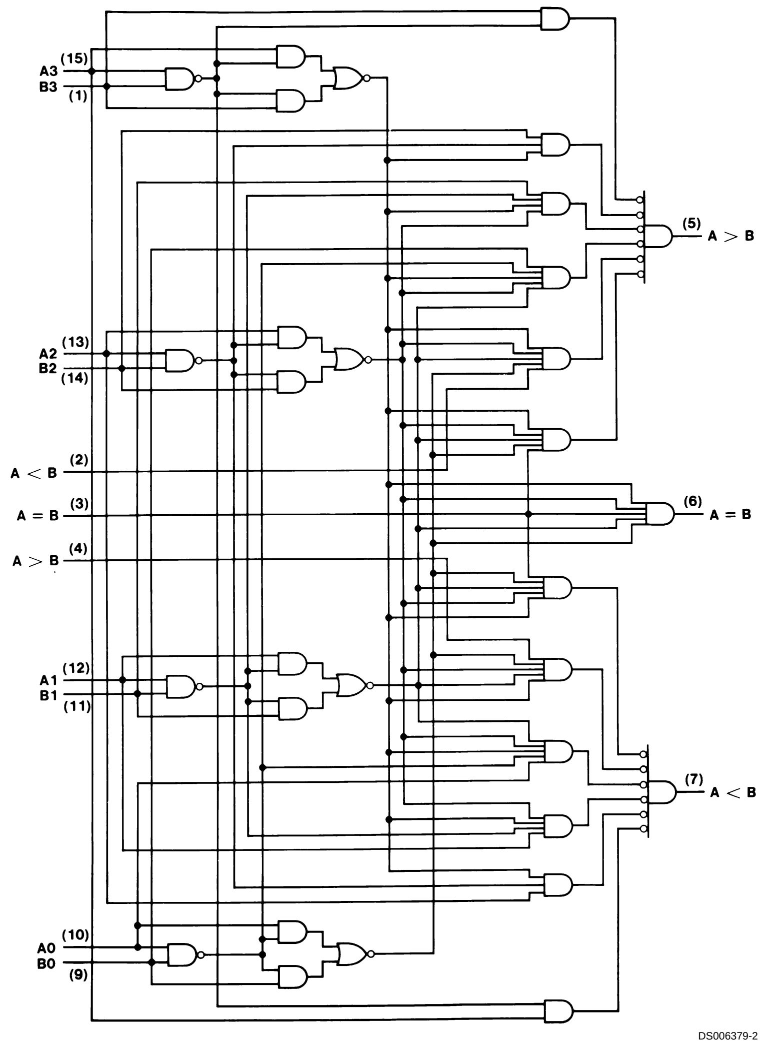
Note 4: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics

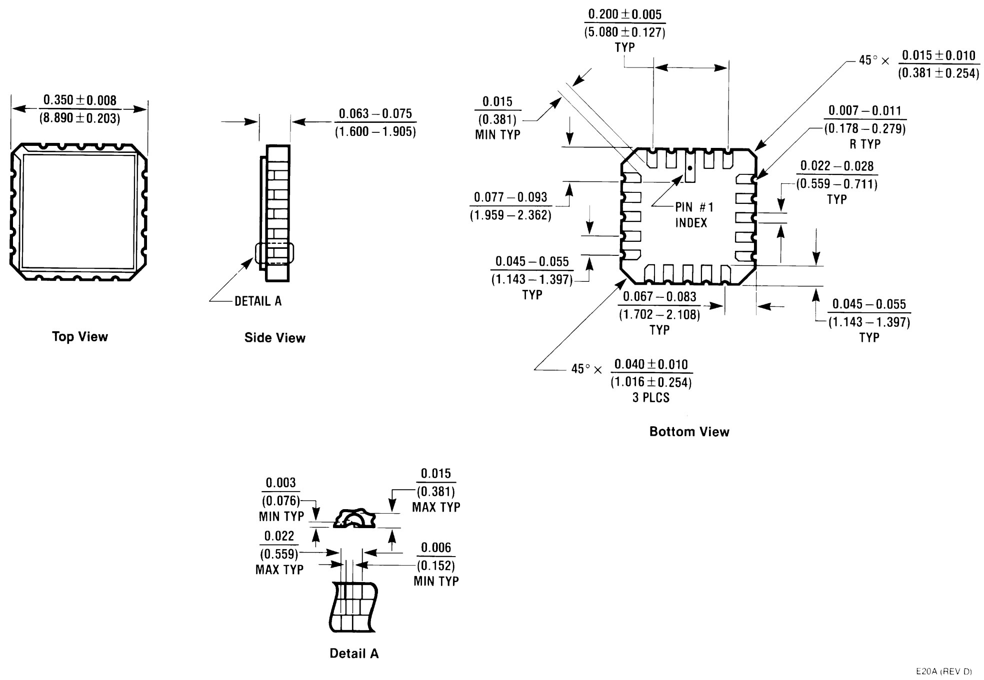
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From Input	To Output	Number of Gate Levels	R_L = 2 kΩ				Units
					C_L = 15 pF		C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A =B	A = B	2		20		25	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

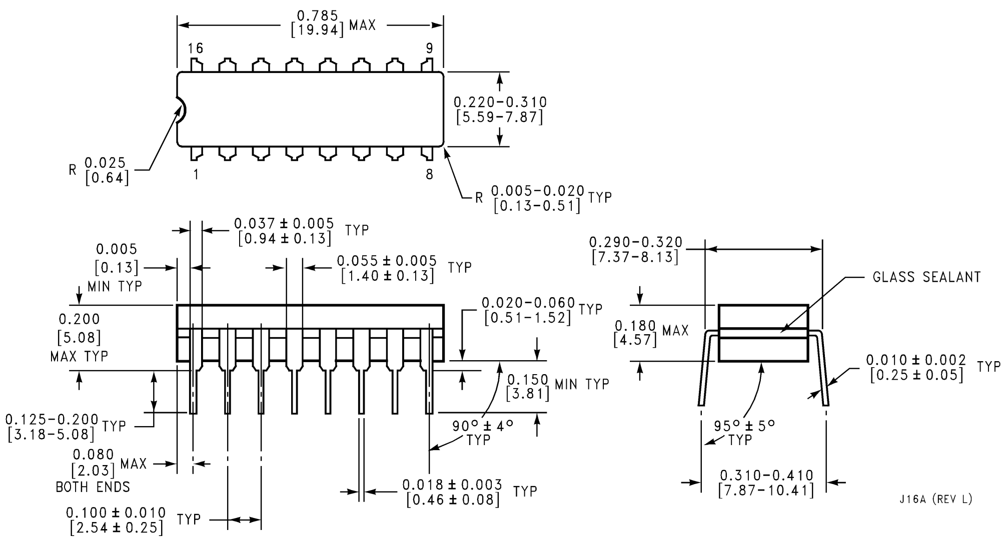
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

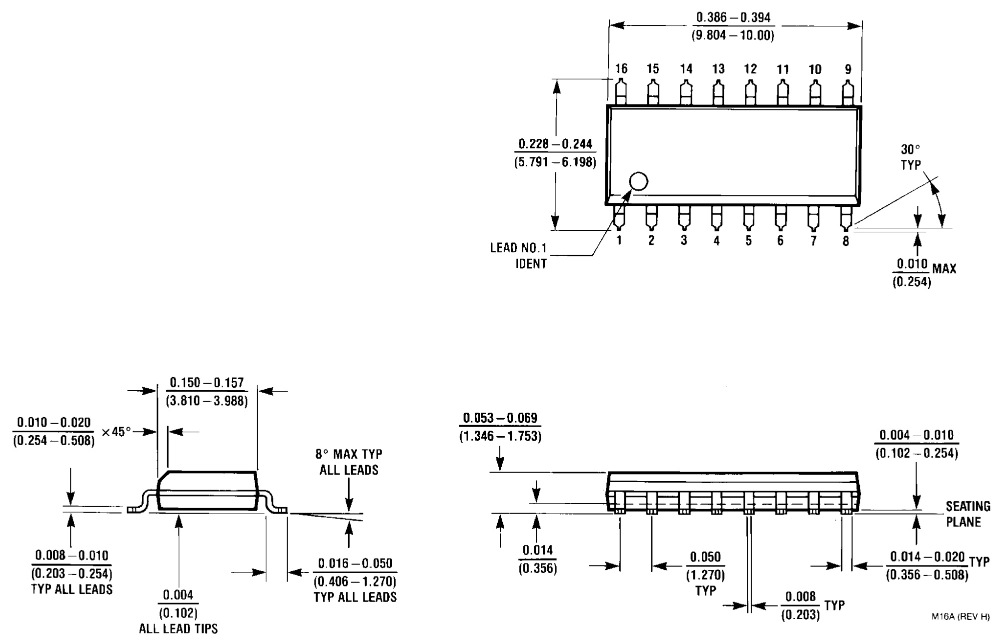


Chip Carrier Package (E)
Order Number 54LS85LMQB
Package Number E20A

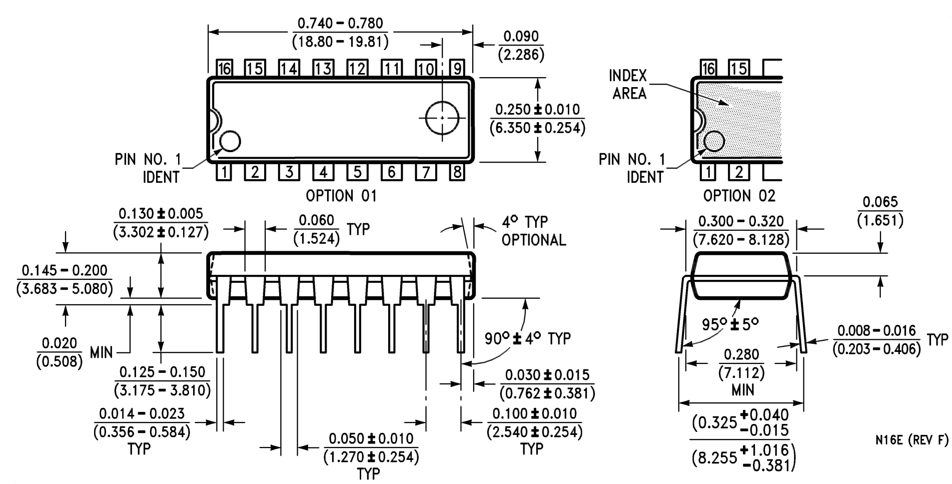


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS85DMQB or DM54LS85J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

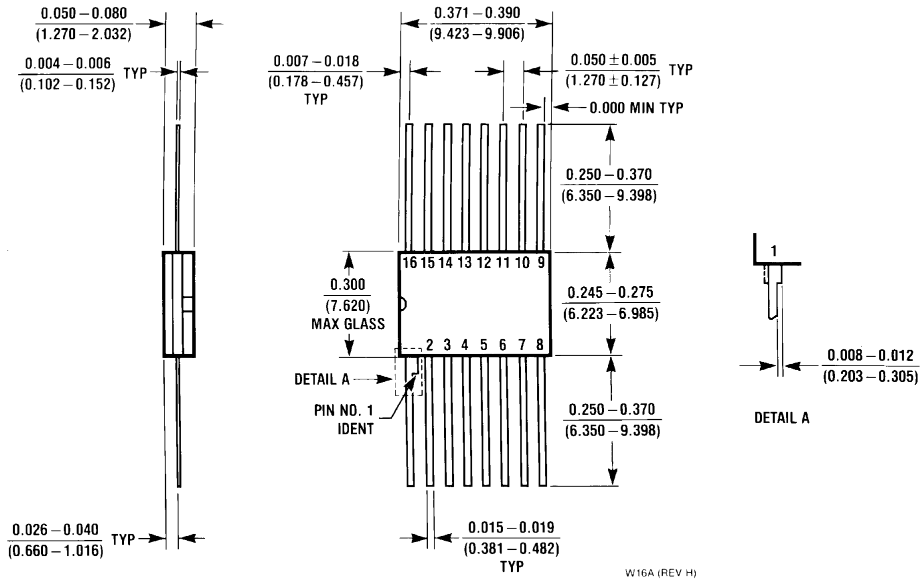


16-Lead Small Outline Molded Package (M)
Order Number DM74LS85M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS85N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS85FMQB or DM54LS85W
Package Number W16A

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March 1998

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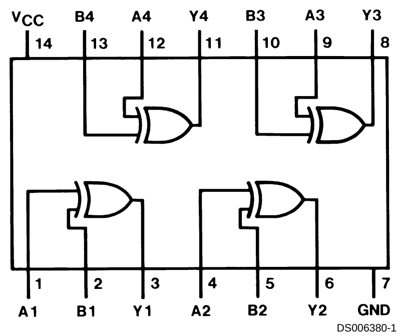
DM74LS86
Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS86J, DM54LS86W, DM74LS86M or DM74LS86N
See Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = A \oplus B = \overline{A}\,B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

DM74LS86 Quad 2-Input Exclusive-OR Gates

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS86			DM74LS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max,	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 4)			6.1	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 5)			9	15	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CCH} is measured with all outputs open, one input at each gate at 4.5V, and the other inputs grounded.

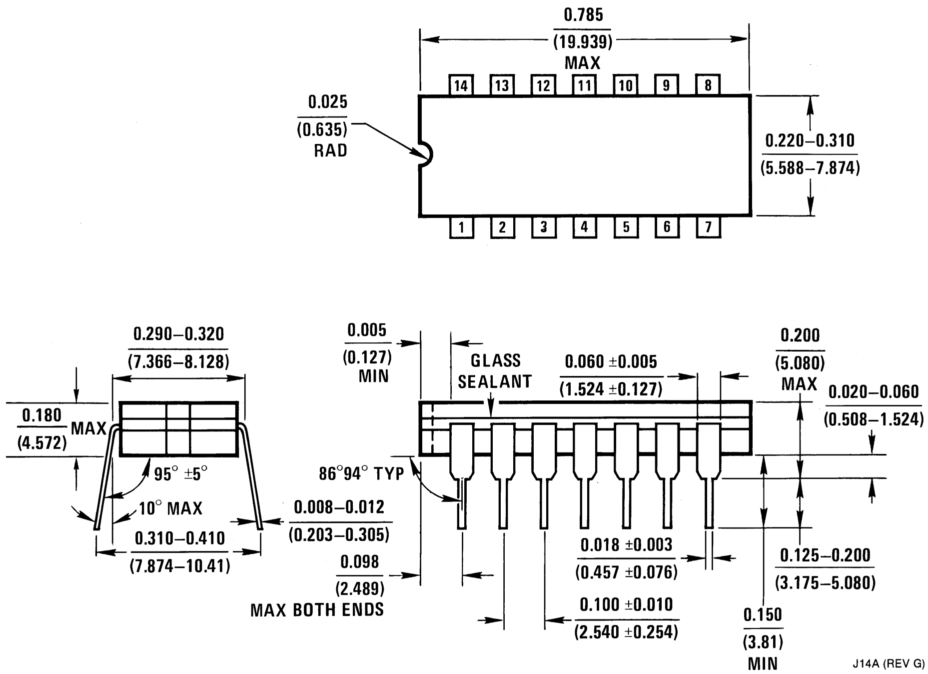
Note 5: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics

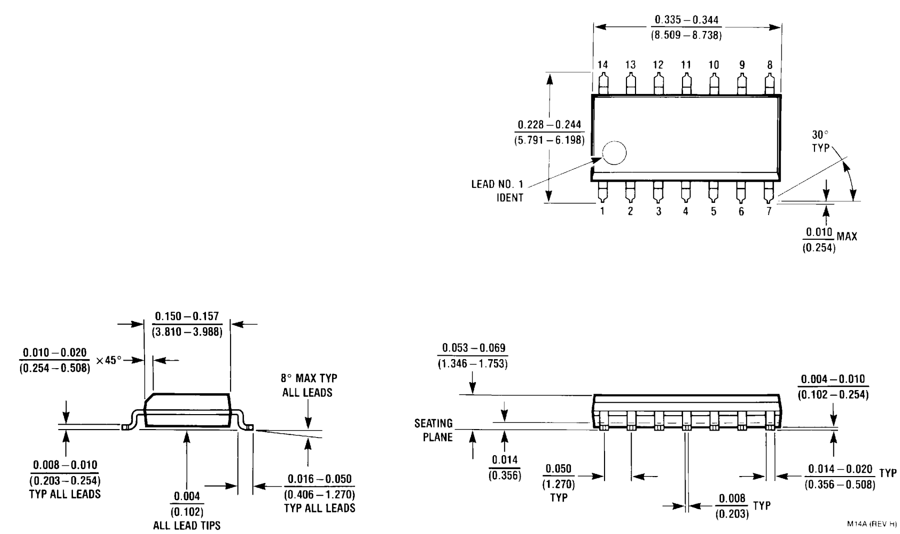
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			12		15	ns

Physical Dimensions inches (millimeters) unless otherwise noted

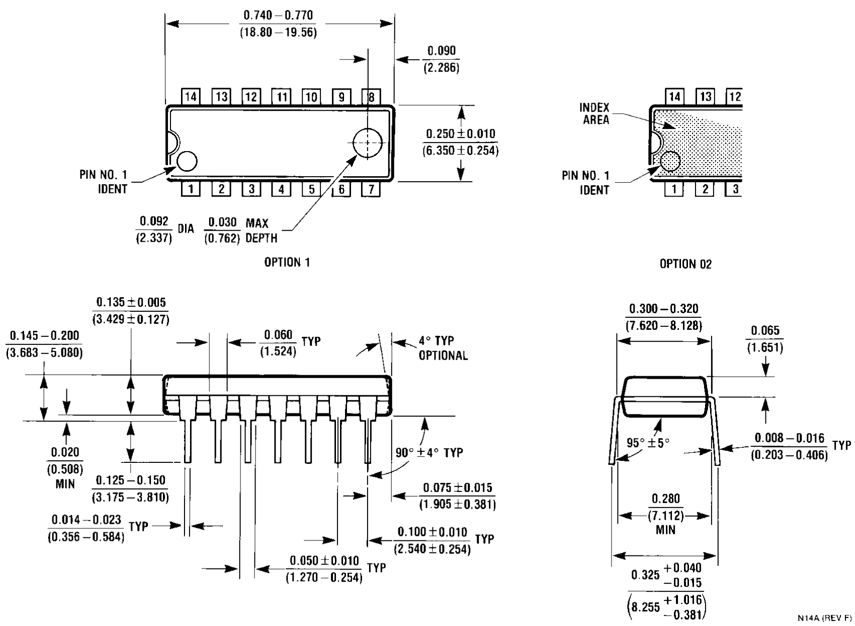


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS86J
Package Number J14A

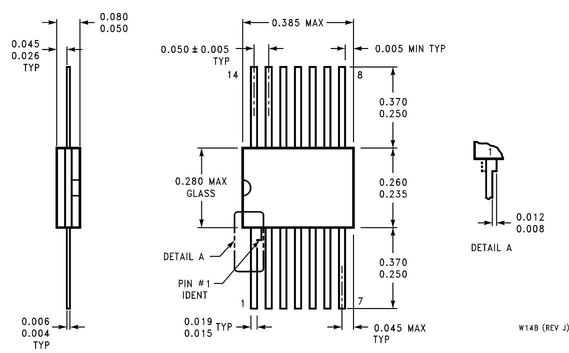


14-Lead Small Outline Molded Package (M)
Order Number DM74LS86M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS86N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM74LS86W
Package Number W14B

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March 1998

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DM74LS90/DM74LS93 Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.

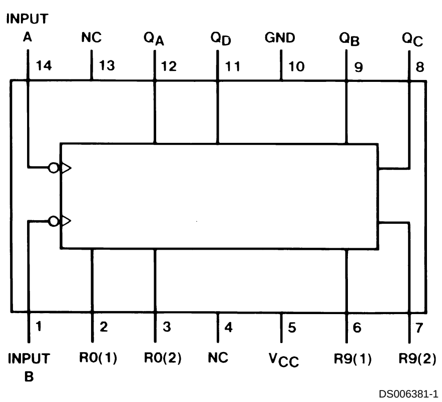
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

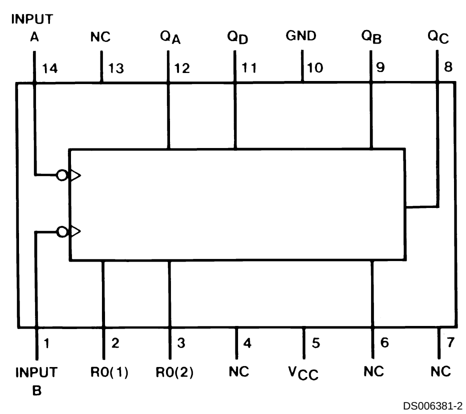
Features

- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagrams (Dual-In-Line Packages)



Order Number DM74LS90M or DM74LS90N
See Package Number M14A or N14A



Order Number DM74LS93M or DM74LS93N
See Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM74LS90			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 3)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 2)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 3)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 2)		25			ns
t_{REL}	Reset Release Time (Note 3)		35			ns
T_A	Free Air Operating Temperature		0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

’LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 7)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	

’LS90 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	15	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 7: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS90 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		52	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Recommended Operating Conditions

Symbol	Parameter		DM74LS93 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 8)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 9)	A to Q_A	0		20	
		B to Q_B	0		10	
t_W	Pulse Width (Note 8)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 9)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 8)		25			ns
t_{REL}	Reset Release Time (Note 9)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

’LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 13)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 11)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 12)			9	15	mA

Note 10: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 13: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS93 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		85	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		90	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Function Tables

LS90
BCD Count Sequence

(Note 14)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
Bi-Quinary (5-2)

(Note 15)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note 14: Output Q_A is connected to input B for BCD count.

Note 15: Output Q_D is connected to input A for bi-quinary count.

Note 16: Output Q_A is connected to input B.

Note 17: H = High Level, L = Low Level, X = Don't Care.

LS93
Count Sequence

(Note 16)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

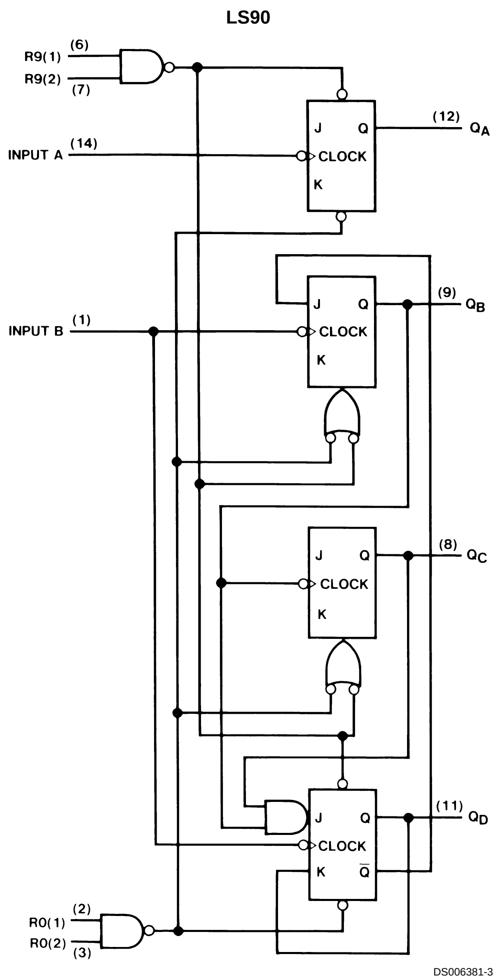
LS90
Reset/Count Truth Table

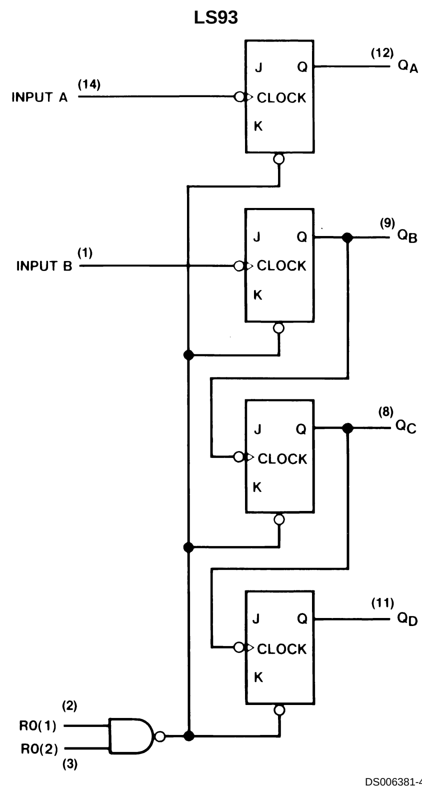
Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

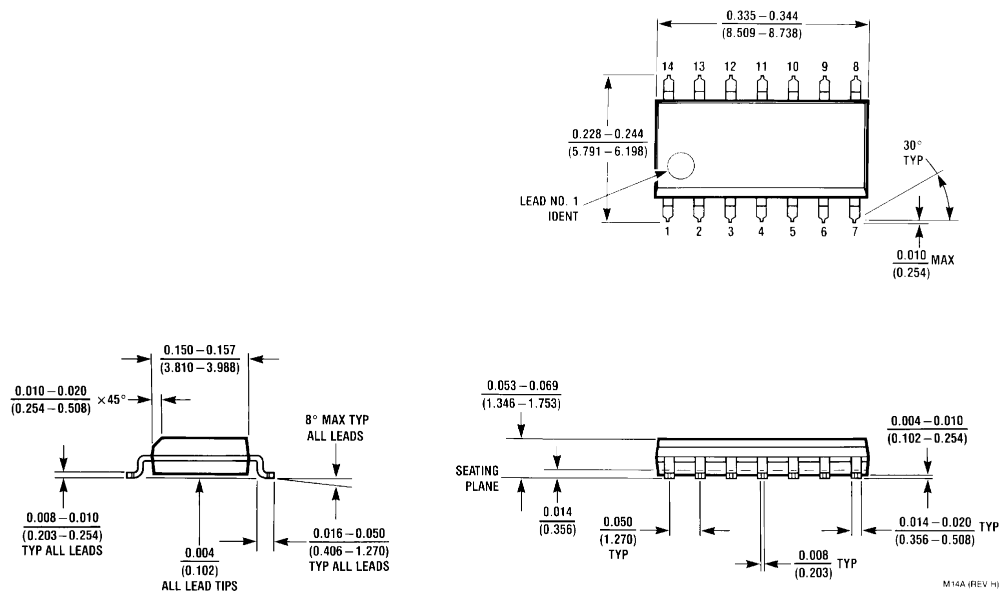
Logic Diagrams



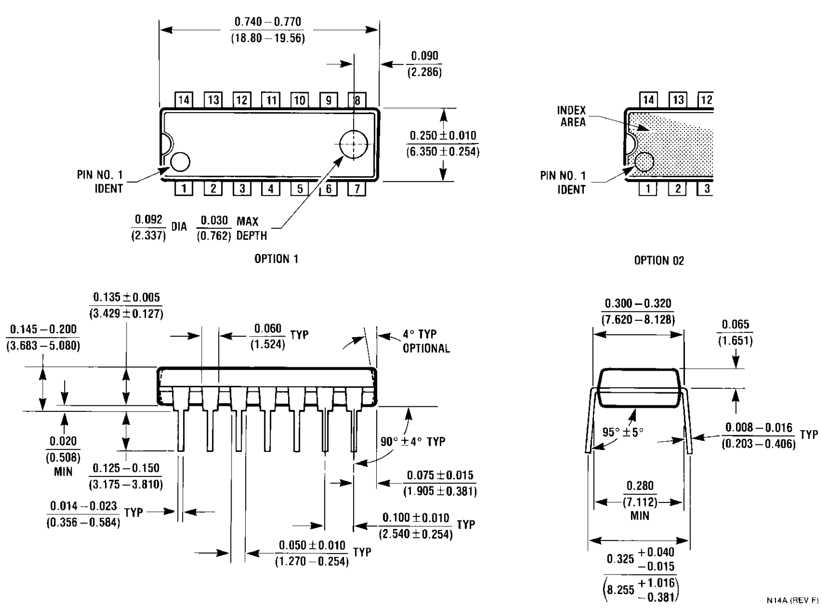


The J and K inputs shown without connection are for reference only and are functionally at a high level.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS90M or DM74LS93M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS90N or DM74LS93N
Package Number N14A

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March 1998

DM74LS90/DM74LS93 Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 'LS90 and divide-by-eight for the 'LS93.

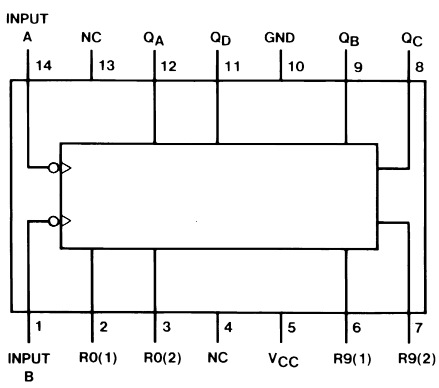
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

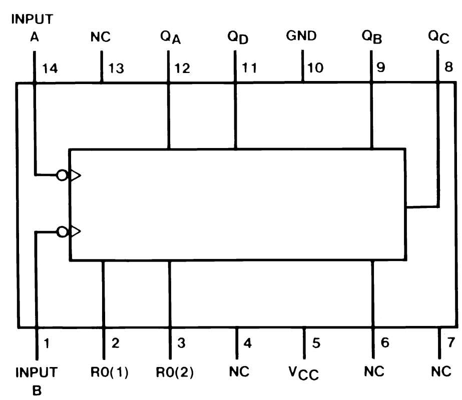
Features

- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagrams (Dual-In-Line Packages)



Order Number DM74LS90M or DM74LS90N
See Package Number M14A or N14A



Order Number DM74LS93M or DM74LS93N
See Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM74LS90			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 3)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 2)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 3)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 2)		25			ns
t_{REL}	Reset Release Time (Note 3)		35			ns
T_A	Free Air Operating Temperature		0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 7)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	

’LS90 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	15	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 7: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS90 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		52	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Recommended Operating Conditions

Symbol	Parameter		DM74LS93 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 8)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 9)	A to Q_A	0		20	
		B to Q_B	0		10	
t_W	Pulse Width (Note 8)	A	15			ns
		B	30			
		Reset	15			
t_W	Pulse Width (Note 9)	A	25			ns
		B	50			
		Reset	25			
t_{REL}	Reset Release Time (Note 8)		25			ns
t_{REL}	Reset Release Time (Note 9)		35			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

’LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 13)			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 11)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 12)			9	15	mA

Note 10: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 13: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

’LS93 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		85	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		90	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Function Tables

LS90
BCD Count Sequence

(Note 14)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
Bi-Quinary (5-2)

(Note 15)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note 14: Output Q_A is connected to input B for BCD count.

Note 15: Output Q_D is connected to input A for bi-quinary count.

Note 16: Output Q_A is connected to input B.

Note 17: H = High Level, L = Low Level, X = Don't Care.

LS93
Count Sequence

(Note 16)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS90
Reset/Count Truth Table

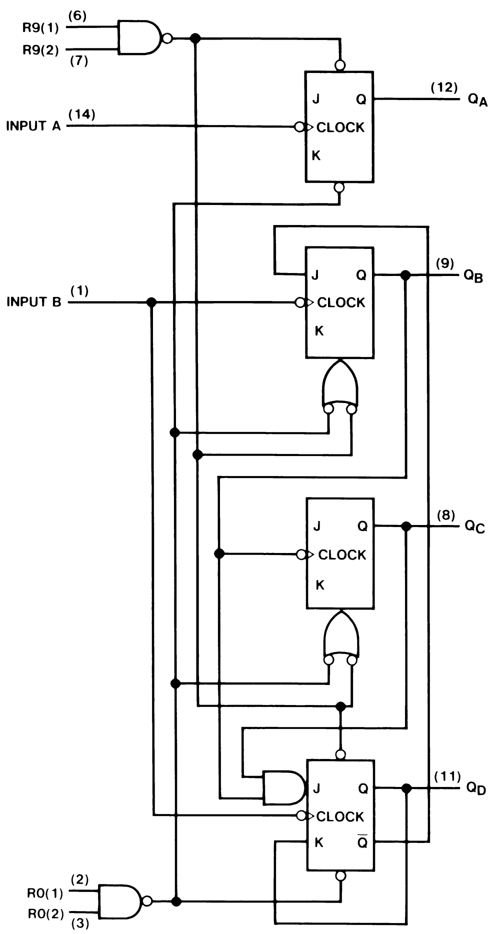
Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Logic Diagrams

LS90



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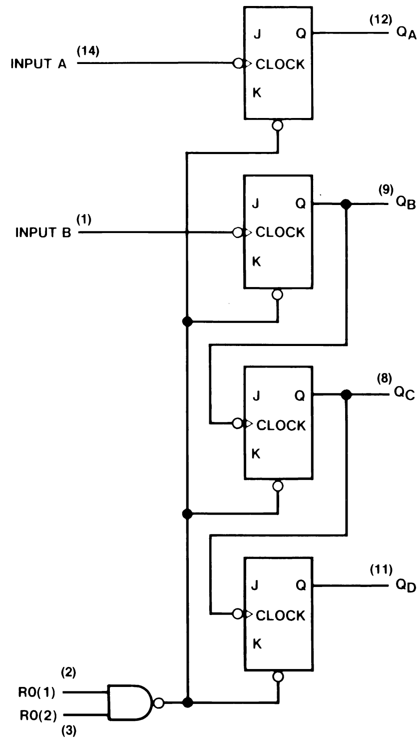
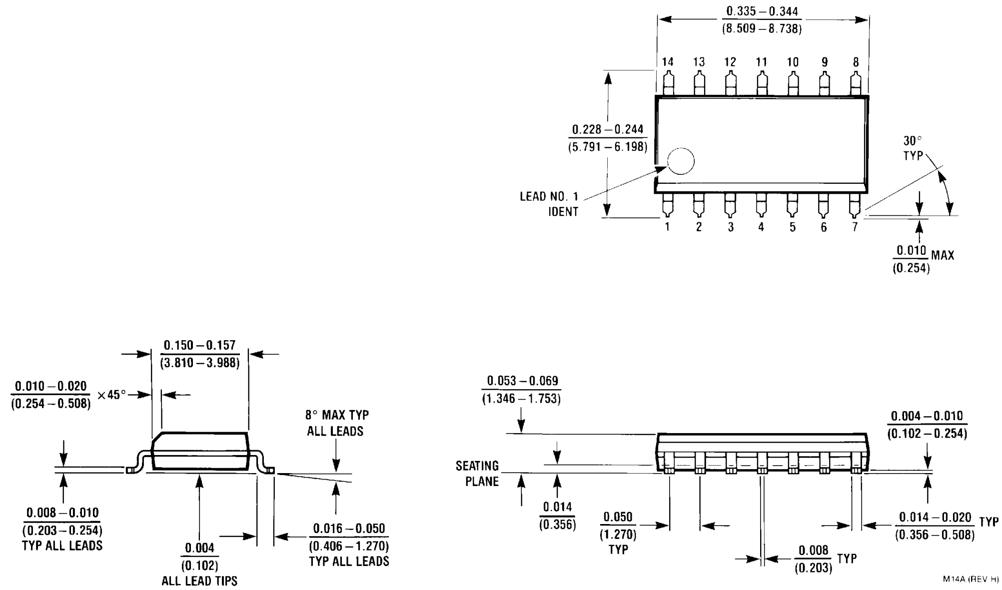
LS93



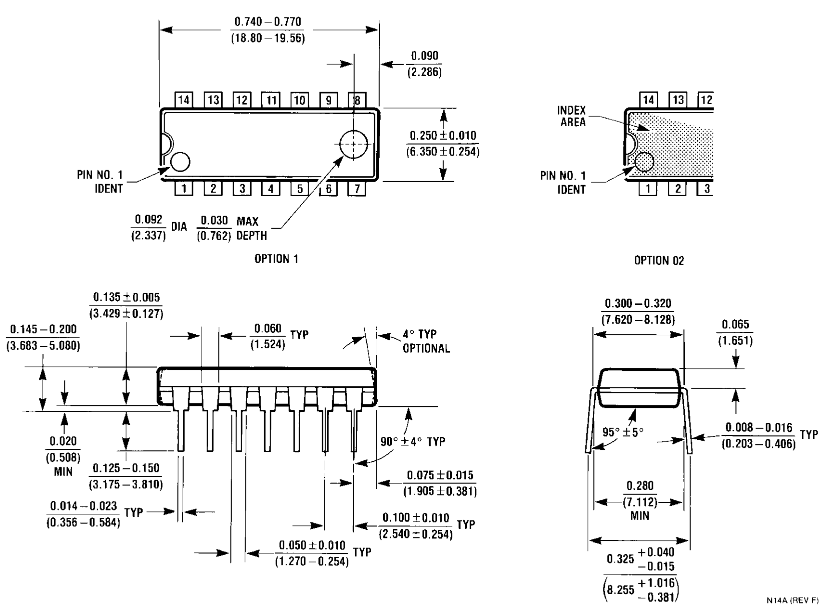
DS006381-4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS90M or DM74LS93M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS90N or DM74LS93N
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

April 1992

DM54LS95B/DM74LS95B 4-Bit Right/Left Shift Register

General Description

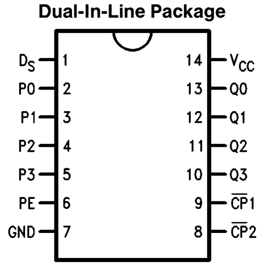
The 'LS95B is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

Features

- Synchronous, expandable shift right
- Synchronous shift left capability
- Synchronous parallel load
- Separate shift and load clock inputs

Connection Diagram

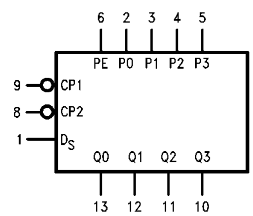
Dual-In-Line Package



TL/F/10175–1

Order Number DM54LS95BJ, DM54LS95BN, DM74LS95BM or DM74LS95BN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



TL/F/10175–2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
$\overline{CP}1$	Serial Clock Input (Active Falling Edge)
$\overline{CP}2$	Parallel Clock Input (Active Falling Edge)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
PE	Parallel Enable Input (Active HIGH)
Q0–Q3	Parallel Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	DM54LS95			DM74LS95			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or Pn to $\overline{CP}$n	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or Pn to $\overline{CP}$n	10 10			10 10			ns
t_w (H)	$\overline{CP}$n Pulse Width HIGH	20			20			ns
t_{en} (L)	Enable Time LOW, PE to $\overline{CP}$1	25			25			ns
t_{inh} (H)	Inhibit Time HIGH, PE to $\overline{CP}$1	20			20			ns
t_{en} (H)	Enable Time HIGH, PE to $\overline{CP}$2	25			25			ns
t_{inh} (L)	Inhibit Time LOW, PE to $\overline{CP}$2	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max, $V_{IL} = $ Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max, $V_{IH} = $ Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 4$ mA, $V_{CC} = $ Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 7V$	DM74			0.1	mA
		$V_I = 10V$	DM54				
	PE Input	$V_{CC} = $ Max, $V_I = 7V$	DM74			200	μA
		$V_I = 10V$	DM54				
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.7V$				20	μA
	PE Input	$V_{CC} = $ Max, $V_I = 2.7V$				40	μA
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.4V$				−0.4	mA
	PE Input	$V_{CC} = $ Max, $V_I = 0.4V$				−0.8	mA
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	$V_{CC} = $ Max				21	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics $V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15$ pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		27	ns
f_{max}	Maximum Shift Frequency	30		MHz

Functional Description

The ’95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P0–P3) Data inputs and four Parallel Data outputs (Q0–Q3). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs, $\overline{CP}1$ and $\overline{CP}2$. The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When PE is HIGH, $\overline{CP}2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}2$ transfers parallel data from the P0–P3 inputs to the Q0–Q3 outputs. When PE is LOW, $\overline{CP}1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}1$ transfers the data from Serial input (D_S) to Q0 and shifts the data in Q0 to Q1, Q1 to Q2, and Q2 to Q3 respectively (right-shift). A left-shift is accomplished by externally connecting Q3 to P2, Q2 to P1, and Q1 to P0, and operating the ’95 in the parallel mode (PE = HIGH). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while $\overline{CP}2$ is HIGH, or changing PE from HIGH to LOW while $\overline{CP}1$ is HIGH and $\overline{CP}2$ is LOW will not cause any changes on the register outputs.

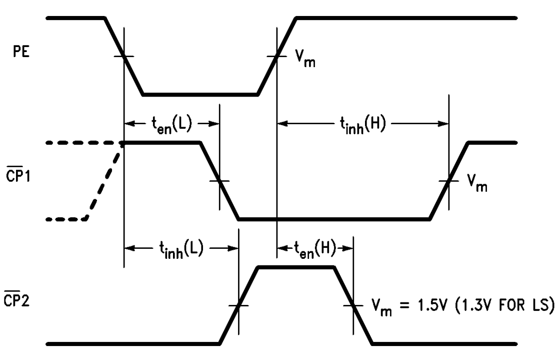
Mode Select Table

Operating Mode	Inputs					Outputs			
	PE	$\overline{CP}1$	$\overline{CP}2$	D_S	Pn	Q0	Q1	Q2	Q3
Shift	L	↓	X	l	X	L	q0	q1	q2
	L	↓	X	h	X	H	q0	q1	q2
Parallel Load	H	X	↓	X	pn	p0	p1	p2	p3
Mode Change	↓	L	L	X	X	No Change			
	↑	L	L	X	X	No Change			
	↓	H	L	X	X	No Change			
	↑	H		X	X	Undetermined			
	↓	L	H	X	X	Undetermined			
	↑	L	H	X	X	No Change			
	↓	H	H	X	X	Undetermined			
	↑	H	H	X	X	No Change			

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

pn = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

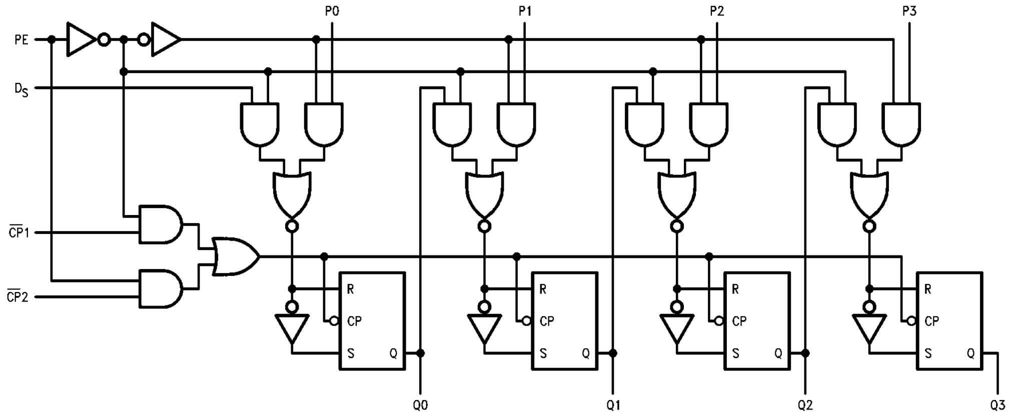
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



TL/F/10175–3

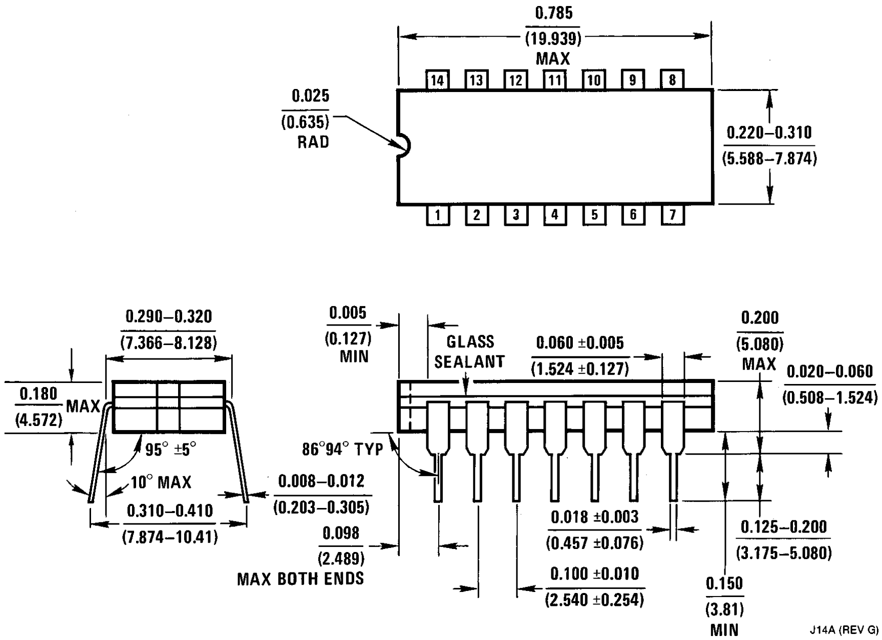
FIGURE A

Logic Diagram



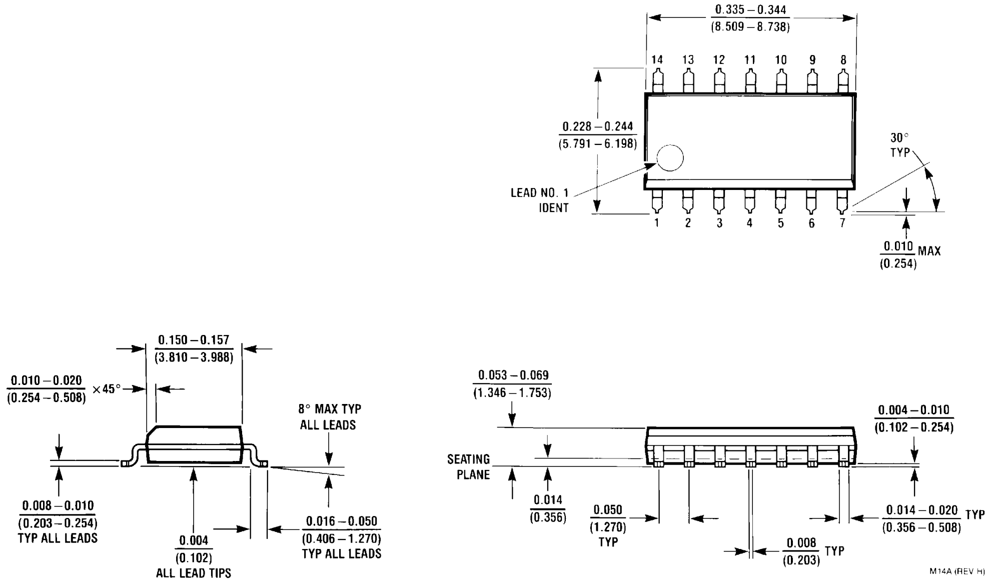
TL/F/10175–4

Physical Dimensions inches (millimeters)

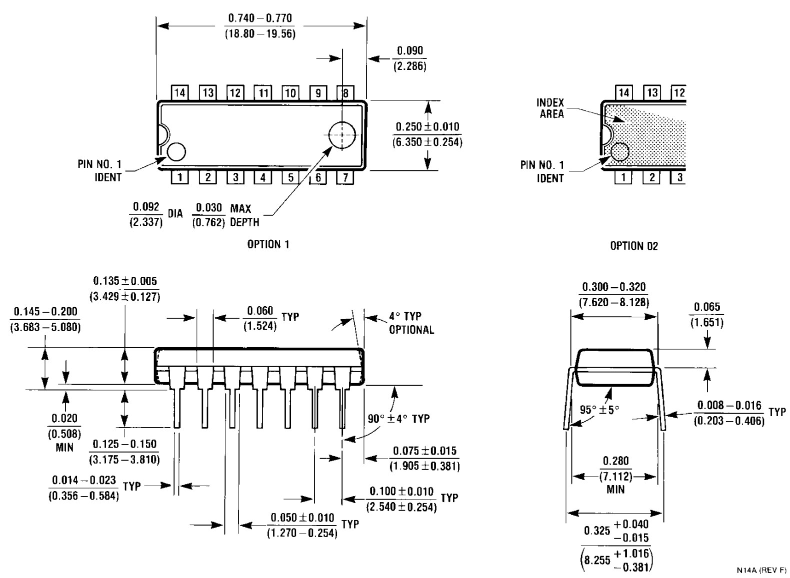


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS95BJ
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

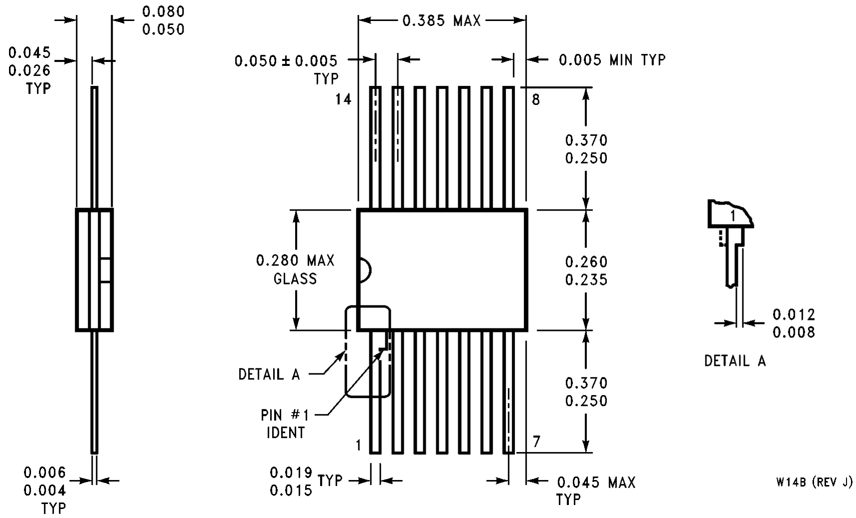


14-Lead Small Outline Molded Package (M)
Order Number DM74LS95BM
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS95BN
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS95BW
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

June 1989

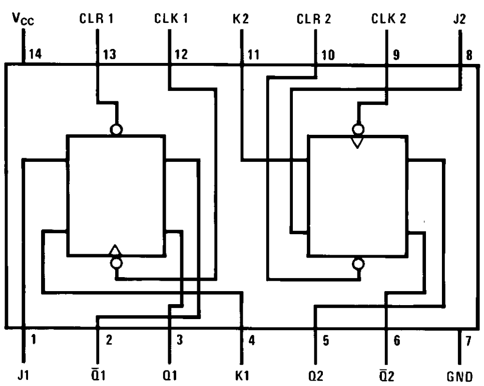
DM54LS107A/DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6367–1

Order Number DM54LS107AJ, DM54LS107AW, DM74LS107AM or DM74LS107AN
See NS Package Number J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS107A			DM74LS107A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 & 2)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 1 & 3)		25↓			25↓			ns
t_H	Hold Time (Notes 1 & 2)		0↓			0↓			ns
t_H	Hold Time (Notes 1 & 3)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

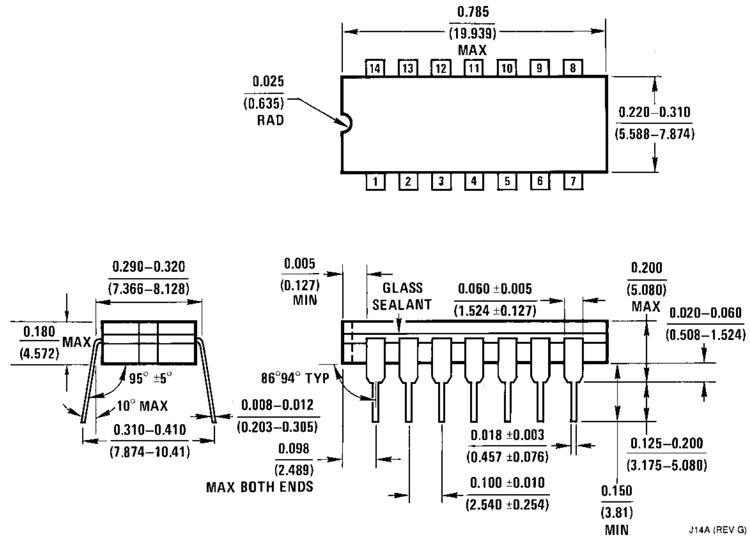
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

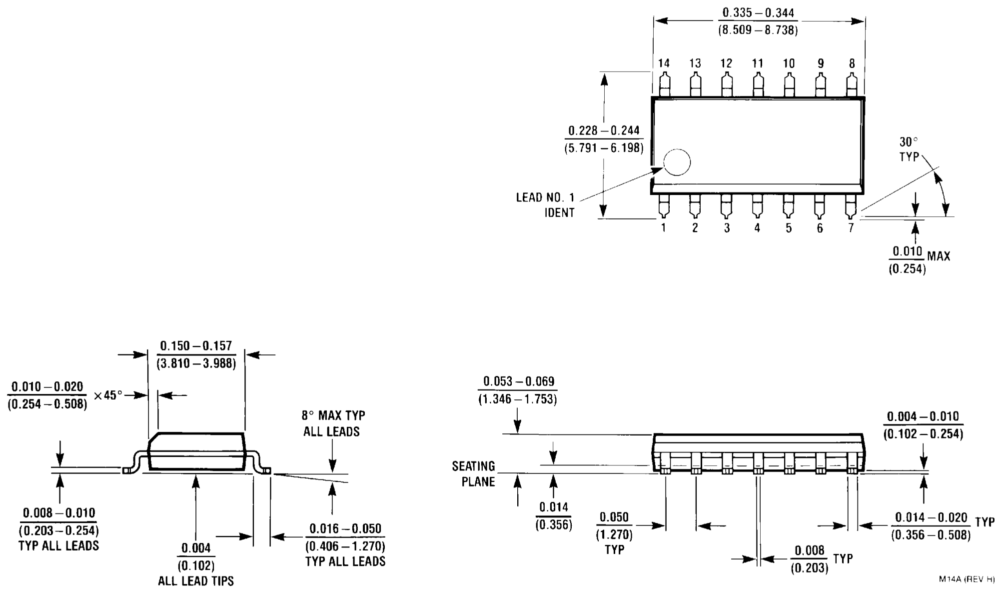
Note 3: With all inputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Physical Dimensions inches (millimeters)

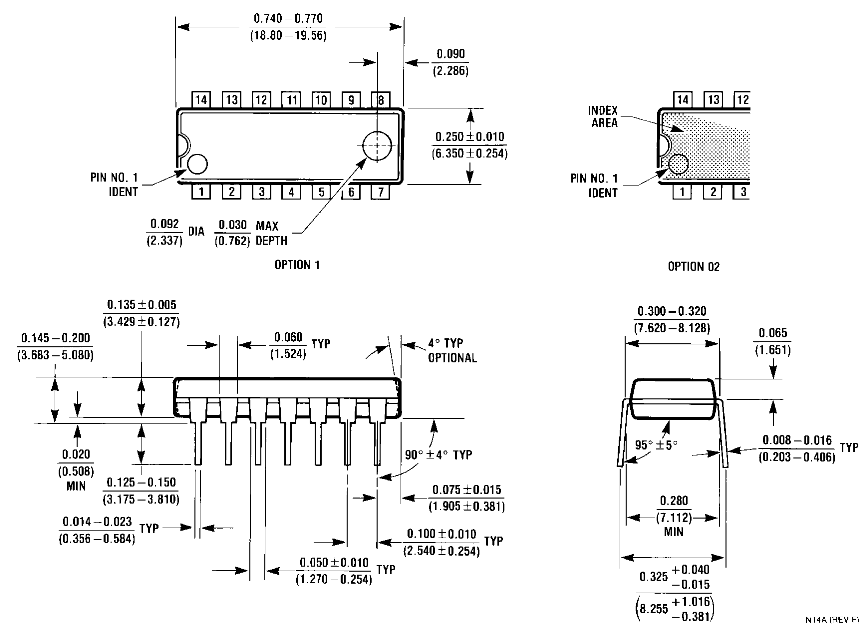


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS107AJ
NS Package Number J14A

Physical Dimensions inches (millimeters) (Continued)

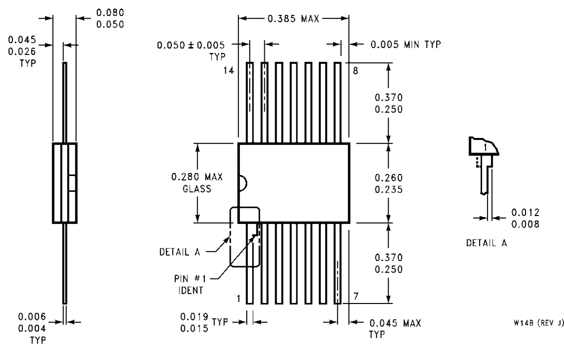


14-Lead Small Outline Molded Package (M)
Order Number DM74LS107AM
NS Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS107AN
NS Package Number N14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Ceramic Flat Package (W)
Order Number DM54LS107AW
NS Package Number W14B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR ™

March 1998

DM74LS109A
Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

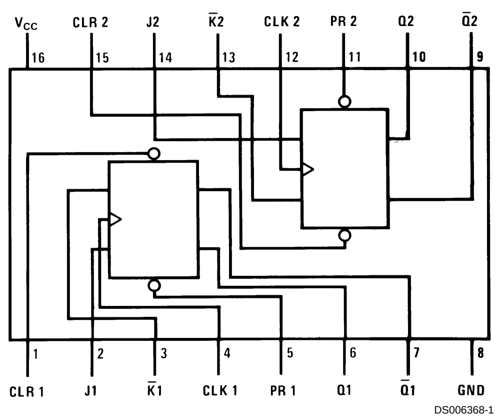
This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS109) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications

Connection Diagram

Dual-In-Line Package



Order Number 54LS109DMQB, 54LS109FMQB, DM54LS109AJ, DM54LS109AW, DM74LS109AM or DM74LS109AN
See Package Number J16A, M16A, N16E or W16A

Function Table

Inputs					Outputs	
PR	**CLR**	**CLK**	**J**	**$\overline{K}$**	**Q**	**$\overline{Q}$**
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↑ = Rising Edge of Pulse

Q_0 = The output logic level of Q before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

 DS006368

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS109A			DM74LS109A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 5)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 5)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 3, 4)	Data High	30↑			30↑			ns
		Data Low	20↑			20↑			
t_{SU}	Setup Time (Notes 3, 5)	Data High	35↑			35↑			ns
		Data Low	25↑			25↑			
t_H	Hold Time (Note 6)		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 4: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 6: T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	J, $\overline{K}$			0.1	mA
		V_I = 7V	Clock			0.1	
			Preset			0.2	
			Clear			0.2	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J,$\overline{K}$			20	μA
			Clock			20	
			Preset			40	
			Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, $\overline{K}$			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 8)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 9)			4	8	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

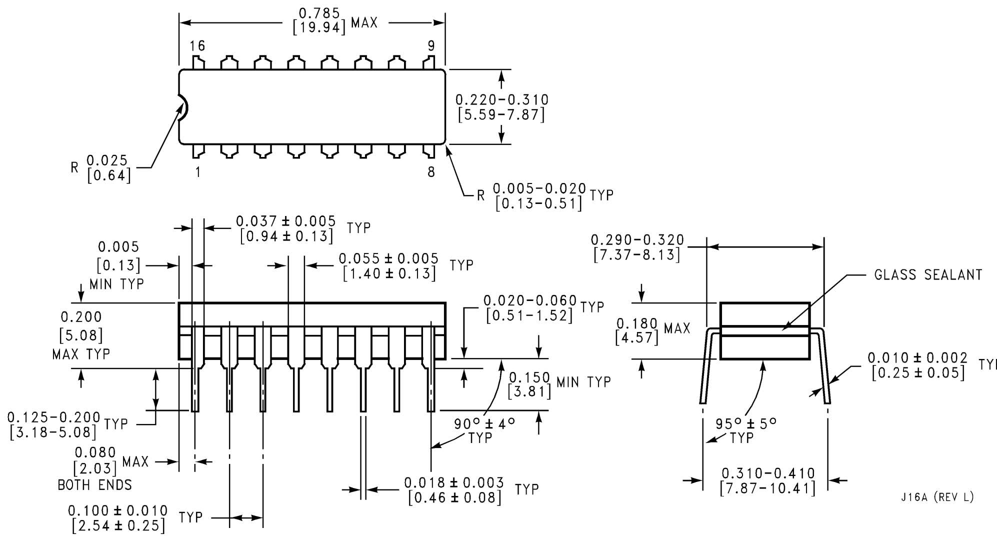
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns

Note 7: All typicals are at V_{CC} = 5V, T_A = 25˚C.

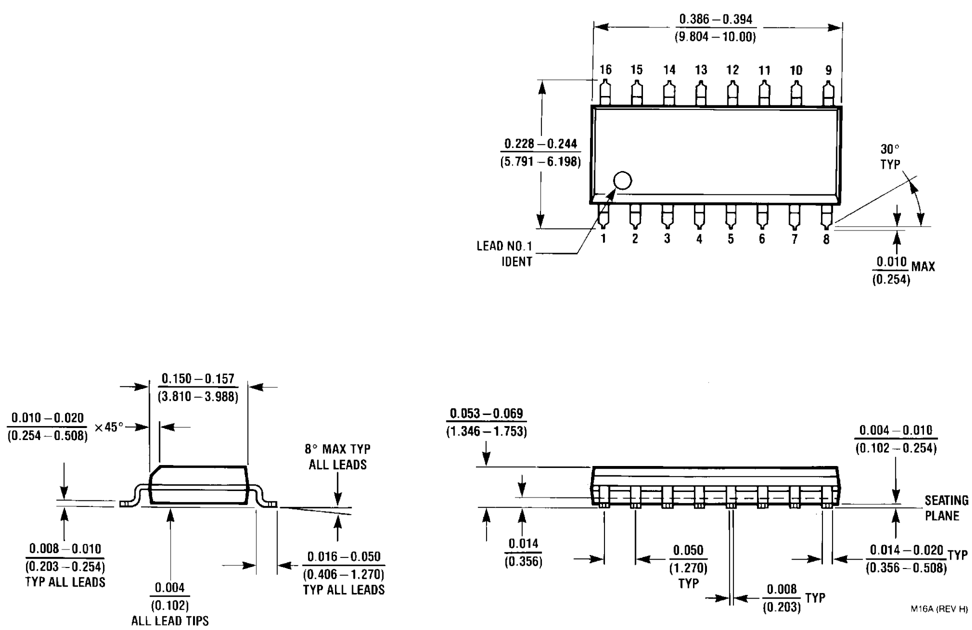
Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 9: I_{CC} is measured with all outputs open, with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Physical Dimensions inches (millimeters) unless otherwise noted

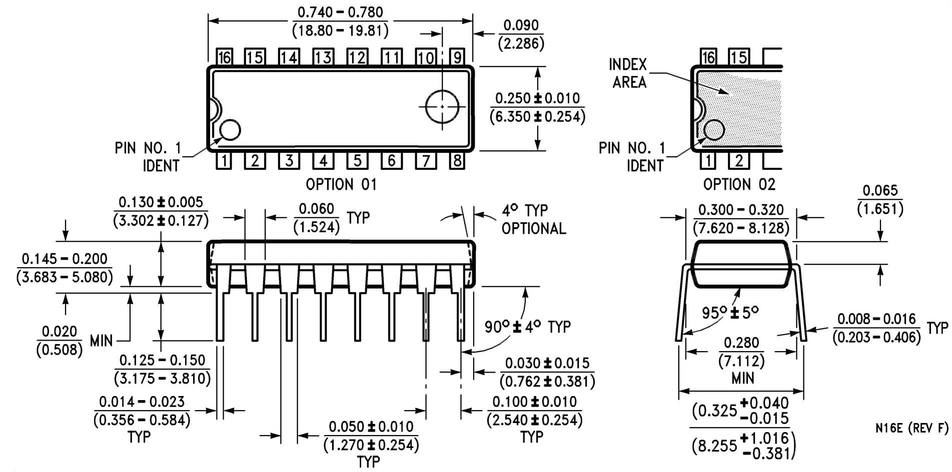


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS109DMQB or DM54LS109AJ
Package Number J16A

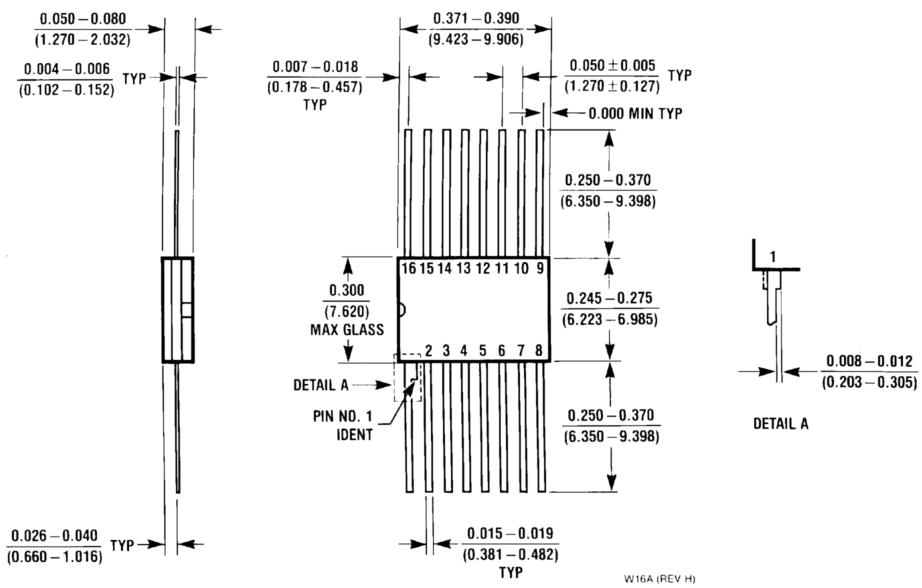


16-Lead Small Outline Molded Package (M)
Order Number DM74LS109AM
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS109AN
Package Number N16E



16-Lead Ceramic Flat Package
Order Number 54LS109FMQB or DM54LS109AW
Package Number W16A

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March 1998

DM74LS112A
Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

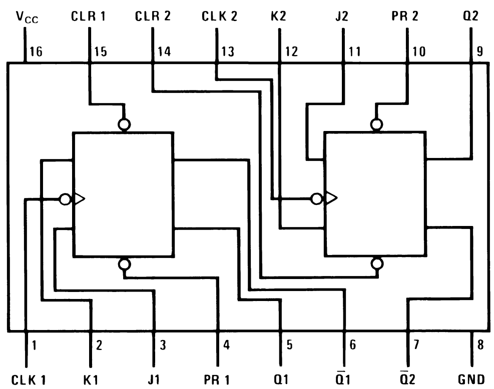
This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Features

- Alternate Military/Aerospace device (54LS112) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006382-1

Order Number 54LS112DMQB, 54LS112FMQB, 54LS112LMQB, DM54LS112AJ, DM54LS112AW, DM74LS112AM or DM74LS112AN
See Package Number E20A, J16A, M16A, N16E or W16A

 DS006382

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H (Note 1)	H (Note 1)
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↓ = Negative Going Edge of Pulse
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Note 1: This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS112A			DM74LS112A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 5)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 5)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 3, 4)		20↓			20↓			ns
t_{SU}	Setup Time (Notes 3, 5)		25↓			25↓			ns
t_H	Hold Time (Notes 3, 4)		0↓			0↓			ns
t_H	Hold Time (Notes 3, 5)		5↓			5↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 3: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 4: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 5: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Preset			60	
			Clock			80	

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 6)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			4	6	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

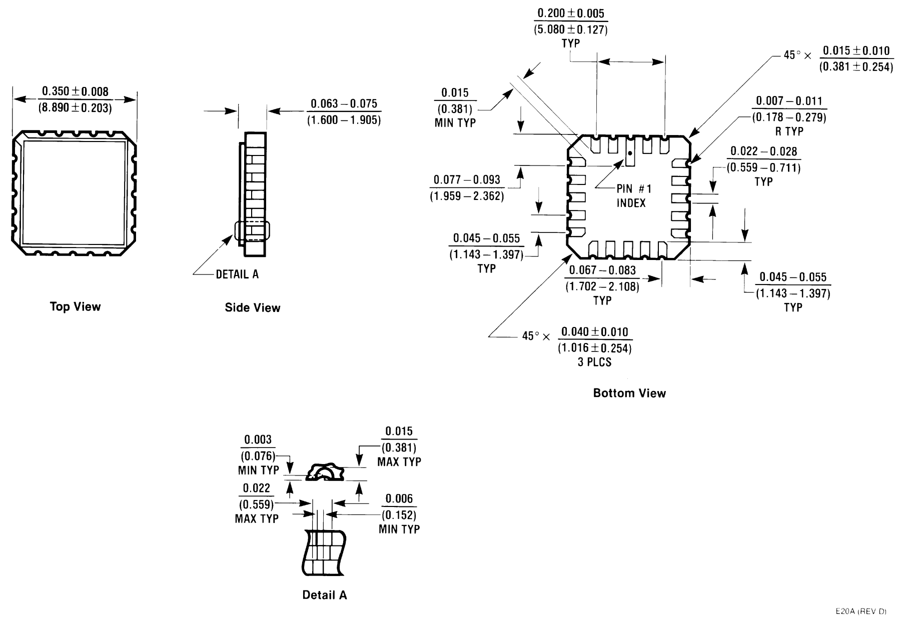
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 6: All typicals are at V_{CC} = 5V, T_A = 25°C.

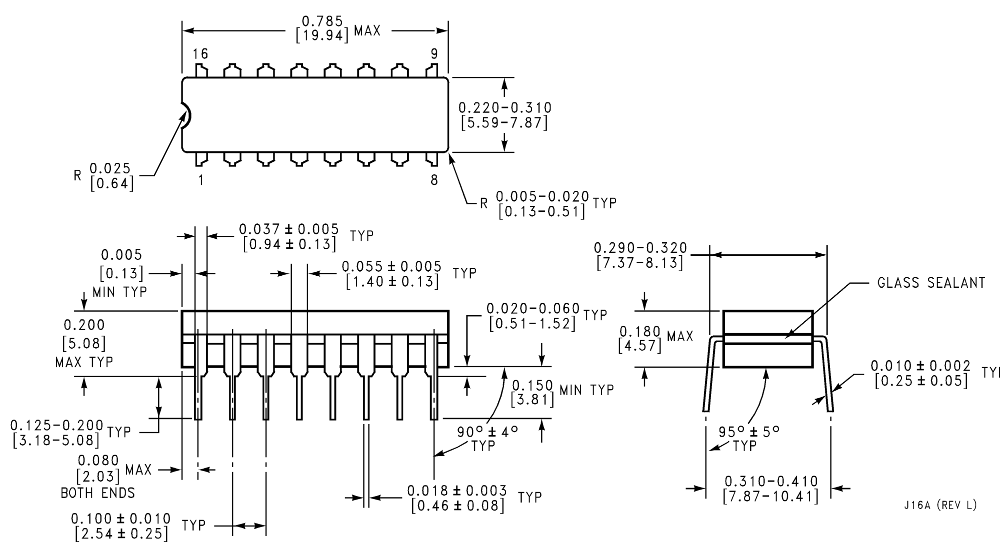
Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 8: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Physical Dimensions inches (millimeters) unless otherwise noted

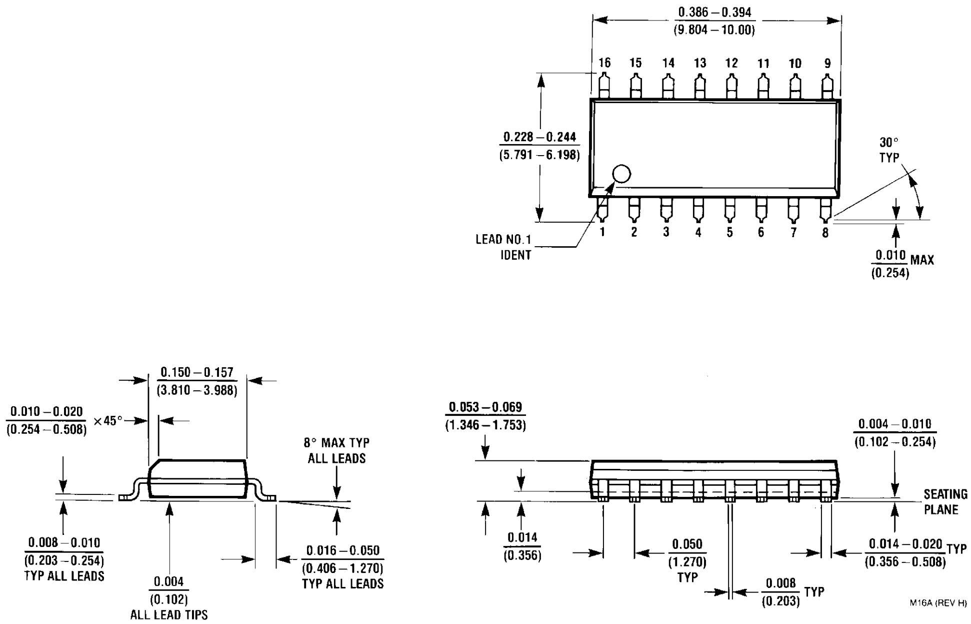


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS112LMQB
Package Number E20A

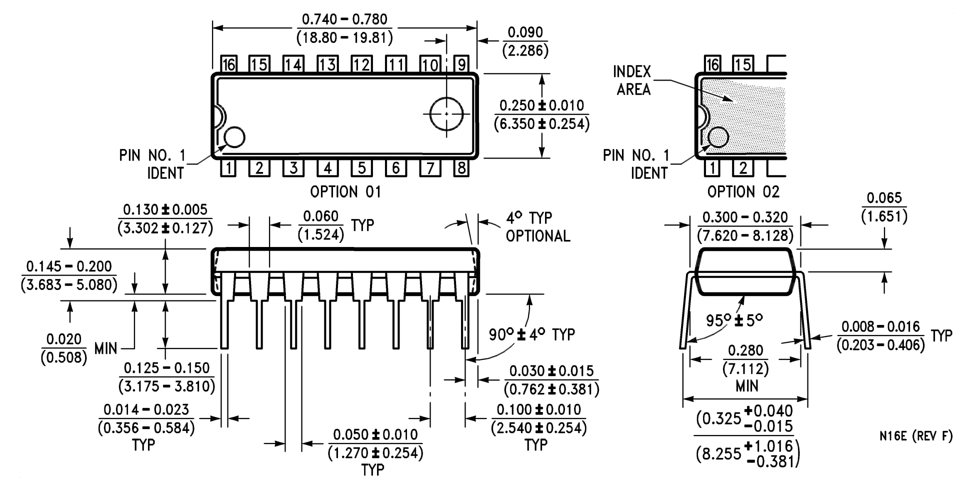


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS112DMQB or DM54LS112AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

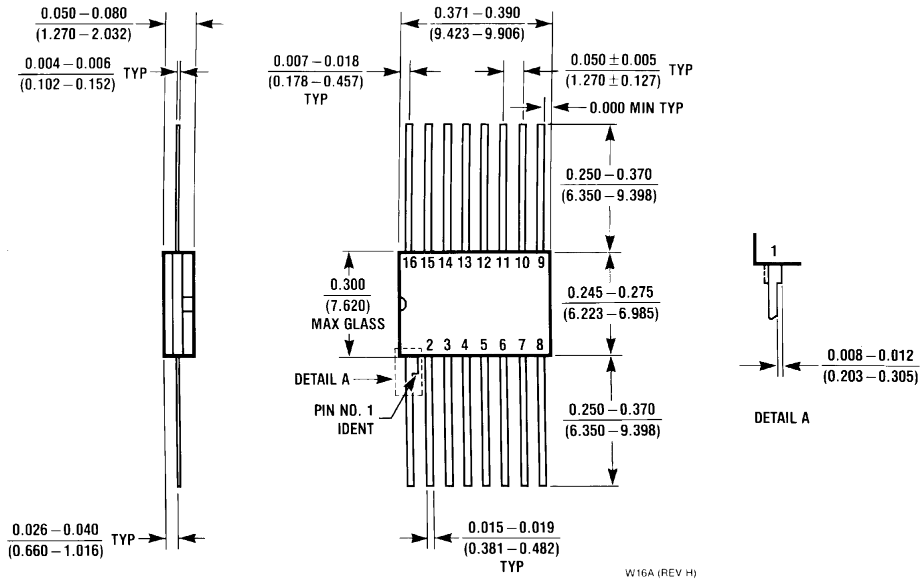


16-Lead Small Outline Molded Package (M)
Order Number DM74LS112AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS112AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS112FMQB or DM54LS112AW
Package Number W16A

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March 1998

DM74LS122
Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS122 is a retriggerable monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 10 kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. The 'LS122 has two active-low transition triggering inputs (A), two active-high transition triggering inputs (B), and a CLEAR input that terminates the output pulse width at a predetermined time independent of the timing components. The clear (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⊔). To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

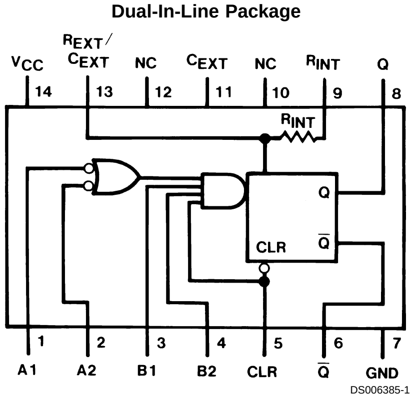
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Over-riding clear terminates output pulse
- Internal 10 kΩ timing resistor
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of the internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered, the output pulse width may be extended by retriggering the gated active-low (A) transition inputs or the active-high transition (B) inputs or the CLEAR input. The output pulse width can be reduced or terminated by overriding it with the active-low CLEAR input.

Connection Diagram

Dual-In-Line Package



Order Number DM74LS122M or DM74LS122N
See Package Number M14A or N14A

Function Table

Inputs					Outputs	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⊓	⊔
H	L	X	H	↑	⊓	⊔
H	X	L	↑	H	⊓	⊔
H	X	L	H	↑	⊓	⊔
H	H	↓	H	H	⊓	⊔
H	↓	↓	H	H	⊓	⊔
H	↓	H	H	H	⊓	⊔
↑	L	X	H	H	⊓	⊔
↑	X	L	H	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameters		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 7)	A or B High	40			ns
		A or B Low	40			
		Clear Low	40			
R_{EXT}	External Timing Resistor		5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50	pF
T_A	Free Air Operating Temperature		0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Notes 4, 5, 6)		6	11	mA

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15 pF, C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns

Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15 pF, C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	µs

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 µF, and R_{EXT} = 25 kΩ.

Note 5: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 µF, and R_{EXT} = 25 kΩ.

Note 6: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Note 7: T_A = 25˚C and V_{CC} = 5V.

Operating Rules

1. To use the internal 10 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (10 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For C_X < 1000 pF see *Figure 1*; design curves on T_W as function of timing components value. For C_X >> 1000 pF the output is defined as:

   $T_W = KR_XC_X$

   where [R_X is in kΩ]
   [C_X is in pF]
   [T_W is in ns]
   K ≈ 0.37

   The K factor is not a constant, but, varies with C_X. See *Figure 2*.
4. The switching diode required for most TTL one-shots when using an electrolytic timing capacitor is not needed for the 'LS122 and should not be used.
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:
6. The retriggerable pulse width is calculated as shown below:

   $$T = T_W + t_{PLH} = 0.50 \times R_X \times C_X + T_{PLH}$$

The retriggered pulse width is equal to the pulse width plus a delay time period (*Figure 4*).

7. Output pulse width variation versus V_{CC} and operation temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}; and *Figure 6* depicts pulse width variation versus temperatures.
8. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (13) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

Operating Rules (Continued)

9. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

Note: For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.

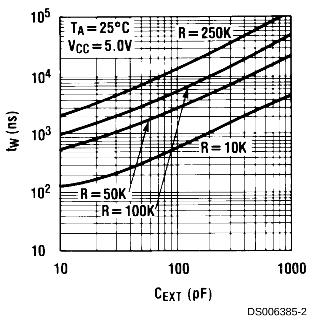


FIGURE 1.

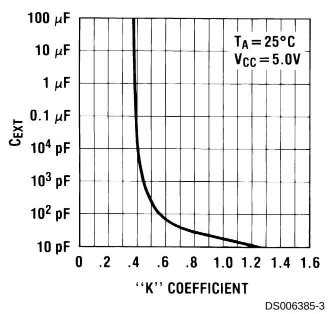
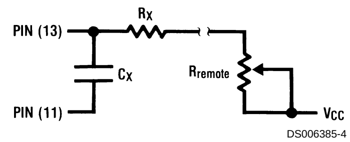


FIGURE 2.



Note: "R_{remote}" should be as close to the device pins as possible.

FIGURE 3.

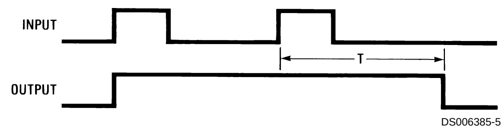


FIGURE 4.

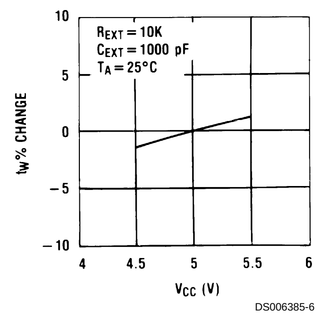


FIGURE 5.

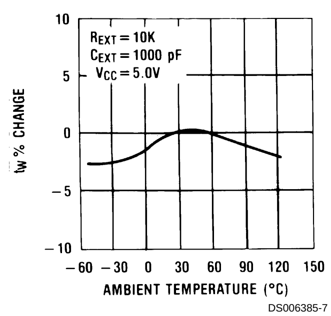
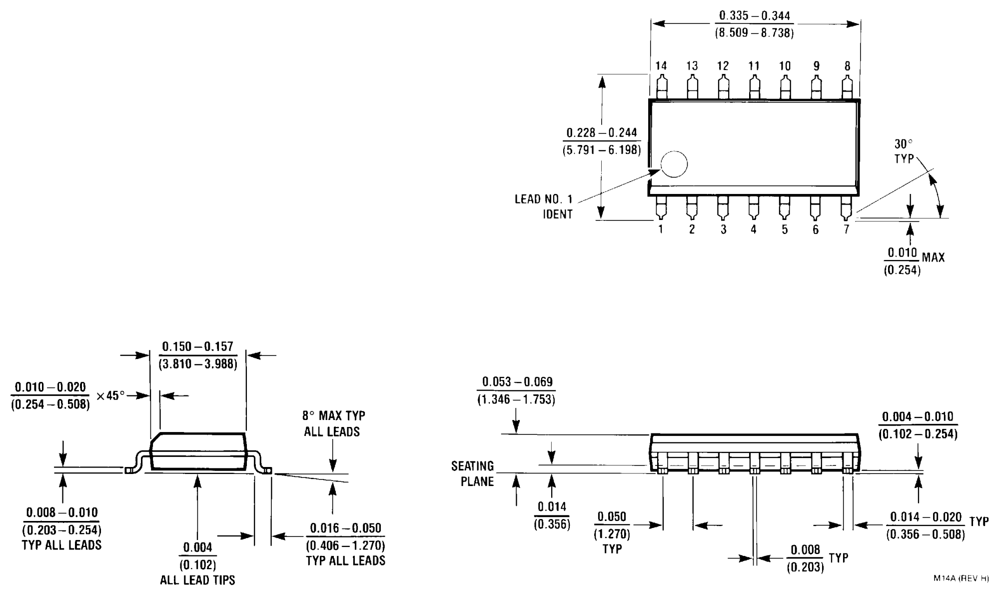
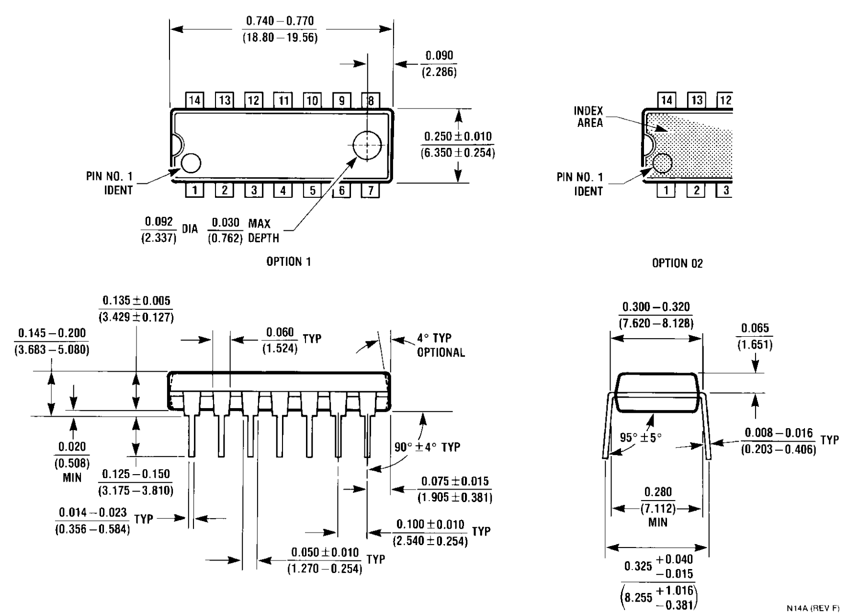


FIGURE 6.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS122M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS122N
Package Number N14A

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March 1998

DM74LS123
Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (⊔). To obtain the best trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

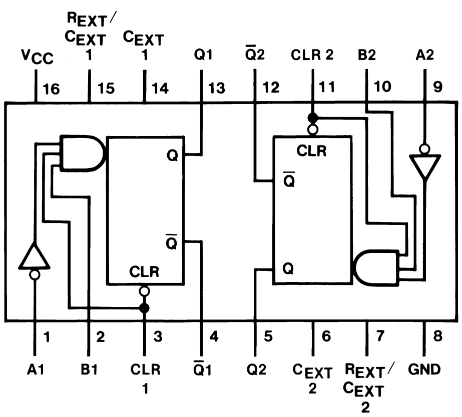
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Compensated for V_{CC} and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low or CLEAR input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram

Dual-In-Line Package



DS006386-1

Order Number DM74LS123M or DM74LS123N
See Package Number M16A or N16E

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑	L	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0˚C to +70˚C
Storage Temperature	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 7)	A or B High	40			ns
		A or B Low	40			
		Clear Low	40			
R_{EXT}	External Timing Resistor		5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			µF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50	pF
T_A	Free Air Operating Temperature		0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Notes 4, 5, 6)		12	20	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 µF, and R_{EXT} = 25 kΩ.

Note 5: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 µF, and R_{EXT} = 25 kΩ.

Note 6: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Note 7: T_A = 25˚C and V_{CC} = 5V.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameters	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15pF, C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	µs

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the ’LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.

   Furthermore, if a polarized timing capacitor is used on the ’LS123 the negative terminal of the capacitor should be connected to the “C_{EXT}” pin of the device (*Figure 1*).

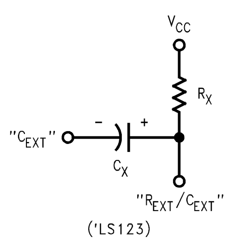


FIGURE 1.

3. For C_X >> 1000 pF the output pulse width (T_W) is defined as follows:

   $T_W = KR_X C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [T_W is in ns]

   $K \approx 0.37$
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

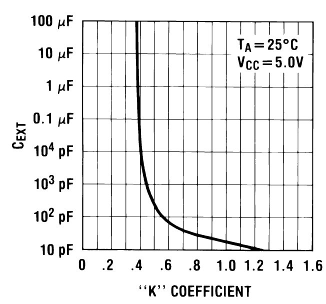


FIGURE 2.

Operating Rules (Continued)

5. For C_X < 1000 pF see *Figure 3* for T_W vs C_X family curves with R_X as a parameter:

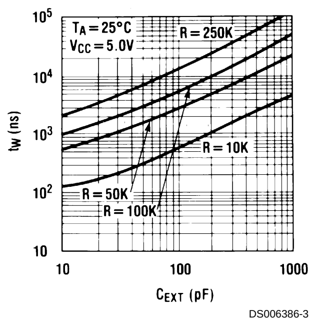


FIGURE 3.

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

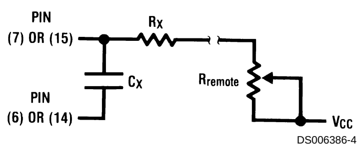


FIGURE 4.

Note: "R_{remote}" should be as close to the device pin as possible.

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

The retriggered pulse width is equal to the pulse width plus a delay time period (*Figure 5*).

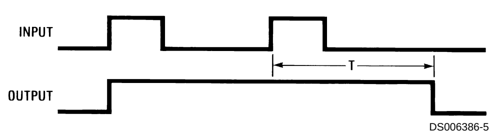


FIGURE 5.

8. Output pulse width variation versus V_{CC} and temperatures: *Figure 6* depicts the relationship between pulse width variation versus V_{CC}, and *Figure 7* depicts pulse width variation versus temperatures.

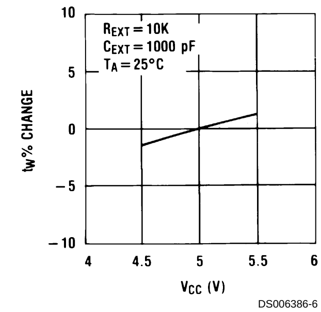


FIGURE 6.

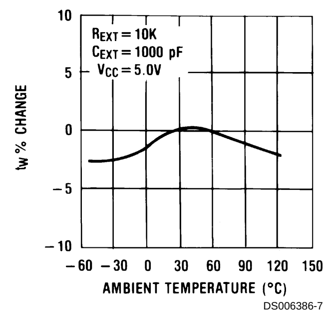


FIGURE 7.

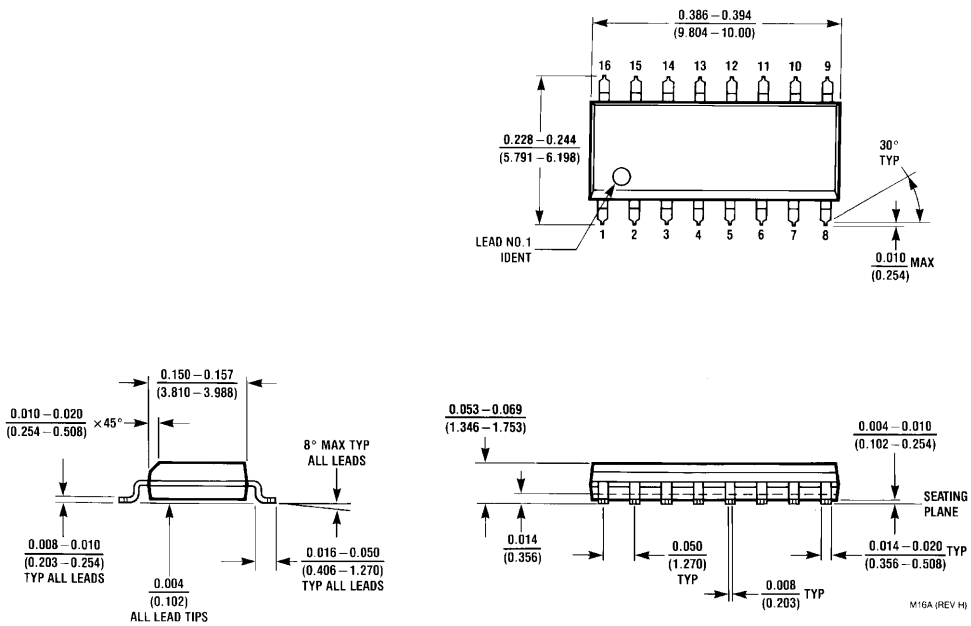
9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.

10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.

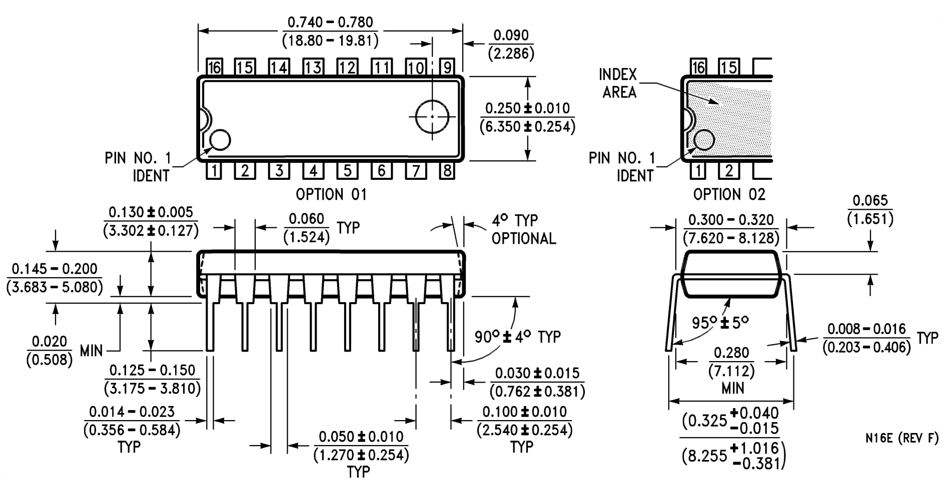
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

Note: For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-372.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Molded Package
Order Number DM74LS123M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS123N
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS125A
Quad 3-STATE Buffers

General Description

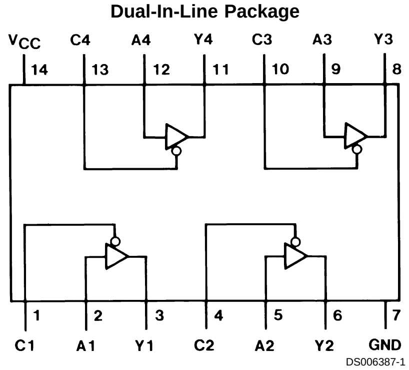
This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS125) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS125ADMQB, 54LS125AFMQB, 54LS125ALMQB, DM54LS125AJ, DM54LS125AW, DM74LS125AM or DM74LS125AN
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Y = A

Inputs		Output
A	**C**	**Y**
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range

DM54LS and 54LS −55°C to +125°C

DM74LS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS125A			DM74LS125A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			11	20	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with the data control (C) inputs at 4.5V and the data inputs grounded.

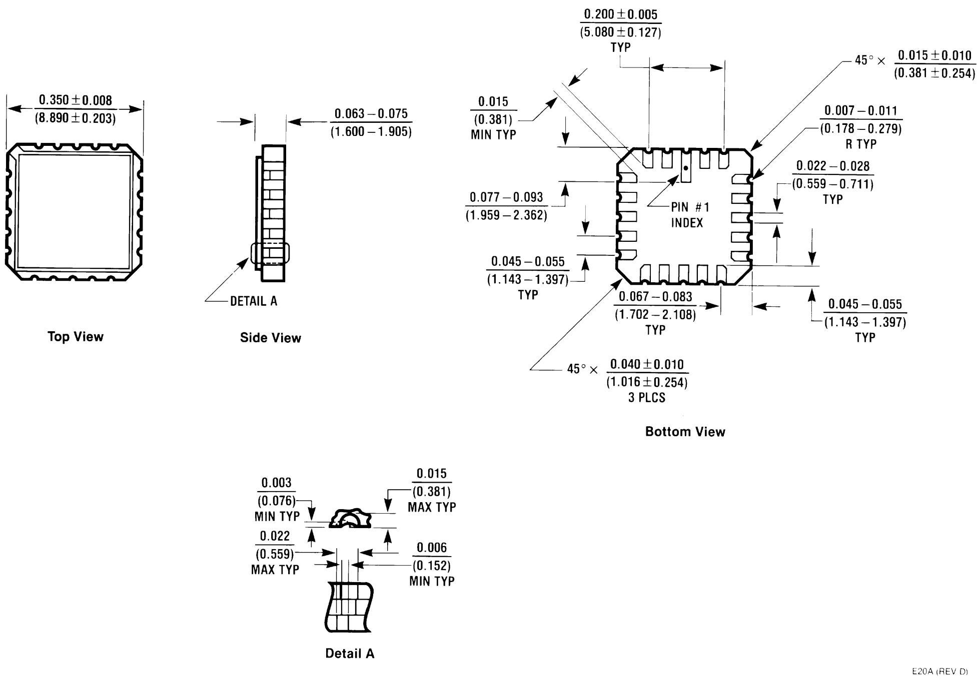
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

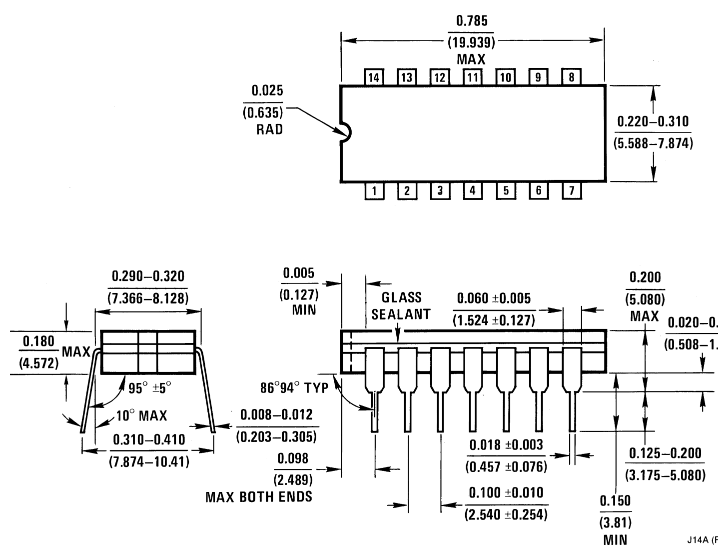
Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		25		35	ns
t_{PZL}	Output Enable Time to Low Level Output		25		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 5)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 5)		20			ns

Note 5: C_L = 5pF.

Physical Dimensions inches (millimeters) unless otherwise noted

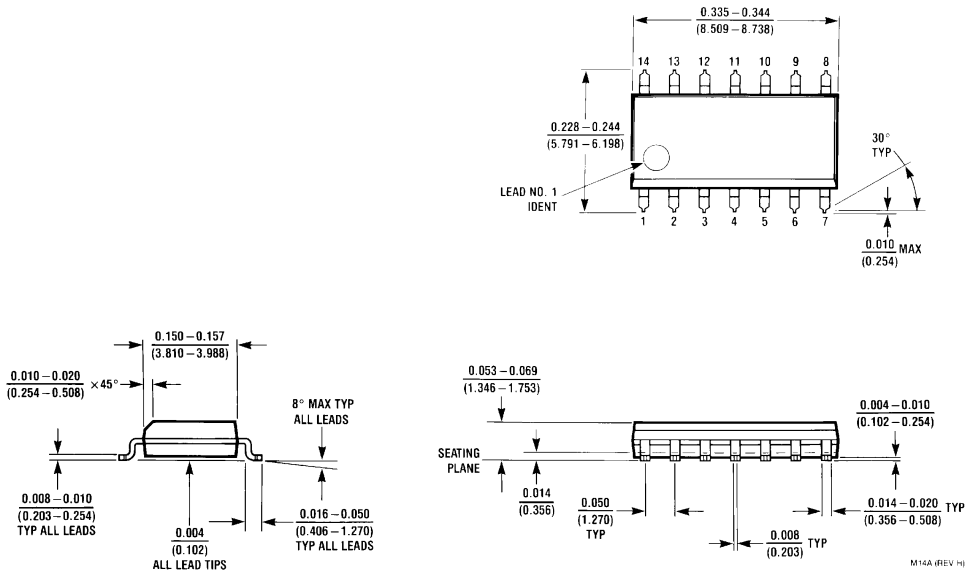


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS125ALMQB
Package Number E20A

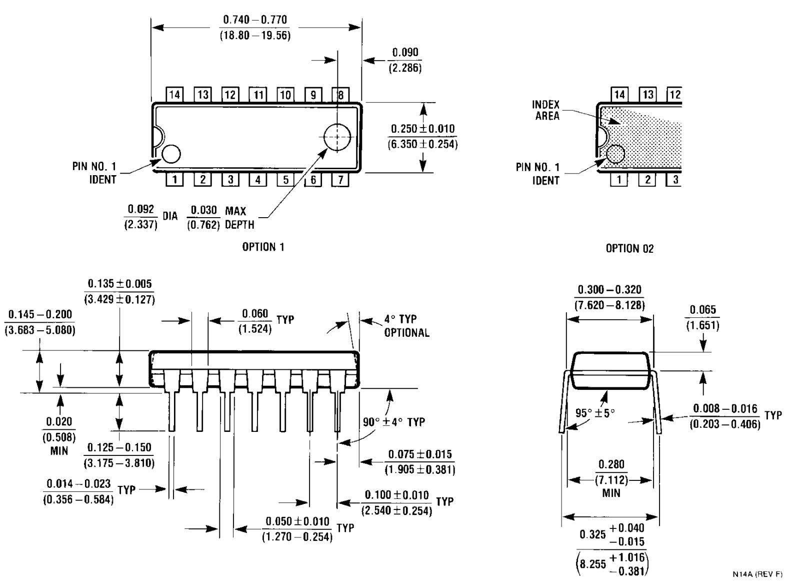


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS125ADMQB or DM54LS125AJ
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

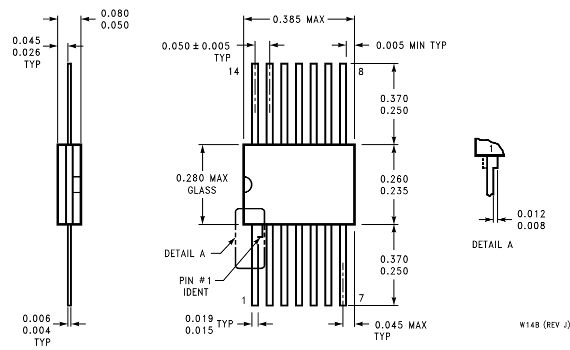


14-Lead Small Outline Molded Package (M)
Order Number DM74LS125AM
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS125AN
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS125AFMQB or DM54LS125AW
Package Number W14B

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FAIRCHILD SEMICONDUCTOR™

March 1998

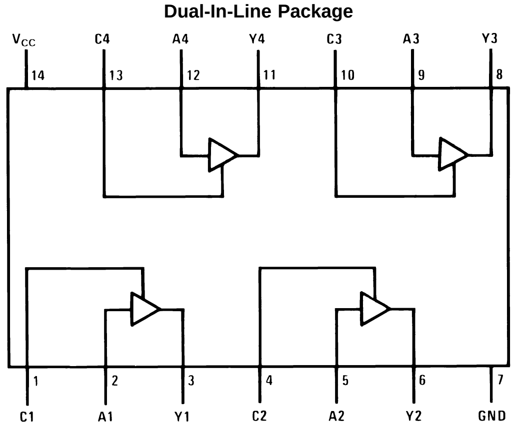
DM74LS126A Quad 3-STATE Buffer

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



DS006388-1

Order Number DM74LS126AM or DM74LS126AN
See Package Number M14A or N14A

Function Table

Y = A

Inputs		Output
A	**C**	**Y**
L	H	L
H	H	H
X	L	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage				V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 12 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max		12	22	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

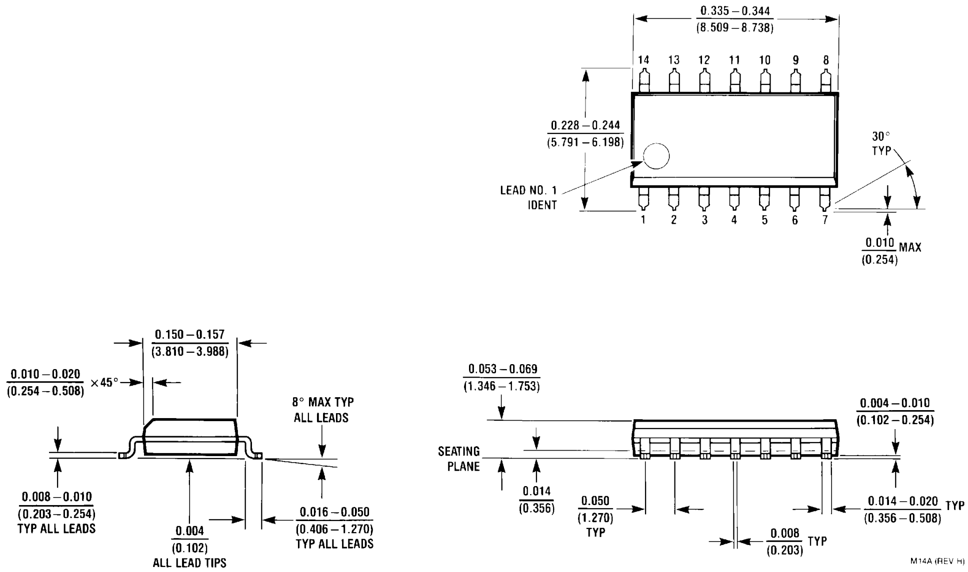
Switching Characteristics:

for test waveforms and output load. V_{CC} = 5V, T_A = 25˚C

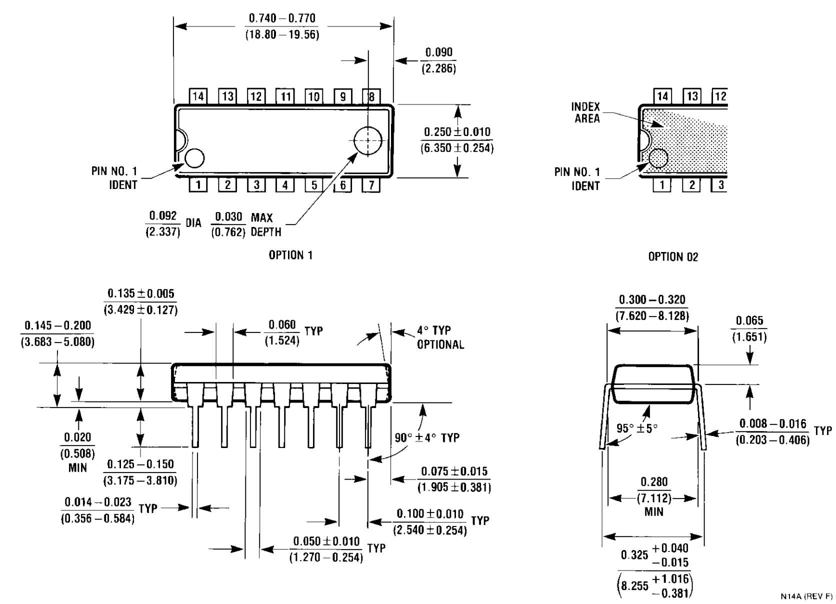
Symbol	Parameter	DM74LS				Units
		R_L = 667Ω				
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		30		36	ns
t_{PZL}	Output Enable Time to Low Level Output		30		42	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)		25			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)		25			ns

Note 4: C_L = 5pF.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS126AM
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS126AN
Package Number N14A

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March 1998

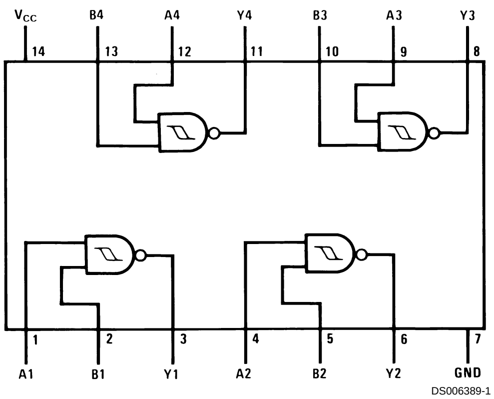
DM74LS132
Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS132J, DM54LS132W, DM74LS132M or DM74LS132N
See Package Number J14A, M14A, N14A or W14B

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS132			DM74LS132			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 2)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 2)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 2)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, $V_I = V_{T-}$ Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, $V_I = V_{T+}$ Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, $V_I = V_{T+}$			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, $V_I = V_{T-}$			−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5.9	11	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.2	14	mA

Note 2: V_{CC} = 5V

Note 3: All typicals are at V_{CC} = 5V, T_A = 25˚C.

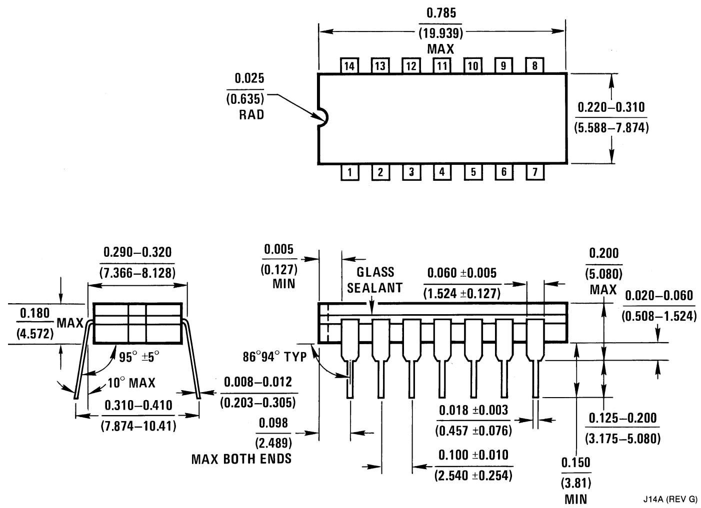
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

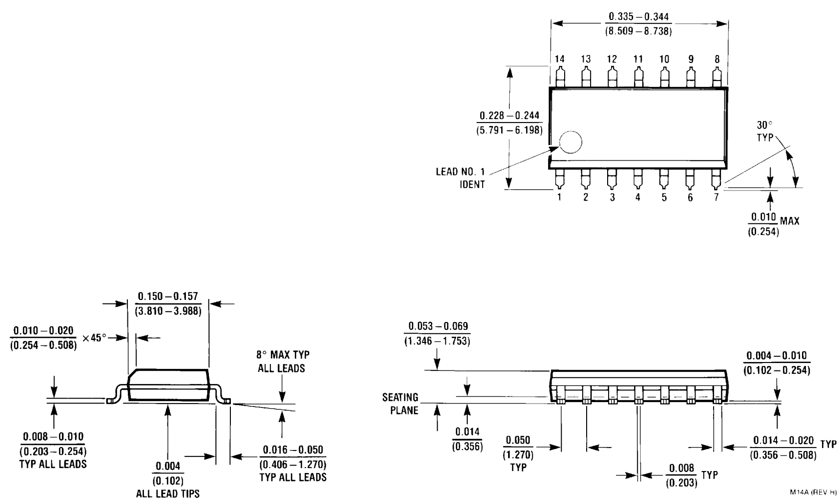
at V_{CC} 5V and T_A = 25˚C

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

Physical Dimensions inches (millimeters) unless otherwise noted

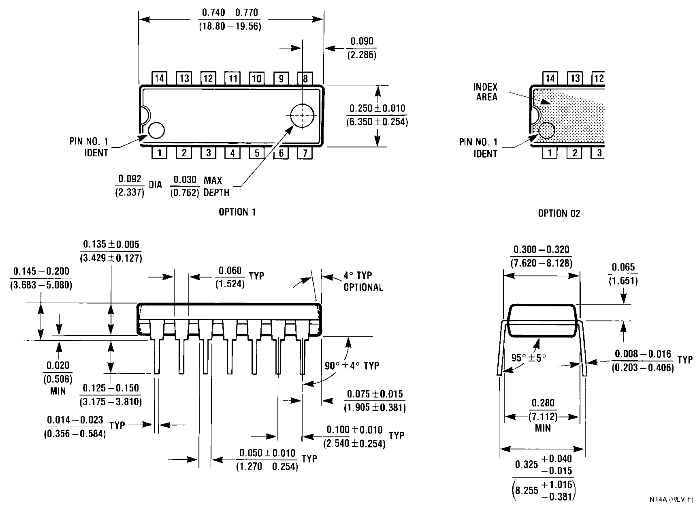


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS132J
Package Number J14A

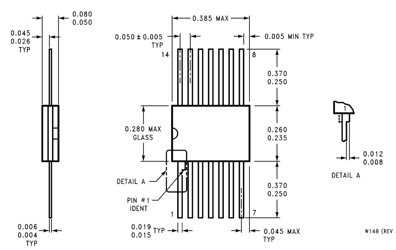


14-Lead Small Outline Molded Package (M)
Order Number DM74LS132M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS132N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS132W
Package Number W14B

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National Semiconductor

May 1992

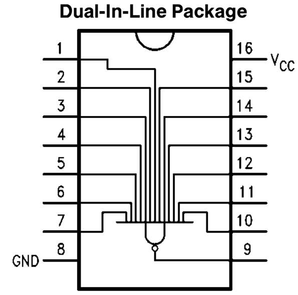
DM54LS133/DM74LS133 13-Input NAND Gate

General Description

This device contains one, 13-input gate that performs the logic NAND functions.

Connection Diagram

Dual-In-Line Package



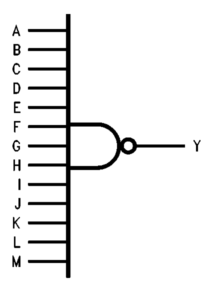
TL/F/9818–1

Order Number DM54LS133E, DM54LS133J, DM54LS133N, DM74LS133M or DM74LS133N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs A through M	Output Y
All Inputs H	L
One or More Inputs L	H

Logic Diagram



TL/F/9818–2

POSITIVE LOGIC

$Y = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H \bullet I \bullet J \bullet K \bullet L \bullet M}$ or

$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H} + \overline{I} + \overline{J} + \overline{K} + \overline{L} + \overline{M}$

 TL/F/9818 RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for acutal device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS133			DM74LS133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				0.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				1.1	mA

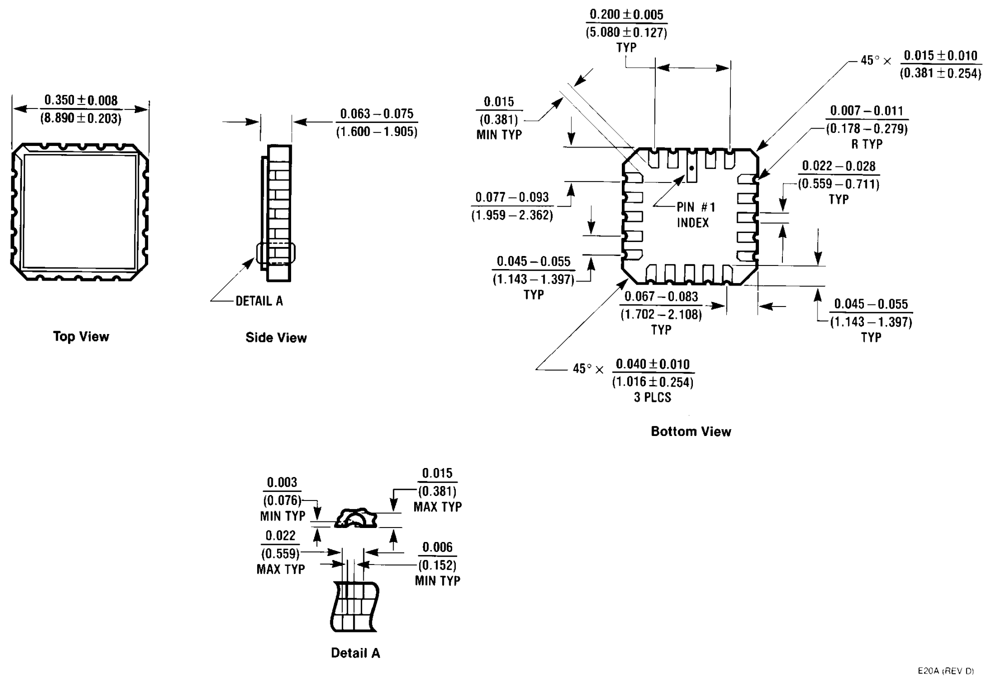
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

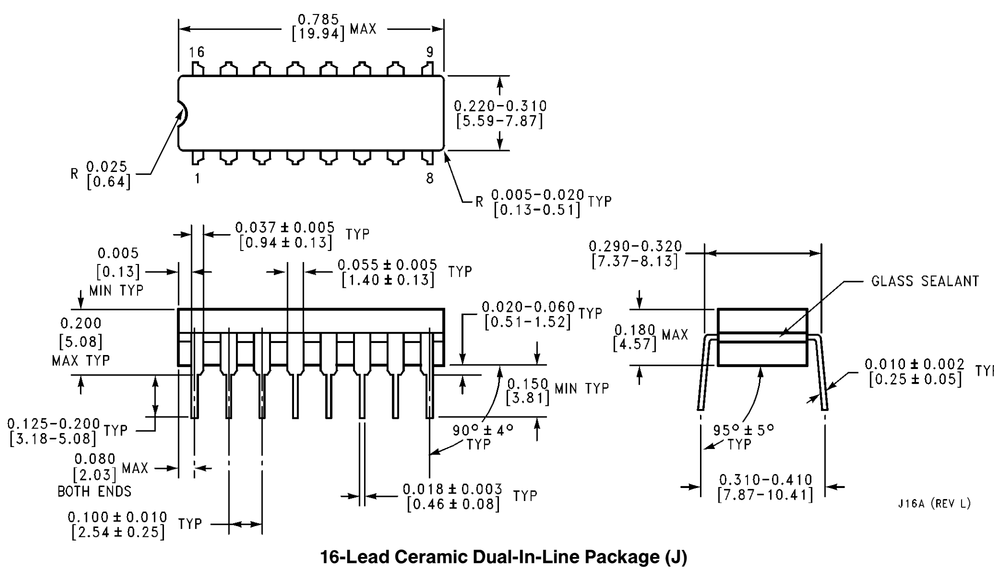
Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		38	ns

Physical Dimensions inches (millimeters)

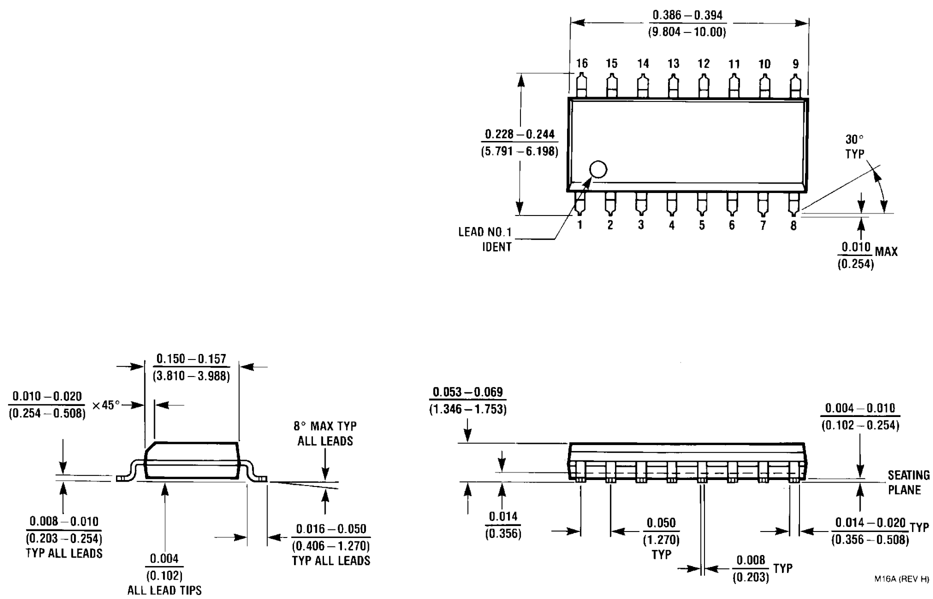


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS133E
NS Package Number E20A

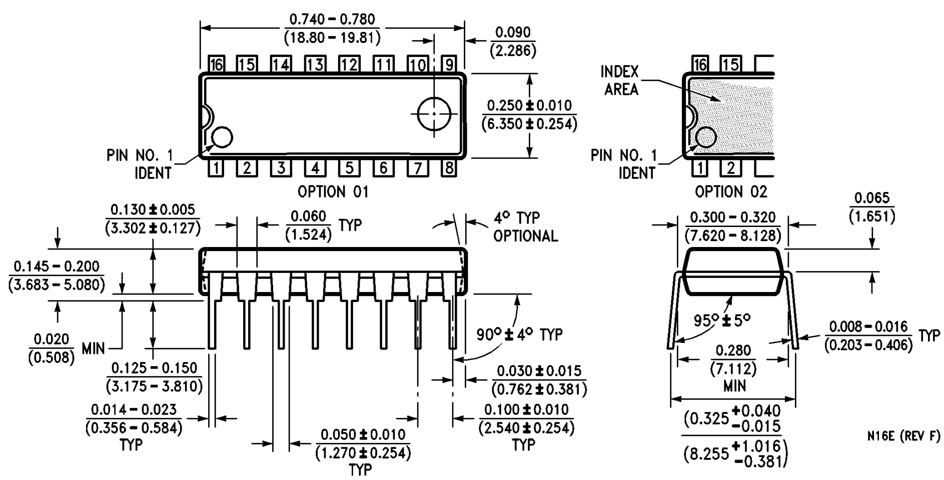


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS133J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

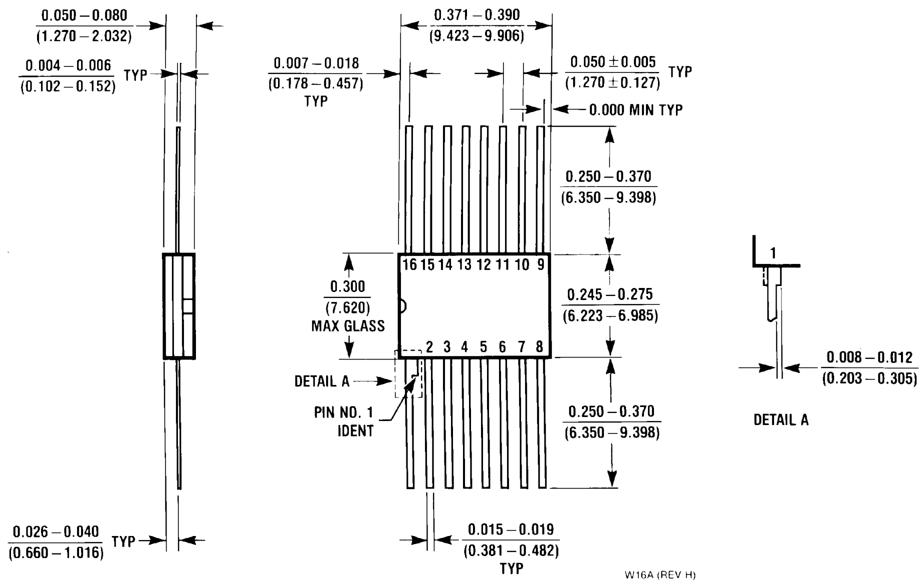


16-Lead Small Outline Molded Package (M)
Order Number DM74LS133M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS133N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS133W
NS Package Number W16A

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FAIRCHILD SEMICONDUCTOR™

March 1998

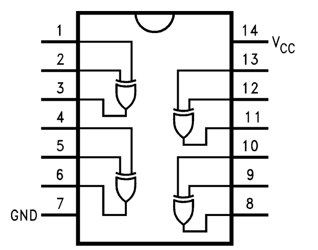
DM74LS136
Quad 2-Input Exclusive-OR Gate with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



DS009819-1

Order Number DM74LS136M or DM74LS136N
See Package Number M14A or N14A

Truth Table

Inputs		Output
A	**B**	**Z**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Leve

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V			100	µA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.6	mA
I_{CC}	Supply Current	V_{CC} = Max			10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

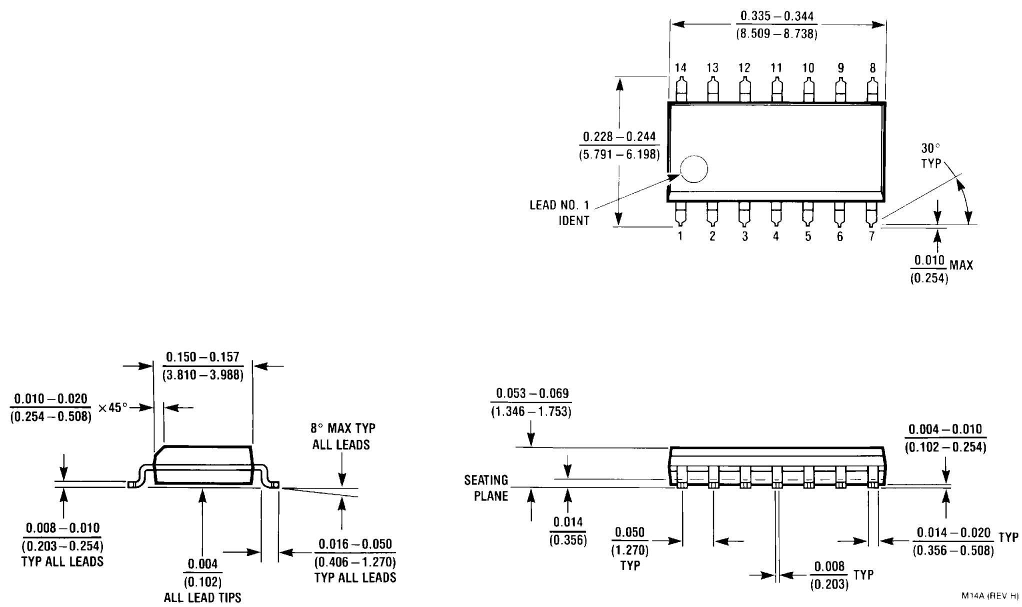
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

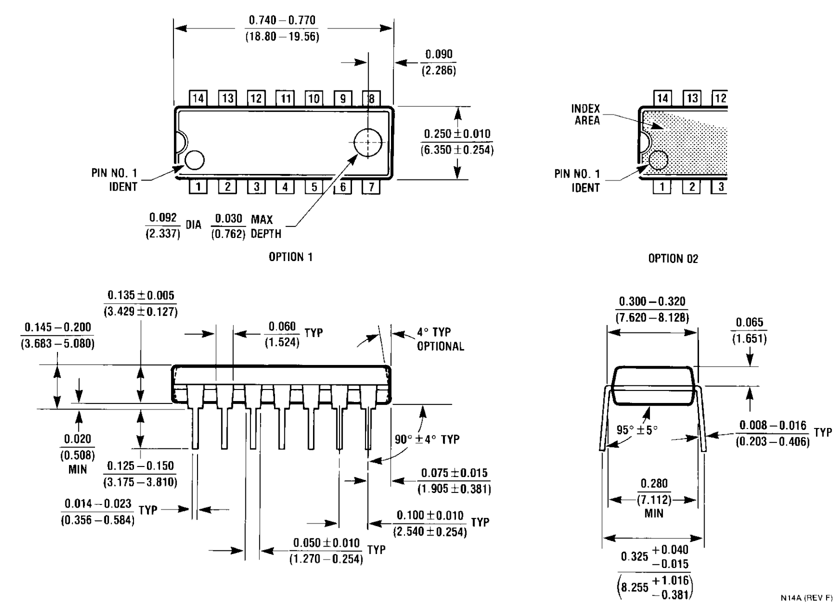
at V_{CC} = 5V and T_A = 25˚C (for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		23	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS136M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS136N
Package Number N14A

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March 1998

DM74LS138, DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

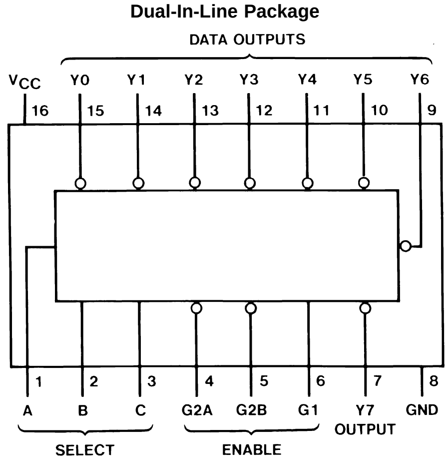
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

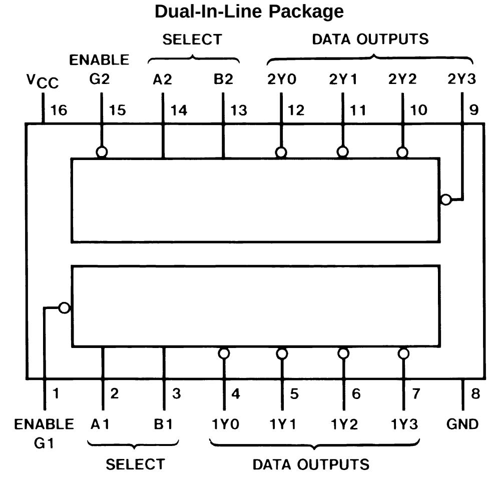
Connection Diagrams

Dual-In-Line Package



Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See Package Number E20A, J16A, M16A, N16E or W16A
Dual-in-Line Package

Dual-In-Line Package



Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			6.3	10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		18		27	ns

'LS138 Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		28		40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139			DM74LS139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

'LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			6.8	11	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 8)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Note 8: G2 = G2A + G2B

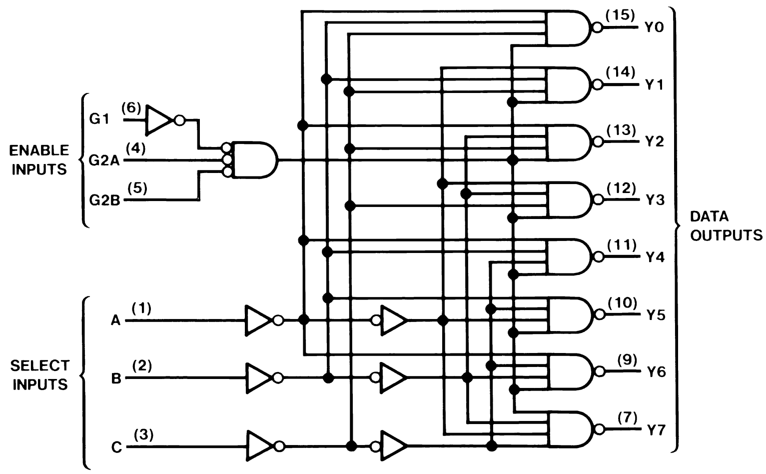
LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Logic Diagrams

LS138



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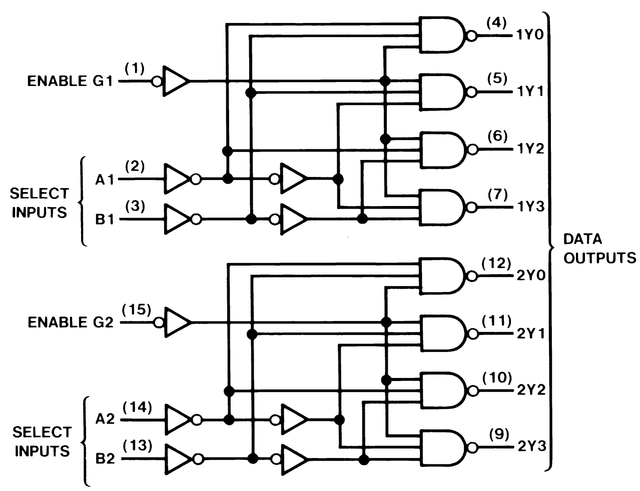
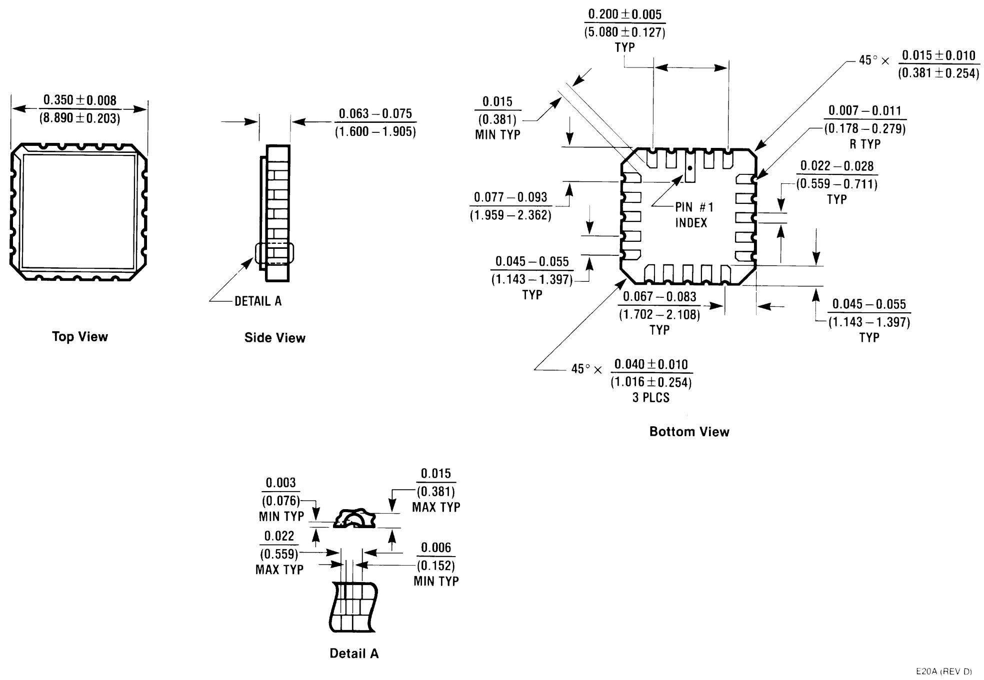
LS139

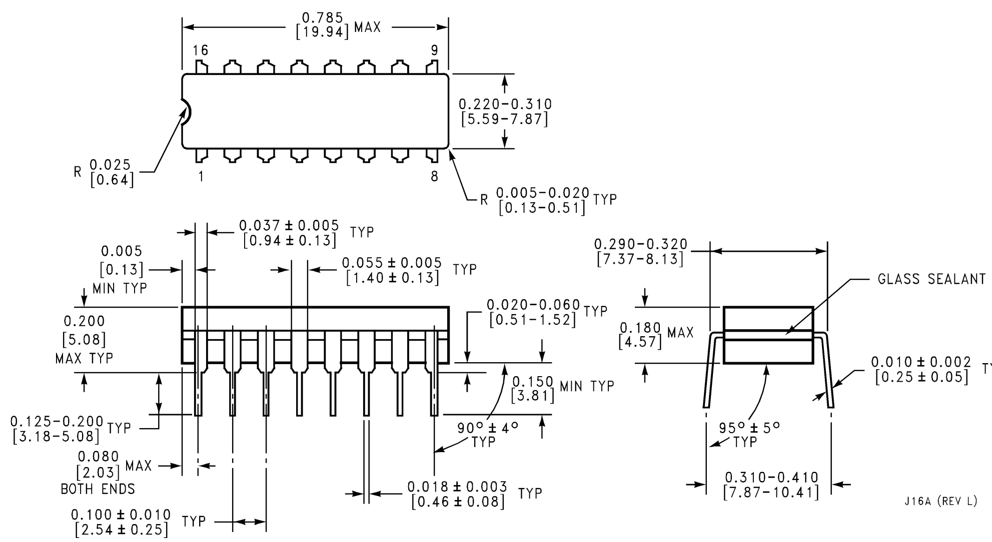


DS006391-4

Physical Dimensions inches (millimeters) unless otherwise noted

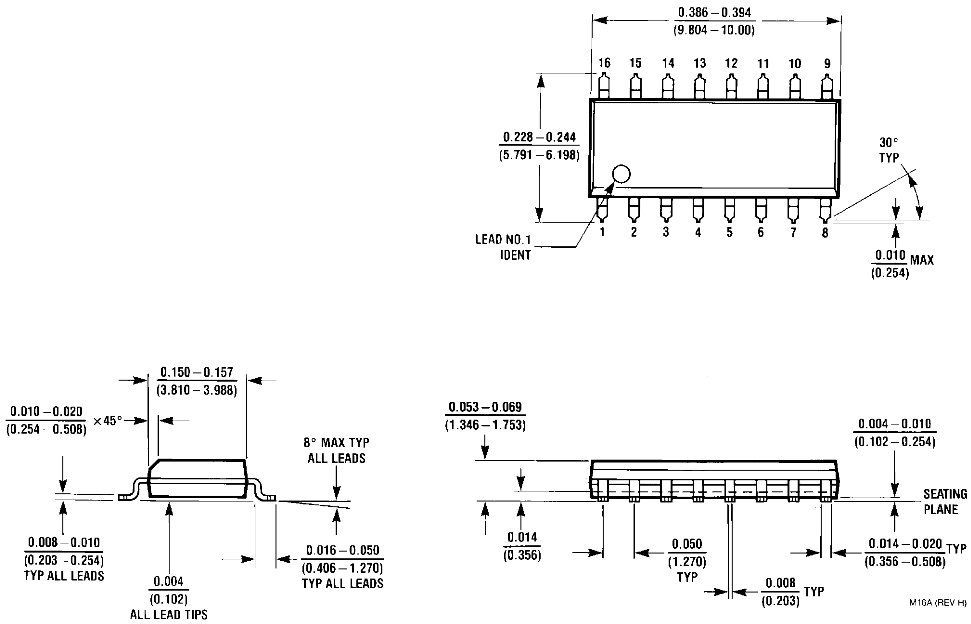


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS138LMQB or 54LS139LMQB
Package Number E20A

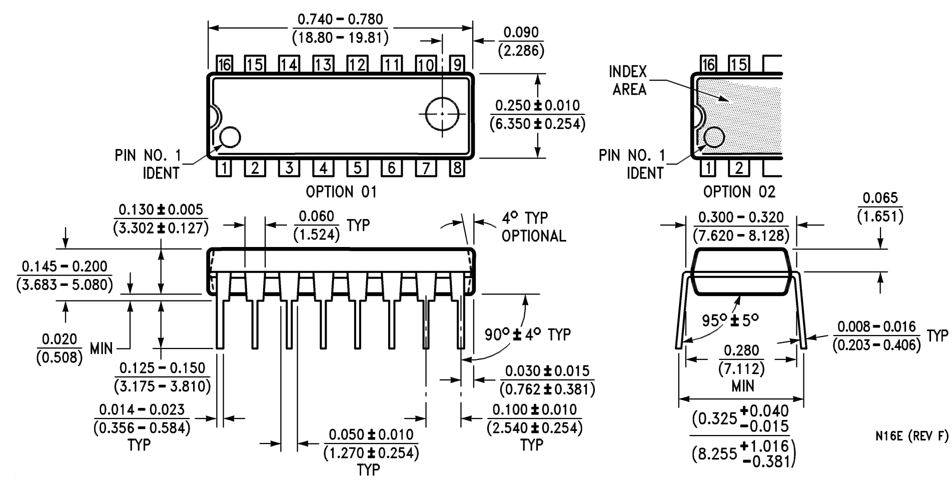


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS138DMQB, 54LS139DMQB, DM54LS138J or DM54LS139J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

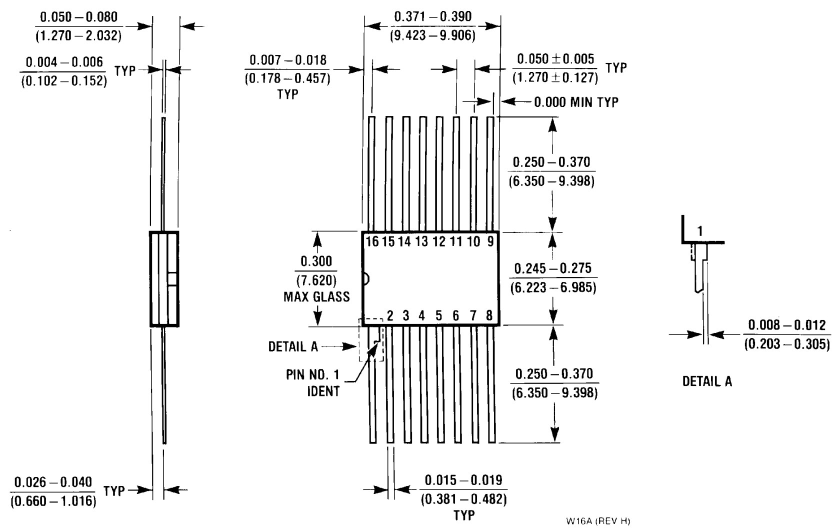


16-Lead Small Outline Molded Package (M)
Order Number DM74LS138M or DM74LS139M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS138N or DM74LS139N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS138FMQB, 54LS139FMQB, DM54LS138W or DM54LS139W
Package Number W16A

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March 1998

DM74LS138, DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

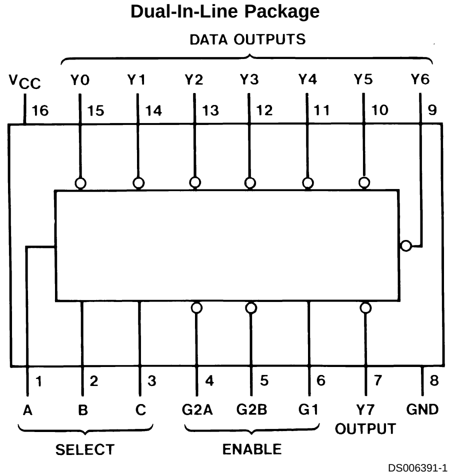
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW
- Alternate Military/Aerospace devices (54LS138, 54LS139) are available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

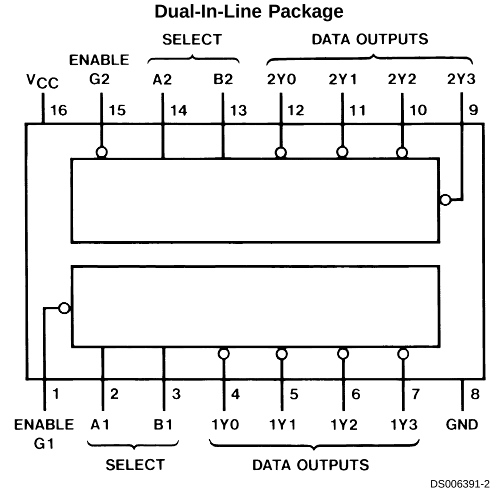
Connection Diagrams

Dual-In-Line Package



Order Number 54LS138DMQB, 54LS138FMQB, 54LS138LMQB, DM54LS138J, DM54LS138W, DM74LS138M or DM74LS138N
See Package Number E20A, J16A, M16A, N16E or W16A
Dual-in-Line Package

Dual-In-Line Package



Order Number 54LS139DMQB, 54LS139FMQB, 54LS139LMQB, DM54LS139J, DM54LS139W, DM74LS139M or DM74LS139N
See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max,	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			6.3	10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		18		27	ns

’LS138 Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		28		40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139			DM74LS139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

’LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max,	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			6.8	11	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured with all outputs enabled and open.

’LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	**G2** (Note 8)	**C**	**B**	**A**	**YO**	**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don’t Care

Note 8: G2 = G2A + G2B

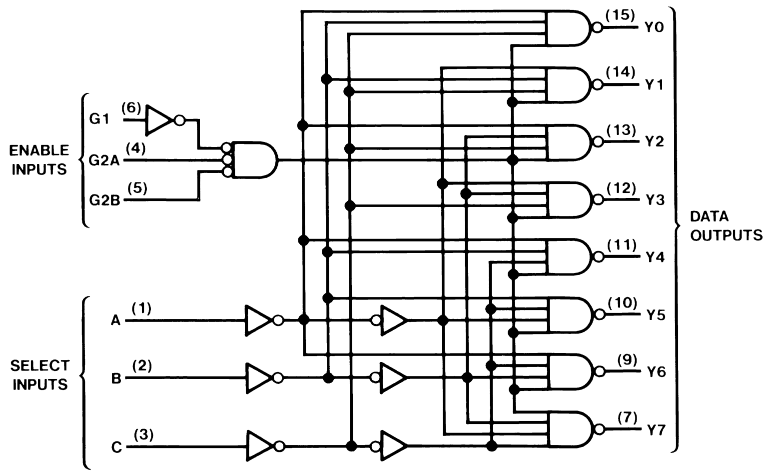
LS139

Inputs			Outputs			
Enable	Select					
G	**B**	**A**	**Y0**	**Y1**	**Y2**	**Y3**
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don’t Care

Logic Diagrams

LS138



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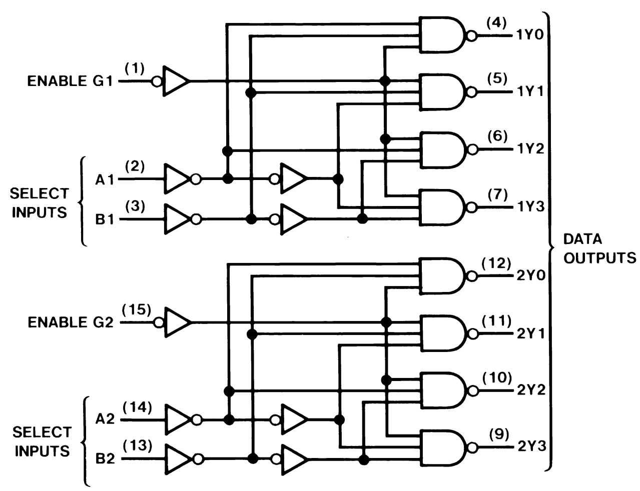
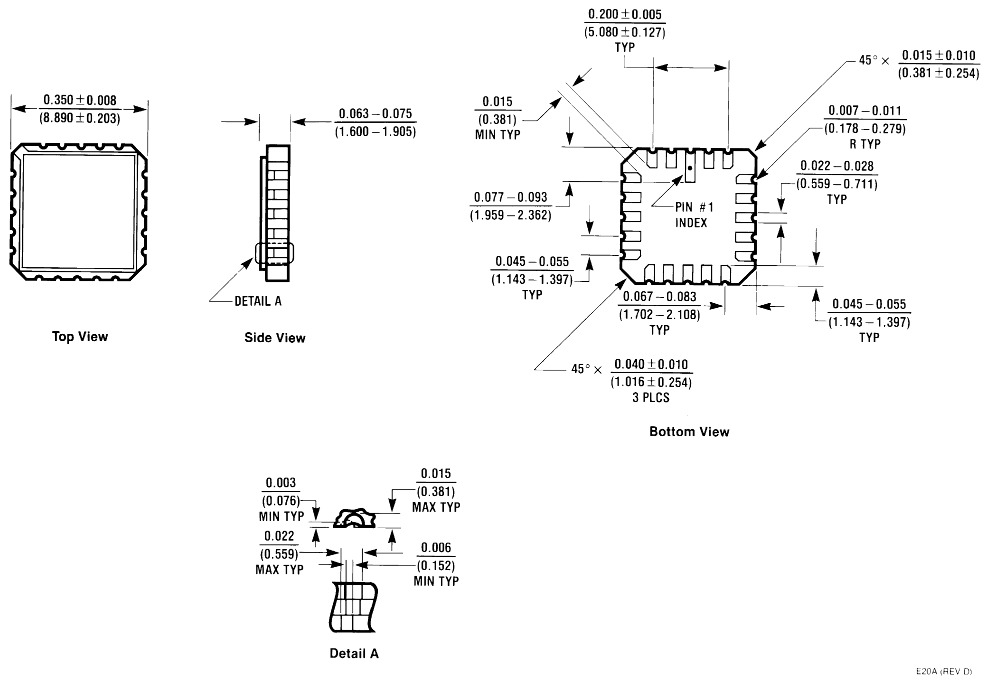
LS139

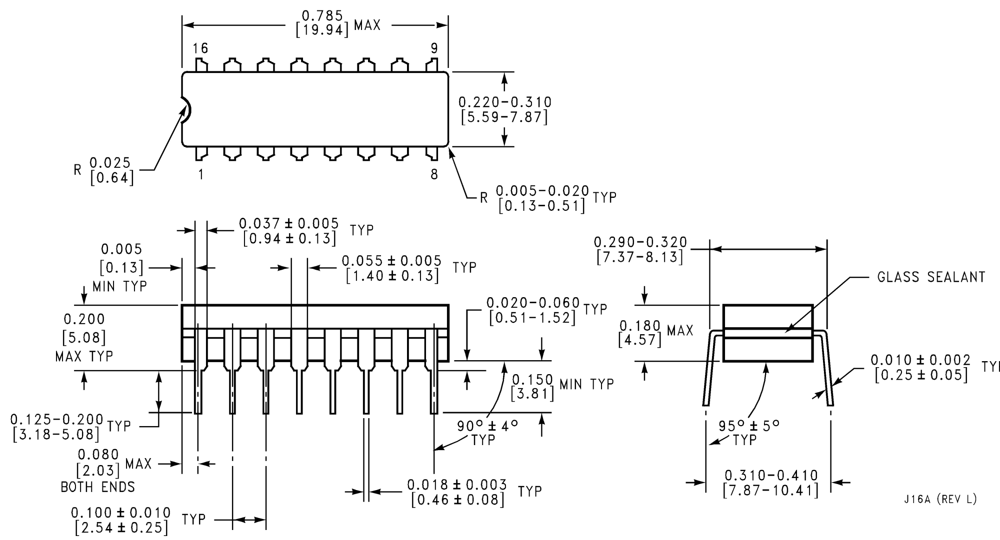


DS006391-4

Physical Dimensions inches (millimeters) unless otherwise noted

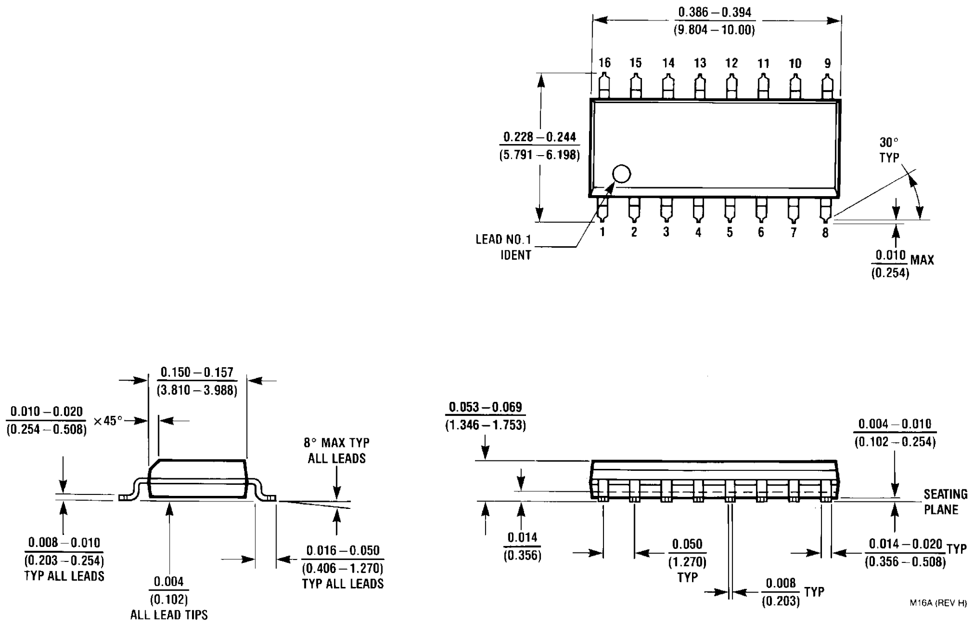


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS138LMQB or 54LS139LMQB
Package Number E20A

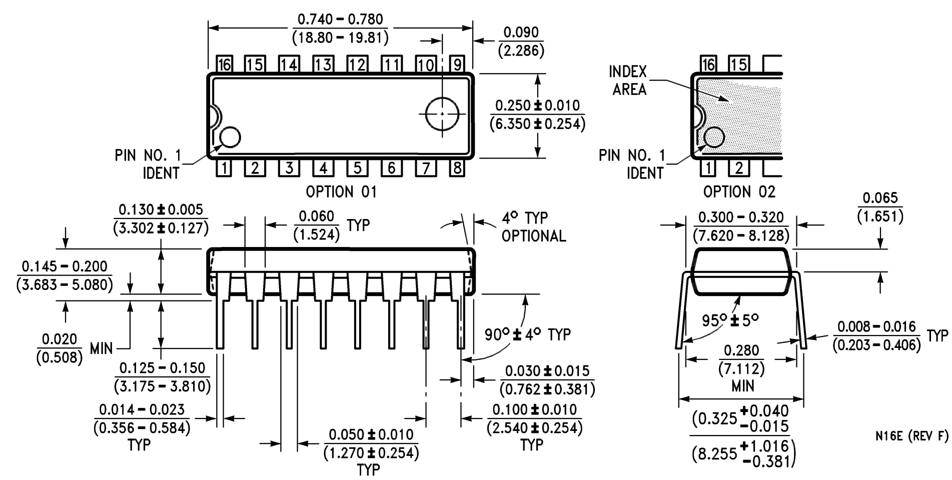


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS138DMQB, 54LS139DMQB, DM54LS138J or DM54LS139J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

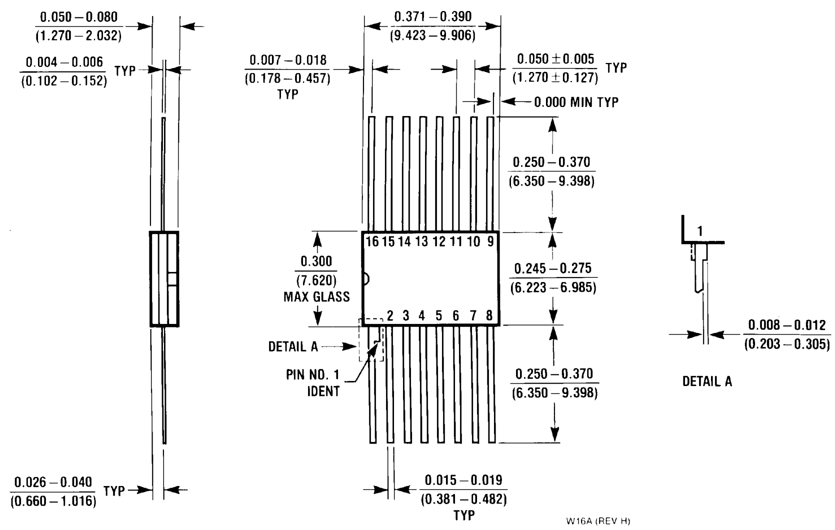


16-Lead Small Outline Molded Package (M)
Order Number DM74LS138M or DM74LS139M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS138N or DM74LS139N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS138FMQB, 54LS139FMQB, DM54LS138W or DM54LS139W
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS151
Data Selector/Multiplexer

General Description

This data selector/multiplexer contains full on-chip decoding to select the desired data source. The 'LS151 selects one-of-eight data sources. The 'LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.

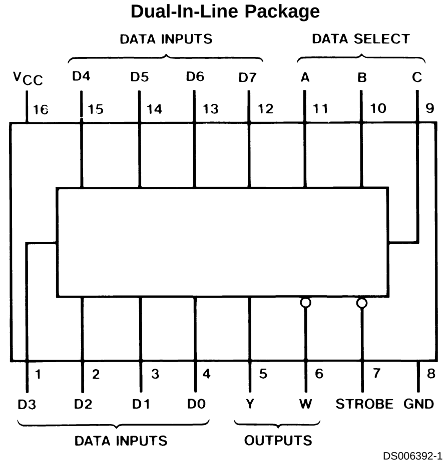
The 'LS151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time data input to W output 12.5 ns
- Typical power dissipation 30 mW

Connection Diagram

Dual-In-Line Package



Order Number 54LS151DMQB, 54LS151FMQB, 54LS151LMQB, DM54LS151J, DM54LS151W, DM74LS151M or DM74LS151N
See Package Number E20A, J16A, M16A, N16E or W16A

Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS151			DM74LS151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			6	10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open, strobe and data select inputs at 4.5V, and all other inputs open.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		43		46	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		23		25	ns

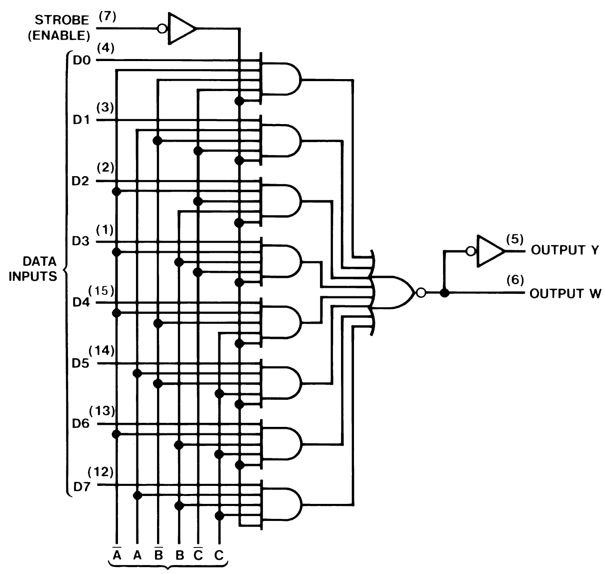
Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		42		44	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		24		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		32		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		26		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to W		21		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to W		20		27	ns

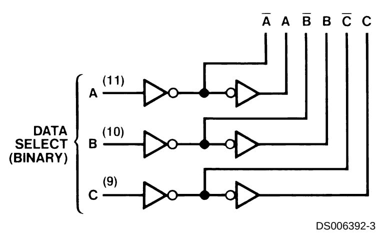
Logic Diagram

LS151

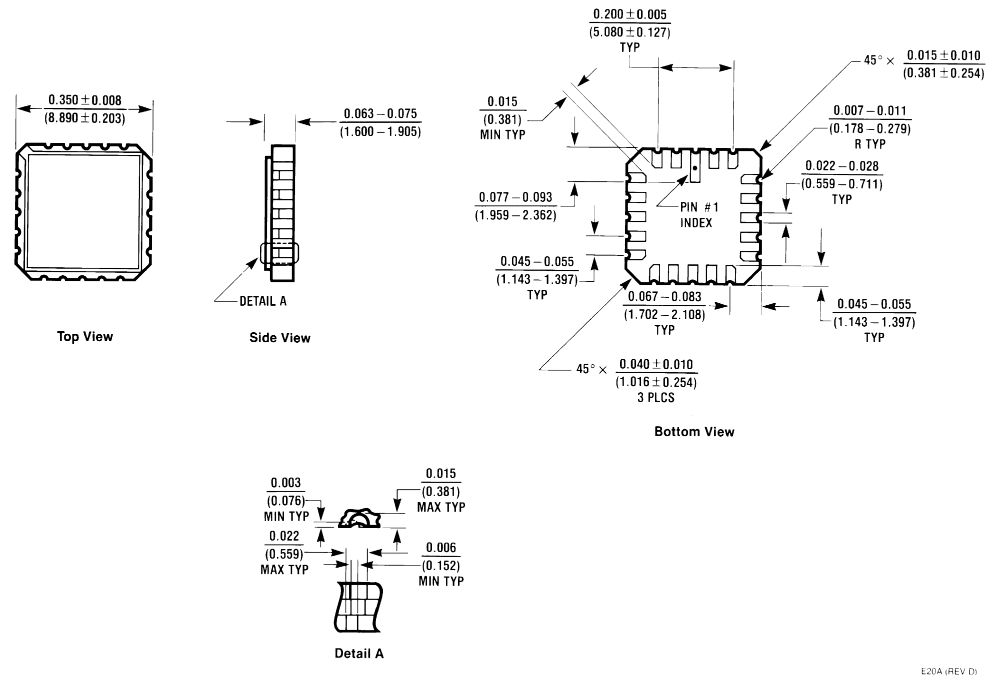


See Address Buffers to the Right

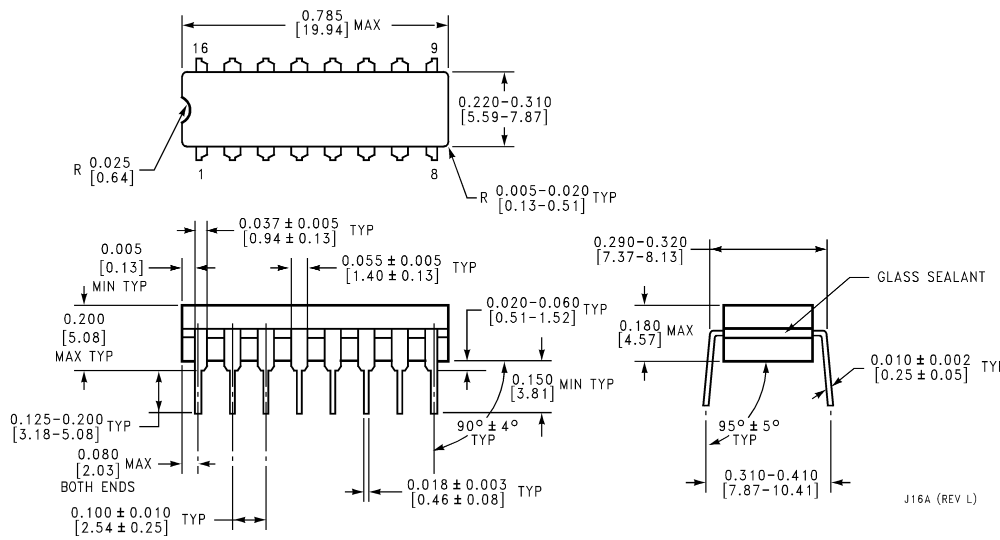
Address Buffers for 54LS151/74LS151



Physical Dimensions inches (millimeters) unless otherwise noted

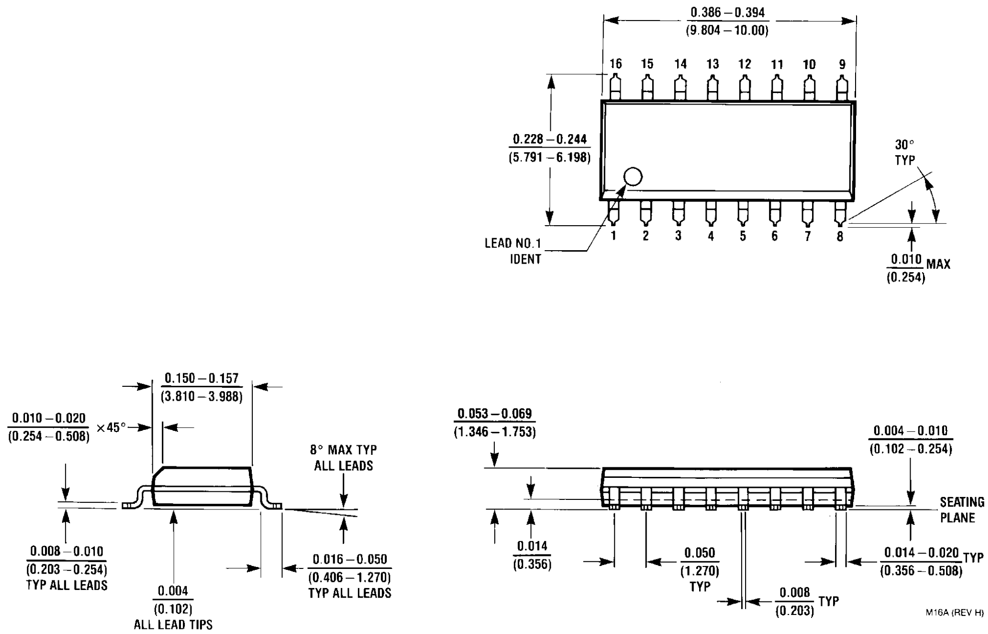


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS151LMQB
Package Number E20A

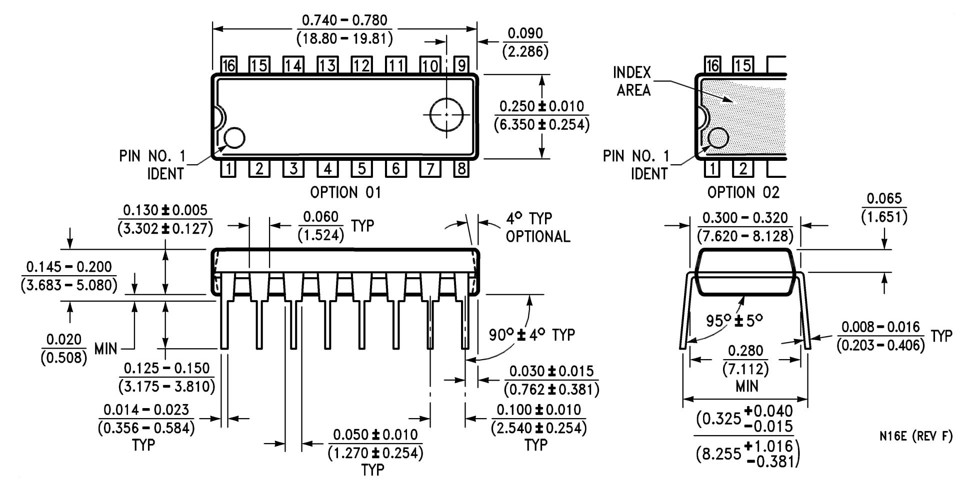


Ceramic Dual-In-Line Package (J)
Order Number 54LS151DMQB or DM54LS151J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

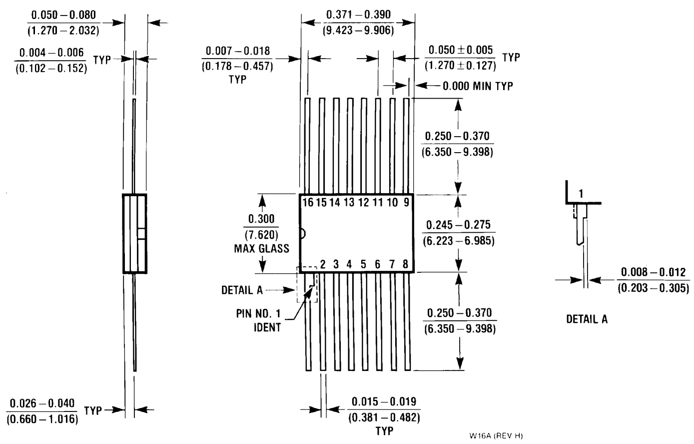


16-Lead Small Outline Molded Package (M)
Order Number DM74LS151M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS151N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS151FMQB or DM54LS151W
Package Number W16A

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

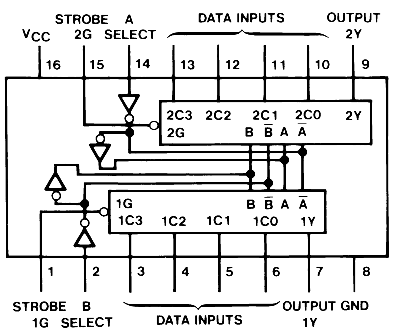
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - From data 14 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

Connection Diagram

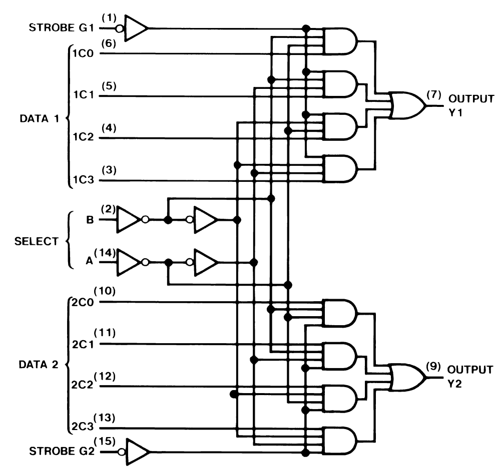
Dual-In-Line Package



DS006393-1

Order Number 54LS153DMQB, 54LS153FMQB, 54LS153LMQB, DM54LS153J, DM54LS153W, DM74LS153M or DM74LS153N
See Package Number E20A, J16A, M16A, N16E or W16A

Logic Diagram



DS006393-2

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	**A**	**C0**	**C1**	**C2**	**C3**	**G**	**Y**
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Recommended Operating Conditions

Symbol	Parameter	DM54LS153			DM74LS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			6.2	10	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

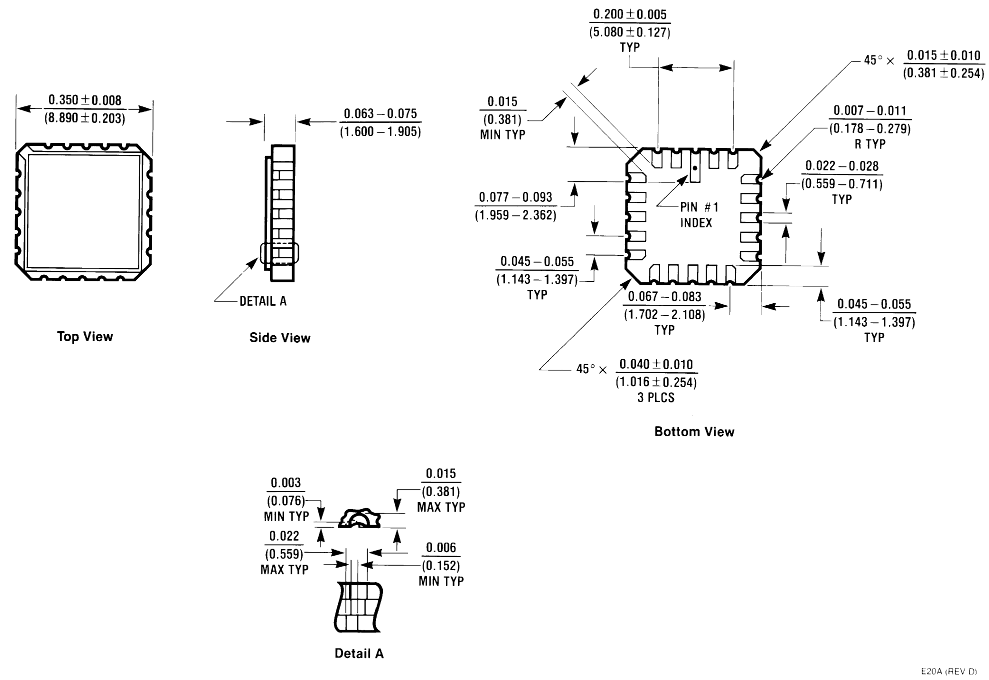
Note 4: I_{CC} is measured with all outputs open and all other inputs grounded.

Switching Characteristics

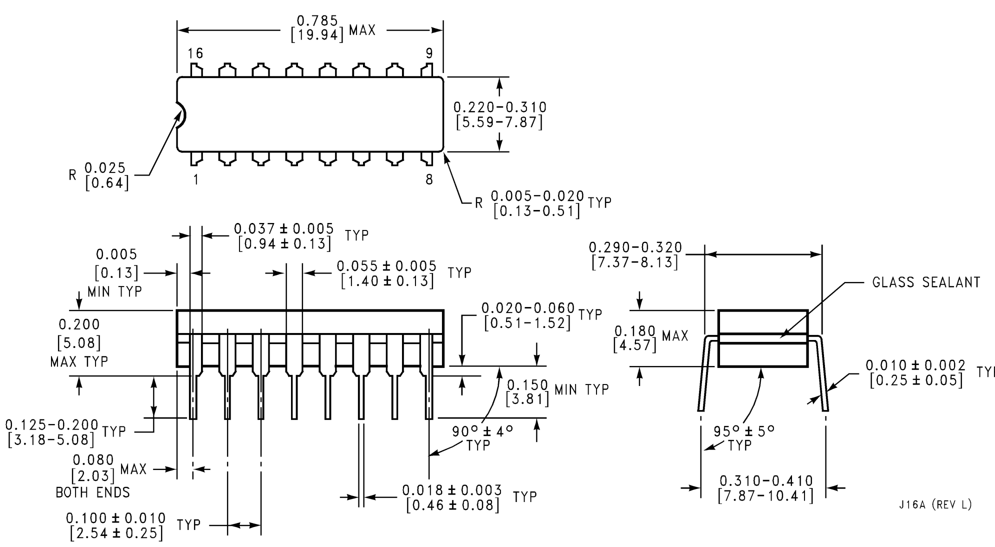
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) to (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		15		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		26		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns

Physical Dimensions inches (millimeters) unless otherwise noted

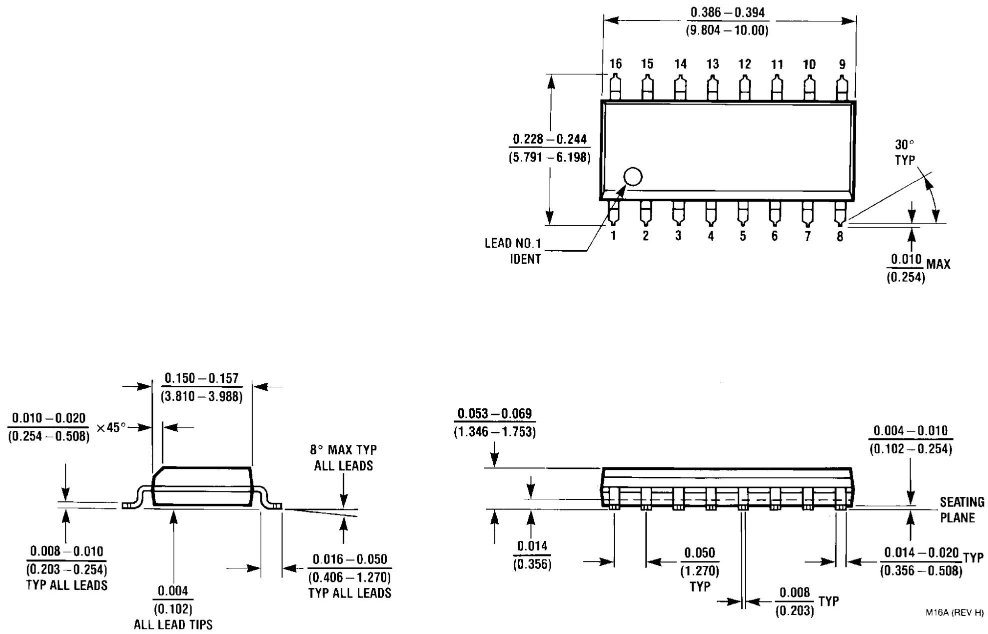


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS153LMQB
Package Number E20A

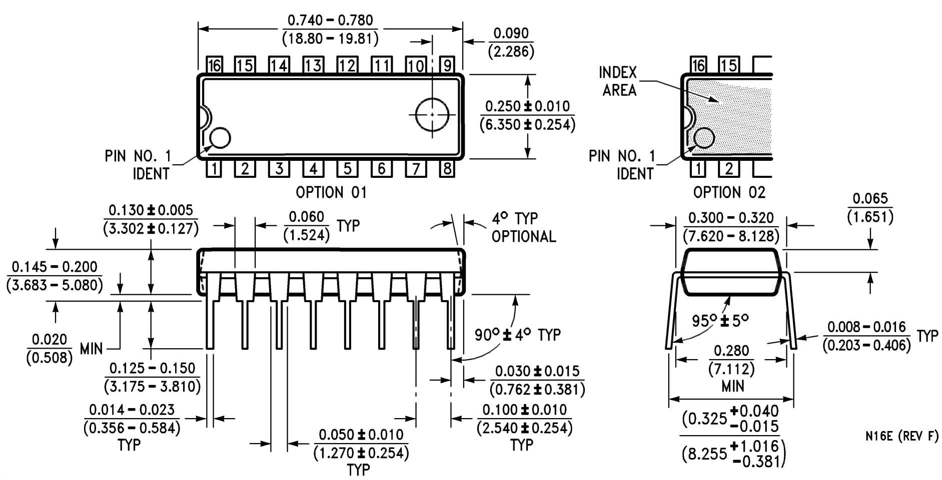


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS153DMQB or DM54LS153J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

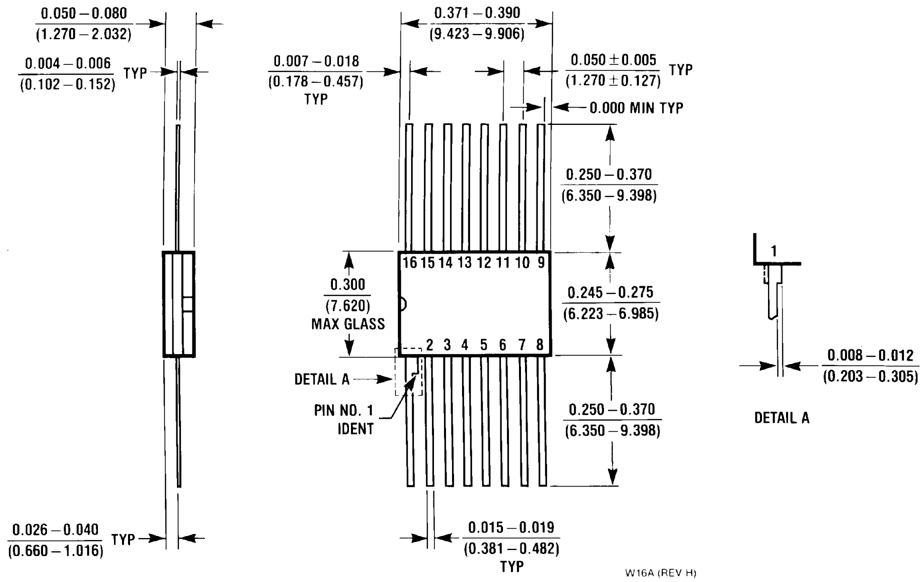


16-Lead Small Outline Molded Package (M)
Order Number DM74LS153M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS153N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS153FMQB or DM54LS153W
Package Number W16A

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March 1998

DM74LS154
4-Line to 16-Line Decoder/Demultiplexer

General Description

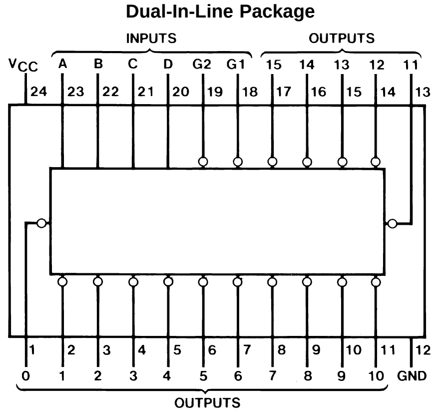
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  - 3 levels of logic 23 ns
  - Strobe 19 ns
- Typical power dissipation 45 mW

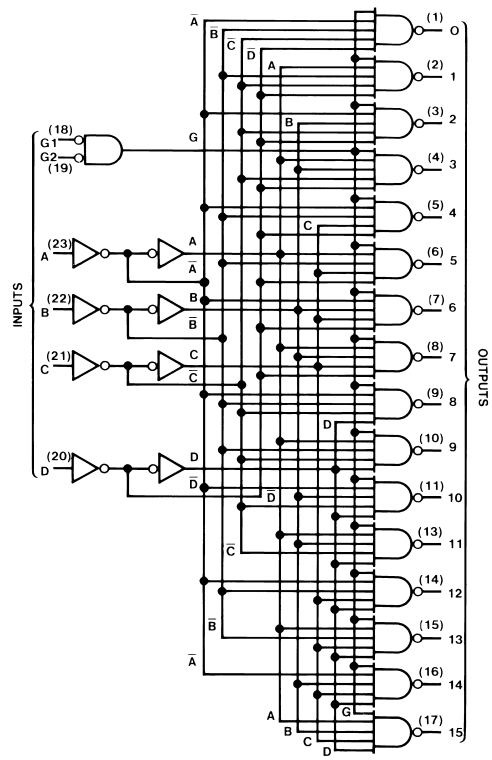
Connection and Logic Diagrams

Dual-In-Line Package



DS006394-1

Order Number DM54LS154J, DM74LS154WM or DM74LS154N
See Package Number J24A, M24B or N24A



DS006394-2

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM74		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min			0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9	14	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20		25	ns

Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

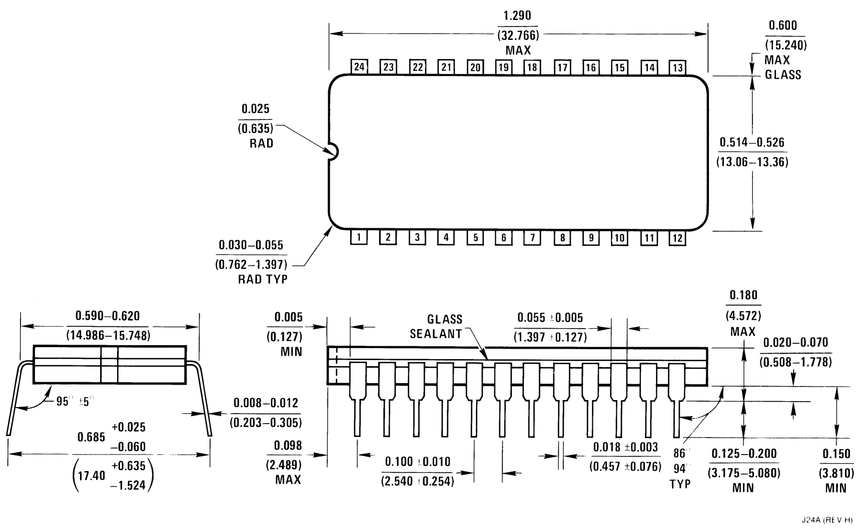
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		25		35	ns

Function Table

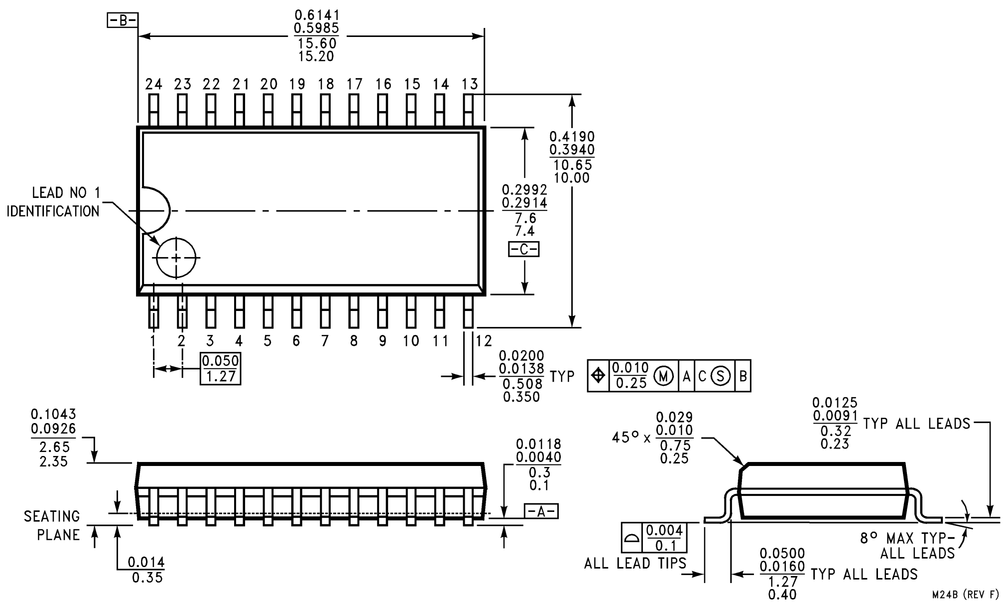
Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Physical Dimensions inches (millimeters) unless otherwise noted

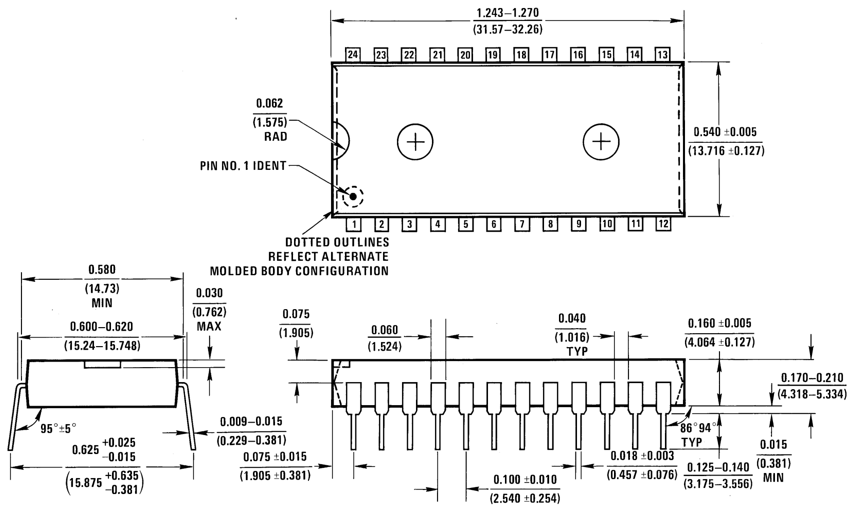


24-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS154J
Package Number J24A



24-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS154WM
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS154N
Package Number N24A

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March 1998

DM74LS155/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

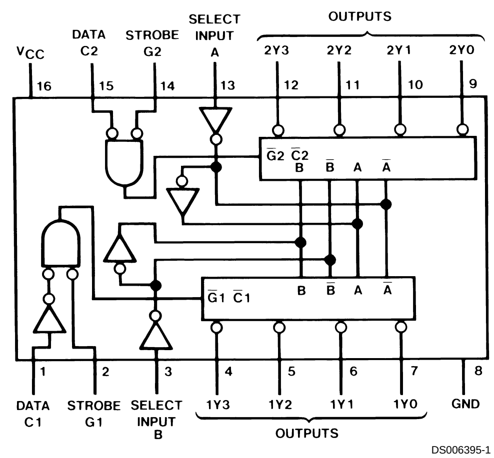
These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (LS155)
  - Open-collector (LS156)

Connection Diagram and Function Tables

Dual-In-Line Package



Order Number 54LS155DMQB, 54LS155FMQB, 54LS155LMQB, DM54LS155J, DM54LS155W, DM74LS155M, DM74LS155N, 54LS156DMQB, 54LS156FMQB, DM54LS156J, DM54LS156W, DM74LS156M or DM74LS156N
See Package Number E20A, J16A, M16A, N16E or W16A

Connection Diagram and Function Tables (Continued)

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C (Note 1)	**B**	**A**	**G** (Note 2)	**2Y0**	**2Y1**	**2Y2**	**2Y3**	**1Y0**	**1Y1**	**1Y2**	**1Y3**
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	**A**	**G1**	**C1**	**1Y0**	**1Y1**	**1Y2**	**1Y3**
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	**A**	**G2**	**C2**	**2Y0**	**2Y1**	**2Y2**	**2Y3**
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

H = high level, L = low level, X = don't care

Note 1: C = inputs C1 and C2 connected together

Note 2: G = inputs G1 and G2 connected together

Absolute Maximum Ratings (Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS155			DM74LS155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 3: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS155 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			6.1	10	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚ C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open, A,B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

'LS155 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		18		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		18		24	ns

’LS155 Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		27		35	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS156			DM74LS156			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

’LS156 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			6.1	10	mA

Note 7: All typicals are at V_{CC} = 5V, T_A = 25˚ C.

Note 8: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

’LS156 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

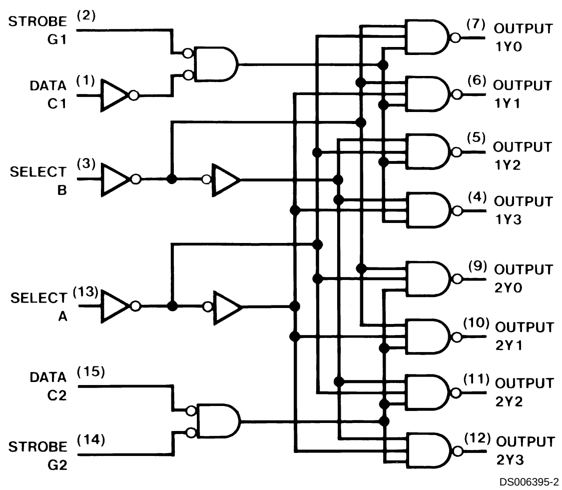
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		33		43	ns

’LS156 Switching Characteristics (Continued)

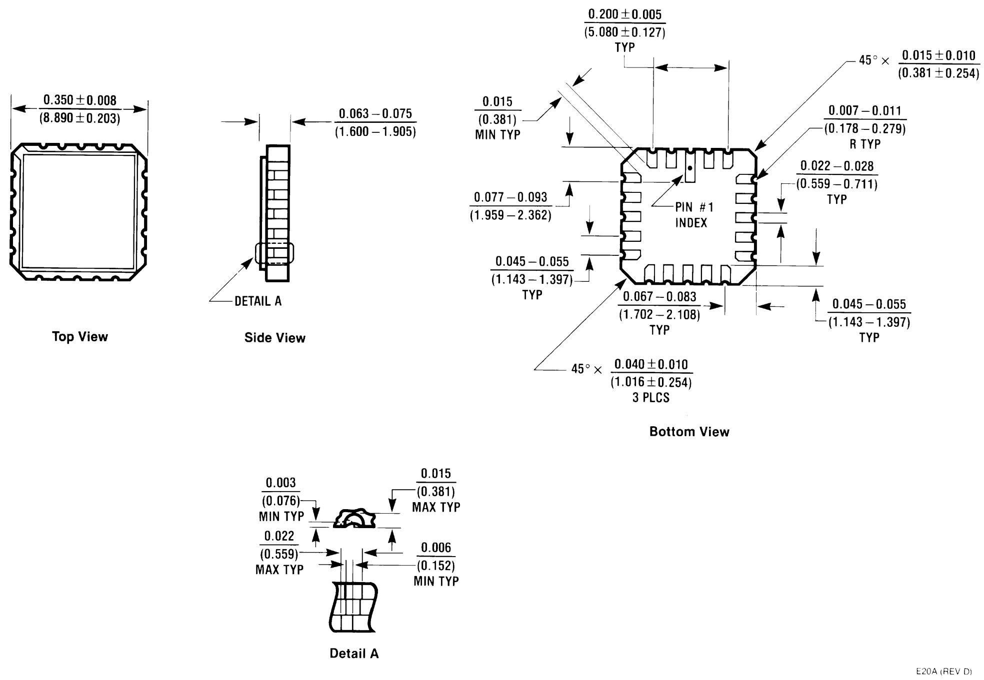
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		34		43	ns

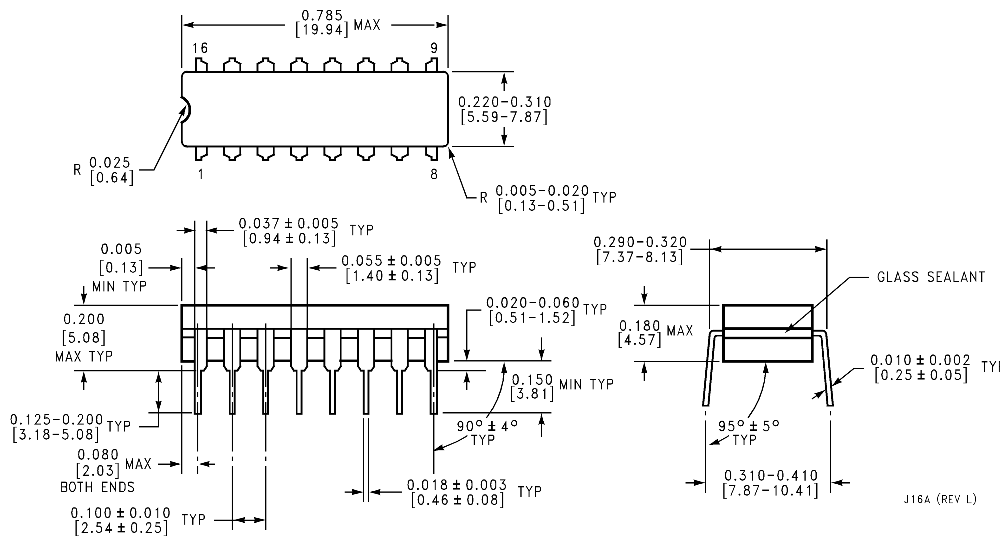
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

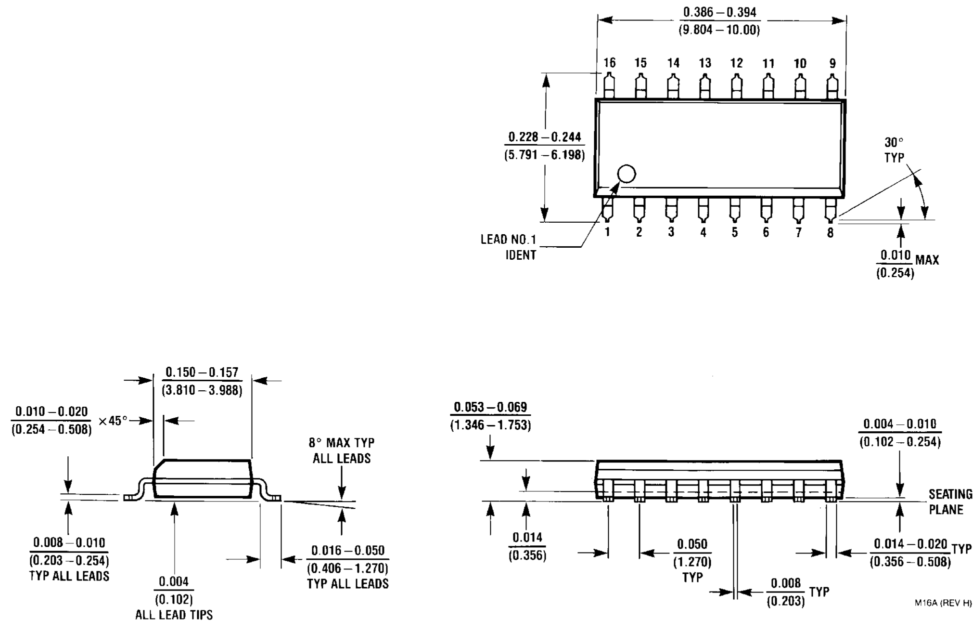


Ceramic Leadless Chip Carrier (E)
Order Number 54LS155LMQB
Package Number E20A

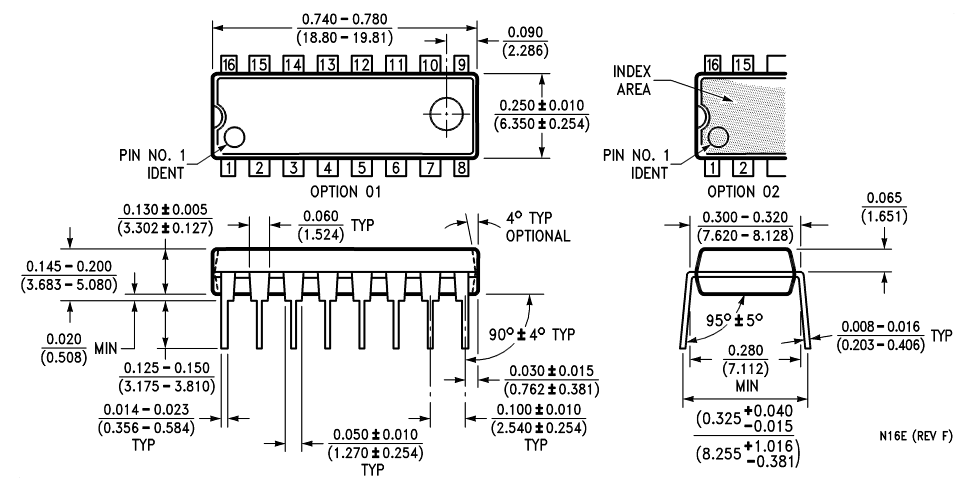


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS155DMQB, 54LS156DMQB, DM54LS155J or DM54LS156J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

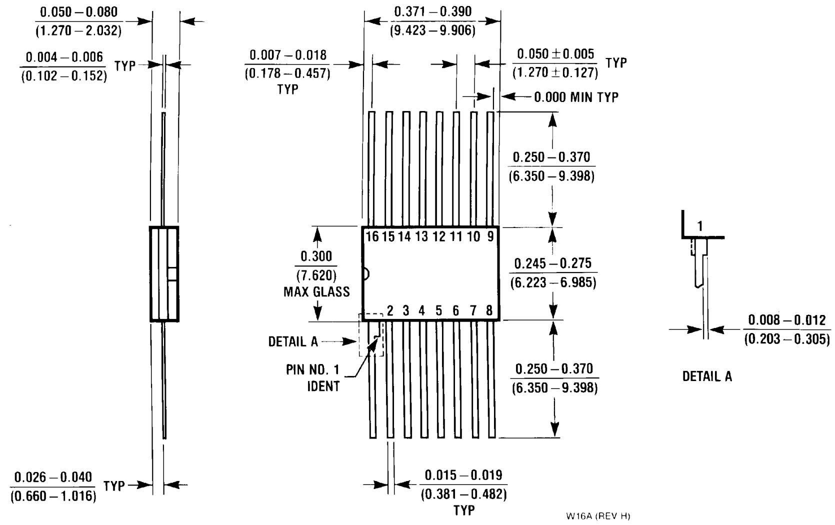


16-Lead Small Outline Molded Package (M)
Order Number DM74LS155M or DM74LS156M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS155N or DM74LS156N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS155FMQB, 54LS156FMQB, DM54LS155W or DM54LS156W
Package Number W16A

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March 1998

DM74LS155/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

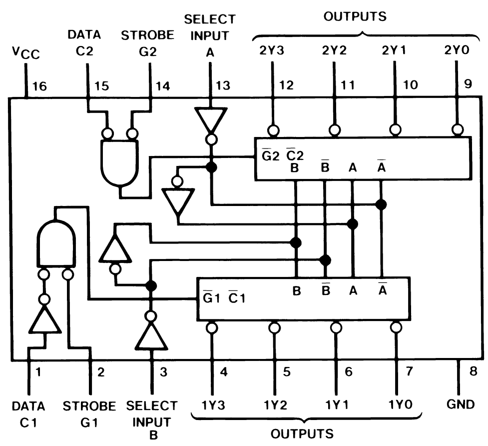
These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  - Totem-pole (LS155)
  - Open-collector (LS156)

Connection Diagram and Function Tables

Dual-In-Line Package



Order Number 54LS155DMQB, 54LS155FMQB, 54LS155LMQB, DM54LS155J, DM54LS155W, DM74LS155M, DM74LS155N, 54LS156DMQB, 54LS156FMQB, DM54LS156J, DM54LS156W, DM74LS156M or DM74LS156N
See Package Number E20A, J16A, M16A, N16E or W16A

Connection Diagram and Function Tables (Continued)

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				**Outputs**							
Select			**Strobe Or Data**	**(0)**	**(1)**	**(2)**	**(3)**	**(4)**	**(5)**	**(6)**	**(7)**
C (Note 1)	**B**	**A**	**G** (Note 2)	**2Y0**	**2Y1**	**2Y2**	**2Y3**	**1Y0**	**1Y1**	**1Y2**	**1Y3**
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				**Outputs**			
Select		**Strobe**	**Data**				
B	**A**	**G1**	**C1**	**1Y0**	**1Y1**	**1Y2**	**1Y3**
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				**Outputs**			
Select		**Strobe**	**Data**				
B	**A**	**G2**	**C2**	**2Y0**	**2Y1**	**2Y2**	**2Y3**
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

H = high level, L = low level, X = don't care

Note 1: C = inputs C1 and C2 connected together

Note 2: G = inputs G1 and G2 connected together

Absolute Maximum Ratings (Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS155			DM74LS155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 3: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS155 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			6.1	10	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open, A,B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

'LS155 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		18		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		18		24	ns

’LS155 Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		27		35	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS156			DM74LS156			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

’LS156 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 8)			6.1	10	mA

Note 7: All typicals are at V_{CC} = 5V, T_A = 25˚ C.

Note 8: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

’LS156 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

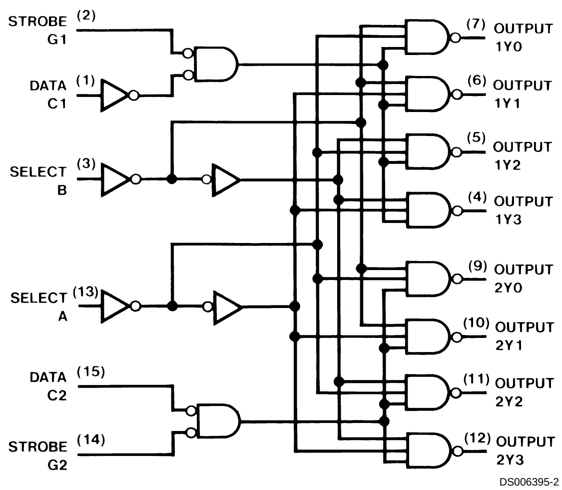
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		33		43	ns

’LS156 Switching Characteristics (Continued)

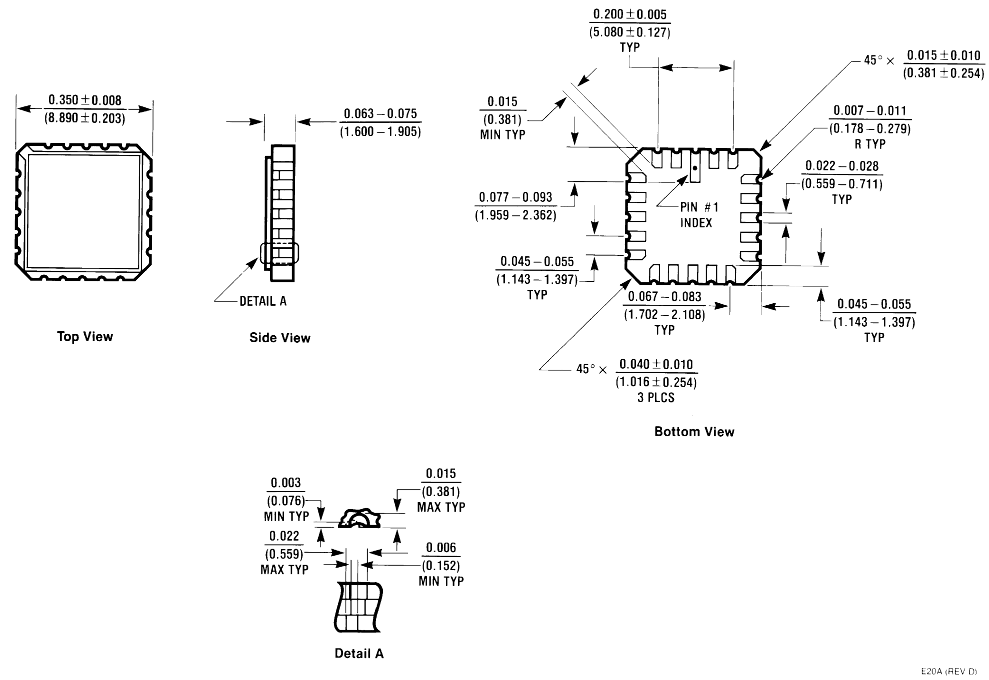
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		34		43	ns

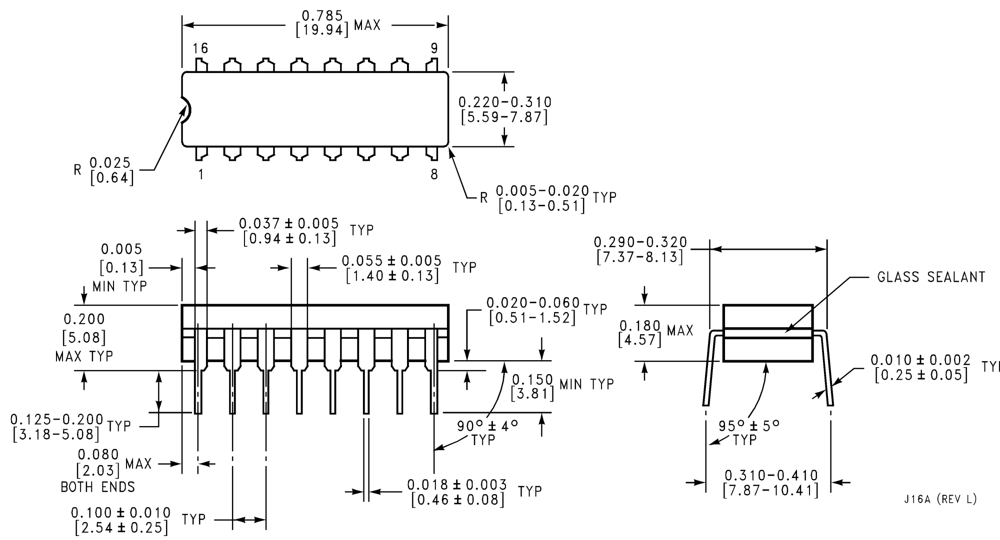
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

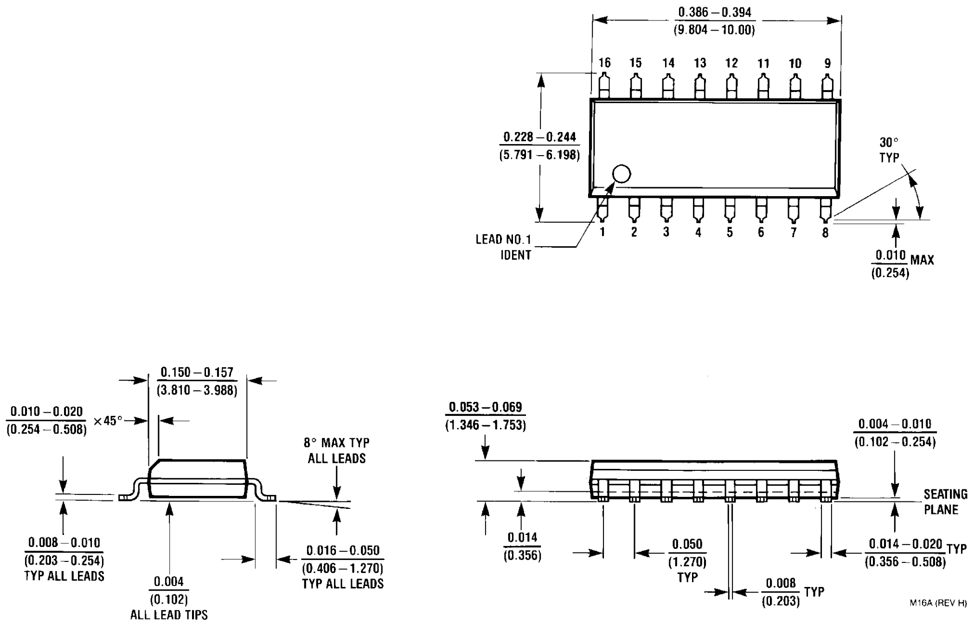


Ceramic Leadless Chip Carrier (E)
Order Number 54LS155LMQB
Package Number E20A

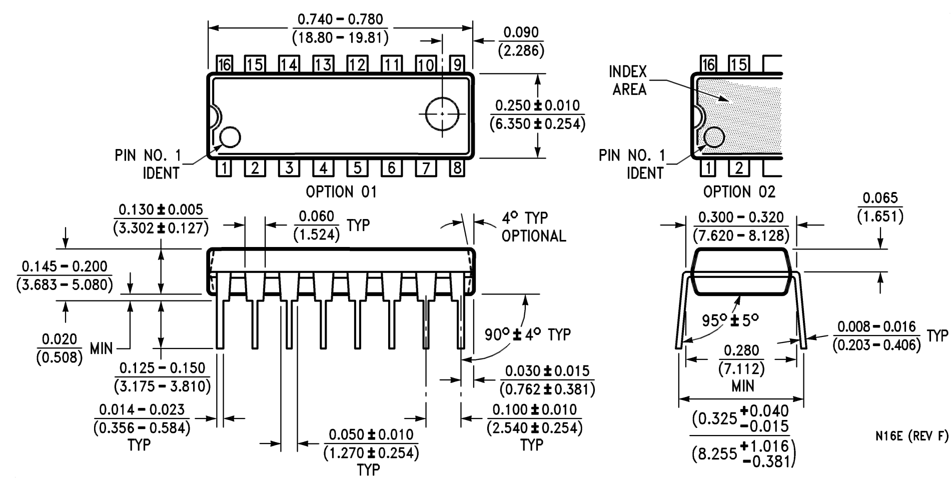


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS155DMQB, 54LS156DMQB, DM54LS155J or DM54LS156J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

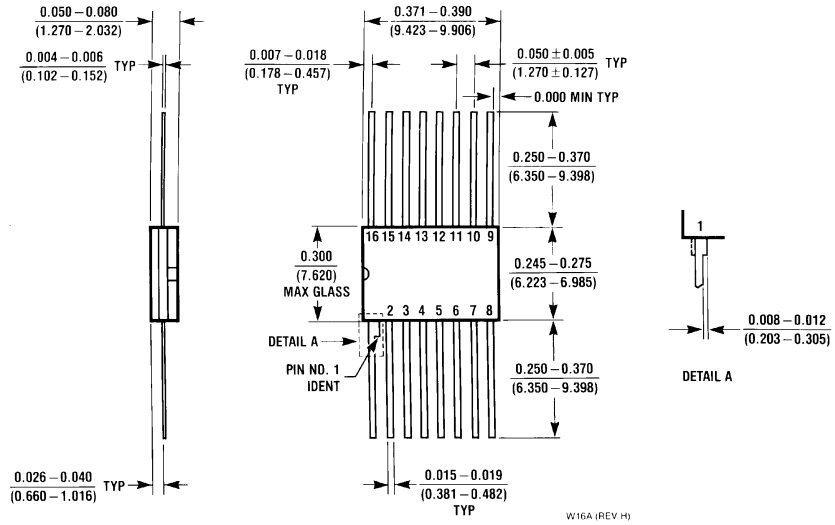


16-Lead Small Outline Molded Package (M)
Order Number DM74LS155M or DM74LS156M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS155N or DM74LS156N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS155FMQB, 54LS156FMQB, DM54LS155W or DM54LS156W
Package Number W16A

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March 1998

DM74LS157/DM74LS158
Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time.

Applications

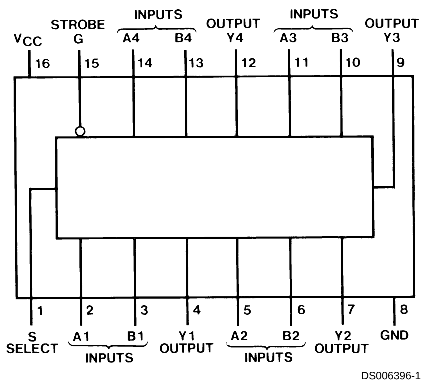
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical Propagation Time
  LS157 9 ns
  LS158 7 ns
- Typical Power Dissipation
  LS157 49 mW
  LS158 24 mW

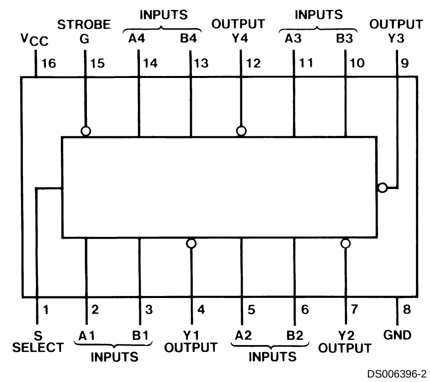
Connection Diagrams

Dual-In-Line Package



Order Number 54LS157DMQB, 54LS157FMQB, 54LS157LMQB, DM54LS157J, DM54LS157W, DM74LS157M or DM74LS157N
See Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



Order Number 54LS158DMQB, 54LS158FMQB, 54LS158LMQB, DM54LS158J, DM54LS158W, DM74LS158M or DM74LS158N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS157			DM74LS157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS157 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	S or G			0.2	mA
		V_I = 7V	A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	S or G			40	µA
		V_I = 2.7V	A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max	S or G			−0.8	mA
		V_I = 0.4V	A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			9.7	16	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

'LS157 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14		23	ns

’LS157 Switching Characteristics (Continued)

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27		32	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS158			DM74LS158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

’LS158 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	S or G			0.2	mA
		V_I = 7V	A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	S or G			40	µA
		V_I = 2.7V	A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max	S or G			−0.8	mA
		V_I = 0.4V	A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 6)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			4.8	8	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

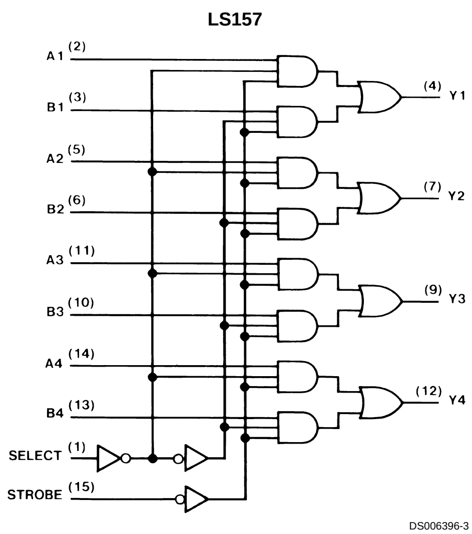
Note 7: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

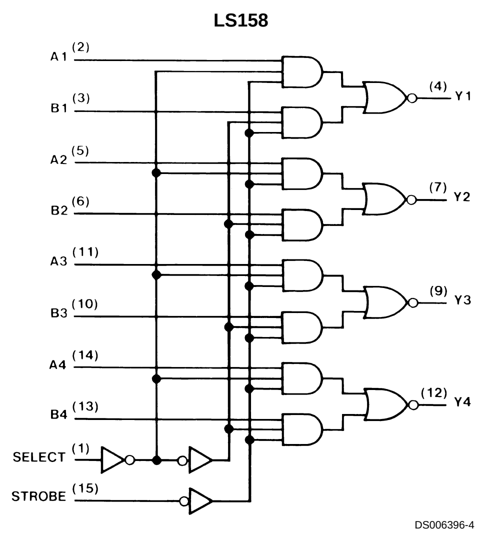
'LS158 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

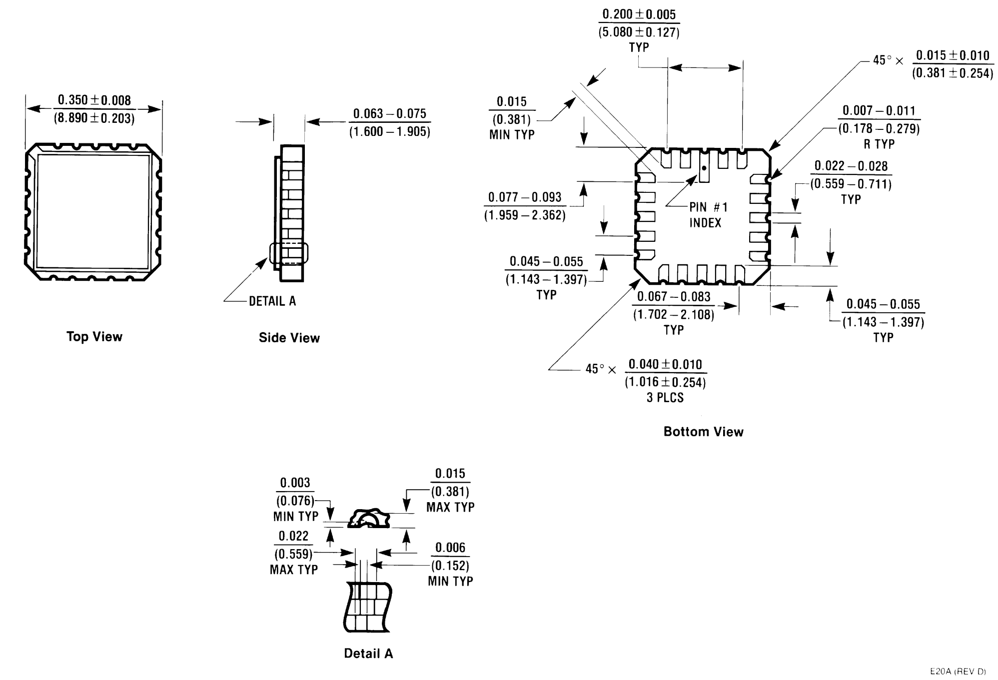
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		12		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		12		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		17		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		24		36	ns

Logic Diagrams

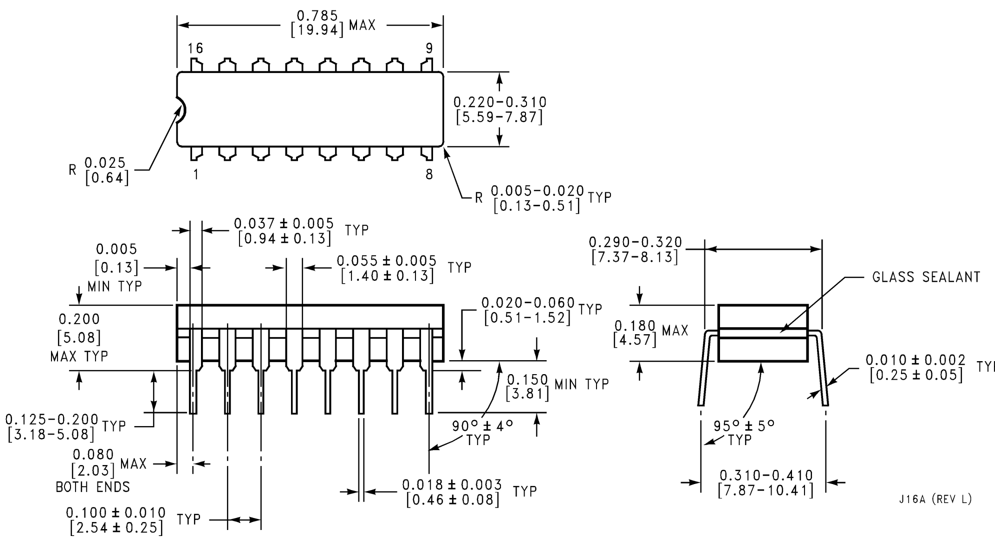




Physical Dimensions inches (millimeters) unless otherwise noted

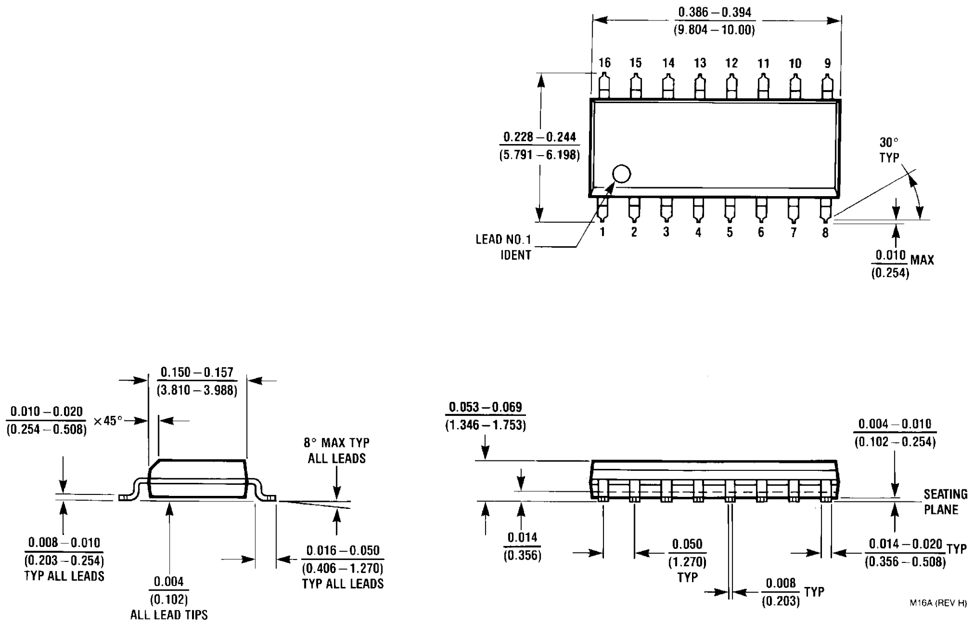


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS157LMQB or 54LS158LMQB
Package Number E20A

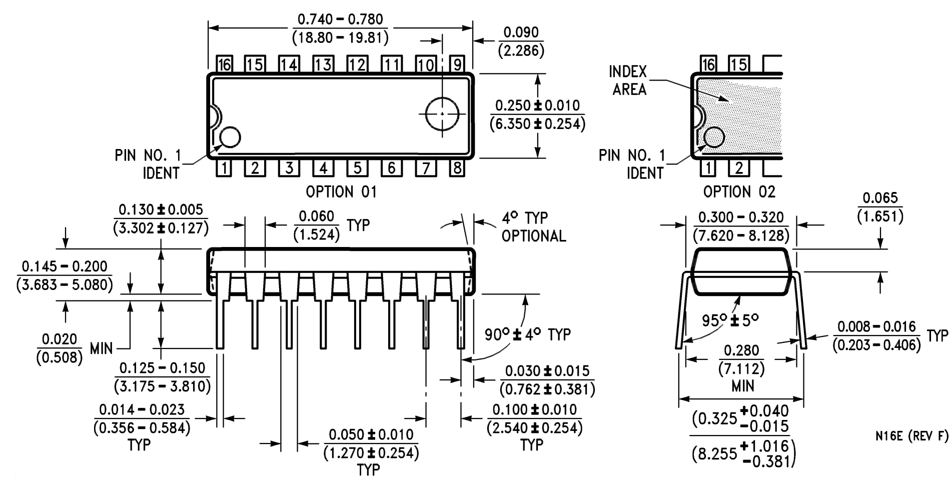


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS157DMQB, 54LS158DMQB, DM54LS157J or DM54LS158J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

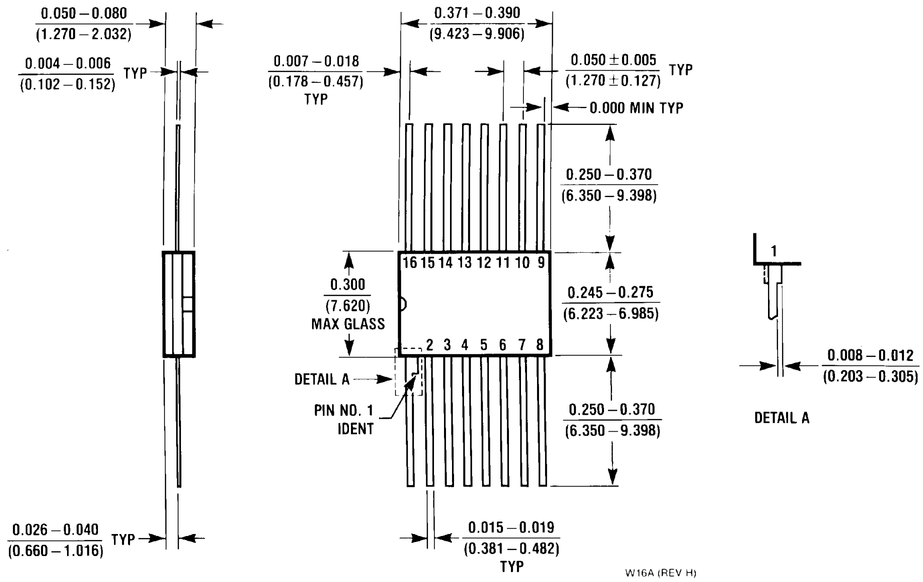


16-Lead Small Outline Molded Package (M)
Order Number DM74LS157M or DM74LS158M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS157N or DM74LS158N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS157FMQB, 54LS158FMQB, DM54LS157W or DM54LS158W
Package Number W16A

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May 1992

54LS160A/DM74LS160A, 54LS162A/DM74LS162A Synchronous Presettable BCD Decade Counters

General Description

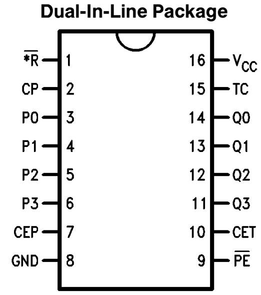
The 'LS160 and 'LS162 are high speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'LS160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'LS162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

Features

- Synchronous counting and loading
- High speed synchronous expansion
- Typical count rate of 35 MHz
- Fully edge triggered

Connection Diagram

Dual-In-Line Package



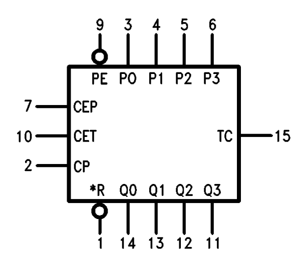
TL/F/10177–1

*$\overline{MR}$ for 'LS160
*$\overline{SR}$ for 'LS162

Order Number 54LS160ADMQB, 54LS160AFMQB, 54LS160ALMQB, 54LS162ADMQB, 54LS162AFMQB, 54LS162ALMQB, DM74LS160AM, DM74LS160AN, DM74LS162AM or DM74LS162AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('160)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('162)	Synchronous Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q0–Q3	Flip-Flop Outputs
TC	Terminal Count Output

Logic Symbol



TL/F/10177–2

V_{CC} = Pin 16 *$\overline{MR}$ for 'LS160
GND = Pin 8 *$\overline{SR}$ for 'LS162

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS160A/162A			DM74LS160A/162A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	0.0 0.0			0.0 0.0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ to CP	0 0			0 0			ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	20 20			20 20			ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP, CET or $\overline{SR}$ to CP	0 0			0 0			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width, HIGH or LOW	15 25			15 25			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW ('160)	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP ('160)	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Other			0.1	mA
		$\overline{PE}$, CET Inputs				0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Other			20	μA
		$\overline{PE}$, CET Inputs				40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V Inputs	54LS			−0.4	mA
			DM74			−1.6	
		$\overline{PE}$, CET Inputs				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs HIGH	V_{CC} = Max, $\overline{PE}$ = GND CP = $\uparrow$, Other Inputs = 4.5V				31	mA
I_{CCL}	Supply Current with Outputs LOW	V_{CC} = Max, V_{IN} = GND CP = $\uparrow$				31	mA

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	25		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to TC		25 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		24 27	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC		14 23	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('160)		28	ns

Functional Description

The 'LS160 and 'LS162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The '161 and '163 count modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'LS160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('LS160), synchronous reset ('LS162), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'LS160), Synchronous Reset ($\overline{SR}$, 'LS162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('LS160) or $\overline{SR}$ ('LS162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'LS160A and 'LS162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Functional Description (Continued)

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in the 9310 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the decade counters of the 'LS160, 'LS162, the TC output is fully decoded and can only be HIGH in state 9.

LOGIC EQUATIONS:

Count Enable = CEP • CET • $\overline{\text{PE}}$

TC = Q0 • $\overline{\text{Q1}}$ • $\overline{\text{Q2}}$ • Q3 • CET

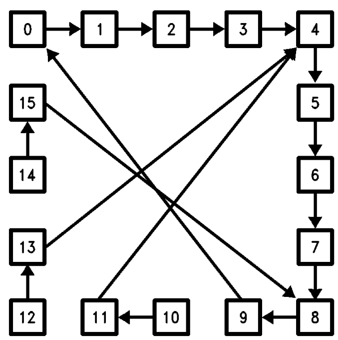
Mode Select Table

*$\overline{\text{SR}}$	$\overline{\text{PE}}$	CET	CEP	Action on the Rising Clock Edge (_/‾)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD ($P_n \rightarrow Q_n$)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the 'LS162
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

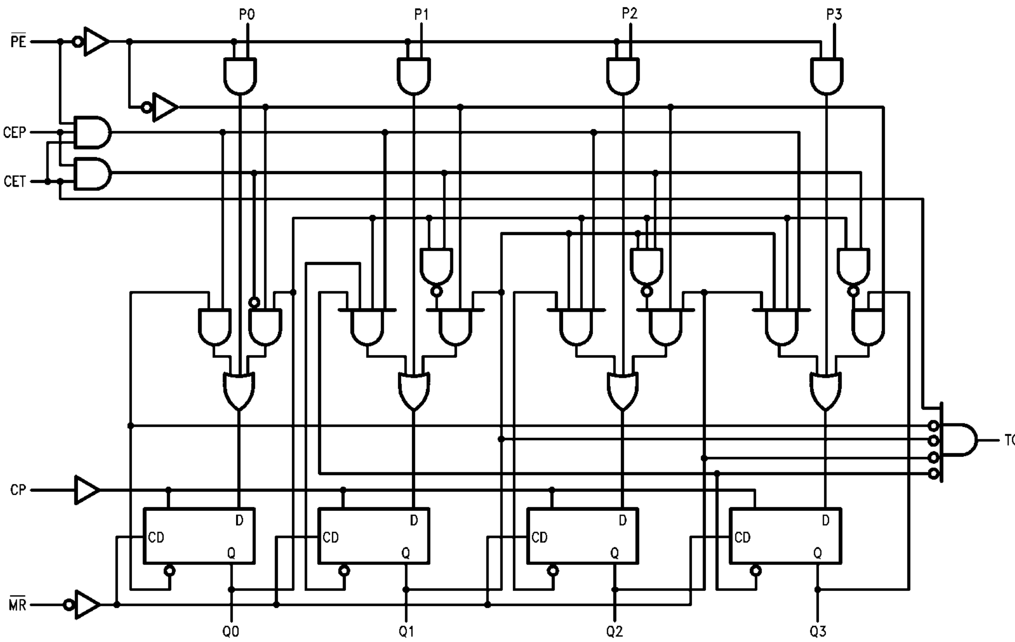
'LS160, 'LS162



TL/F/10177–5

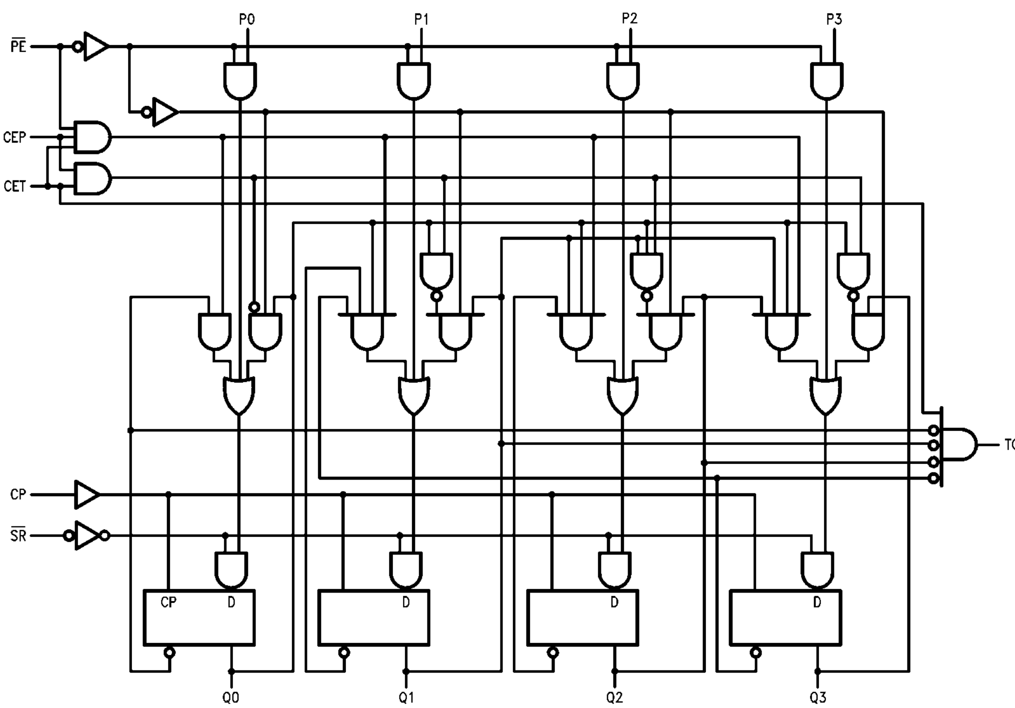
Logic Diagrams

'LS160



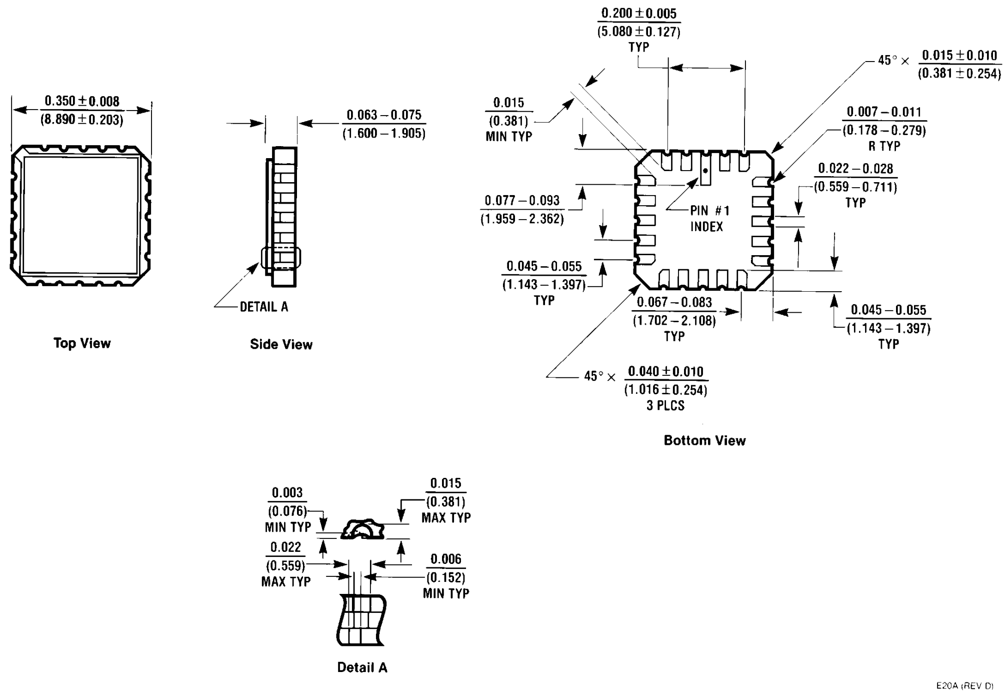
TL/F/10177–3

'LS162

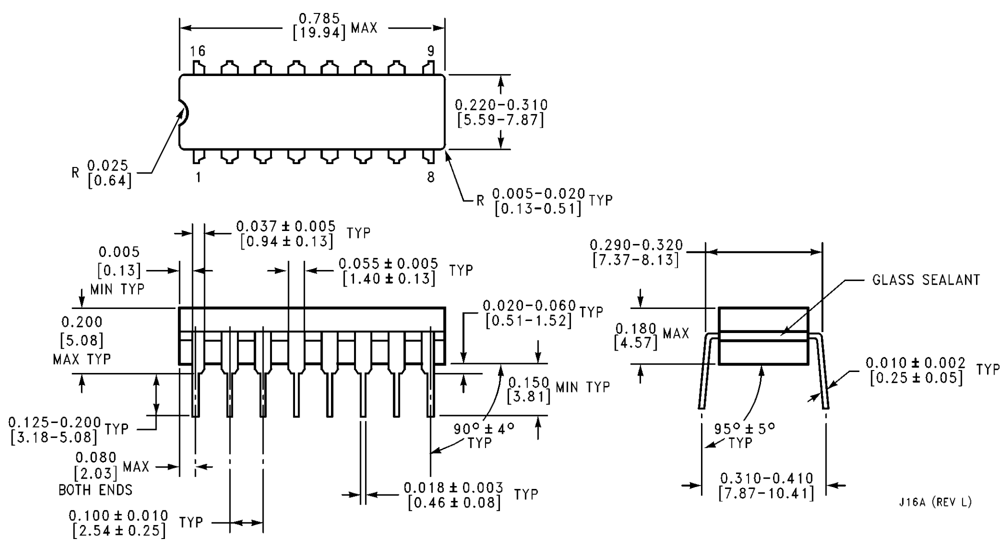


TL/F/10177–4

Physical Dimensions inches (millimeters)

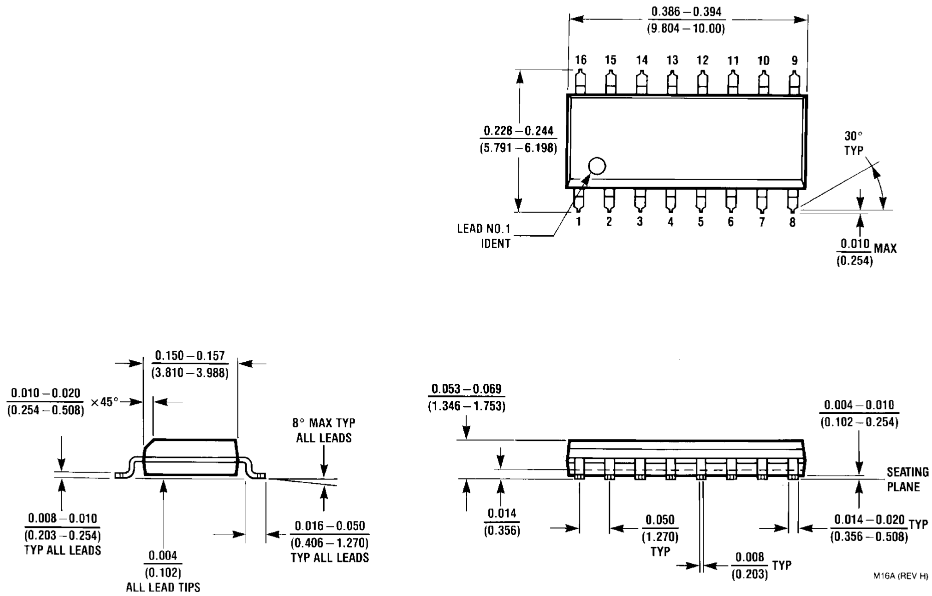


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS160ALMQB or 54LS162ALMQB
NS Package Number E20A

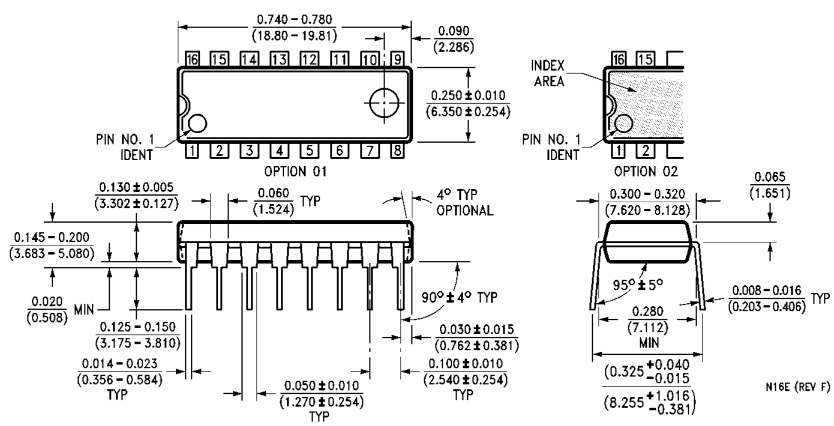


Ceramic Dual-In-Line Package (J)
Order Number 54LS160ADMQB or 54LS162ADMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

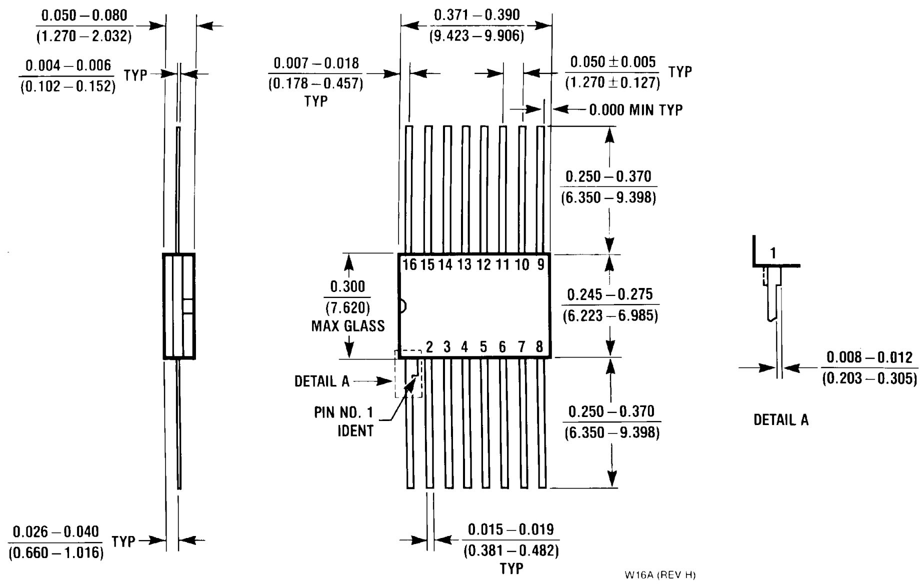


16-Lead Small Outline Molded Package (M)
Order Number DM74LS160AM DM74LS162AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS160AN or DM74LS162AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS160AFMQB or 54LS162AFMQB
NS Package Number W16A

National Semiconductor Corporation
1111 West Bardin Road
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March 1998

DM74LS161A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

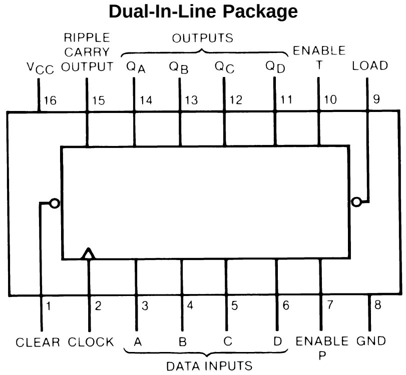
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Connection Diagram

Dual-In-Line Package



DS006397-1

Order Numbers 54LS161ADMQB, 54LS161AFMQB, 54LS161ALMQB, 54LS163ADMQB, 54LS163AFMQB, 54LS163ALMQB, DM54LS161AJ, DM54LS161AW, DM54LS163AJ, DM54LS163AW, DM74LS161AM, DM74LS161AN, DM74LS163AM or DM74LS163AN
See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS161A			DM74LS161A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 3)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 2)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 3)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 2)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 3)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 2)		20			20			ns
	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

’LS161 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	

’LS161 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 6)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 7)			19	32	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 7: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

’LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		28		45	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS163A			DM74LS163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 8)		0		25	0		25	MHz
	Clock Frequency (Note 9)		0		20	0		20	MHz
t_W	Pulse Width (Note 8)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 9)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 8)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 9)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 8)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 9)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 8)		20			20			ns
	Clear Release Time (Note 9)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

’LS163 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock, Clear			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Load			40	
			Clock, Clear			40	
			Others			20	

’LS163 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 10)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock, Clear			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 11)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 12)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 13)			18	32	mA

Note 10: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 11: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 12: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 13: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

’LS163 Switching Characteristics

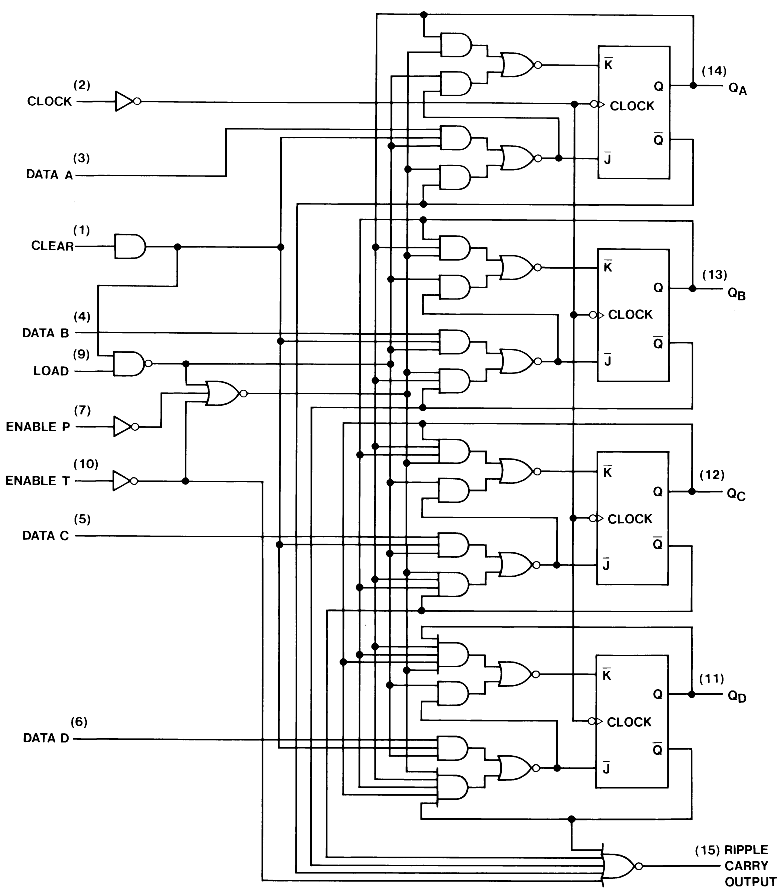
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		27		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		14		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q (Note 14)		28		45	ns

Note 14: The propagation delay clear to output is measured from the clock input transition.

Logic Diagram

LS163A

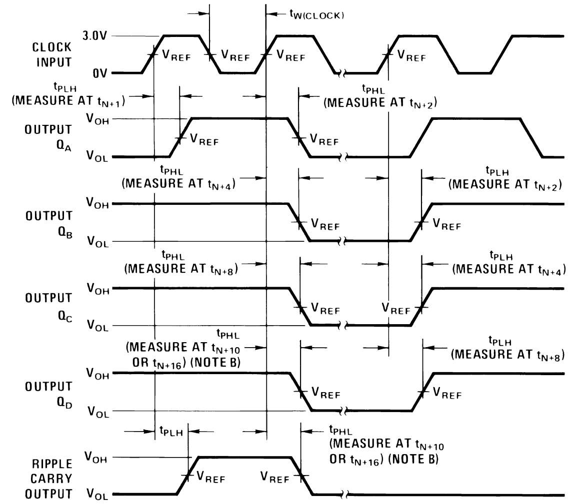


DS006397-2

The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

Parameter Measurement Information

Switching Time Waveforms



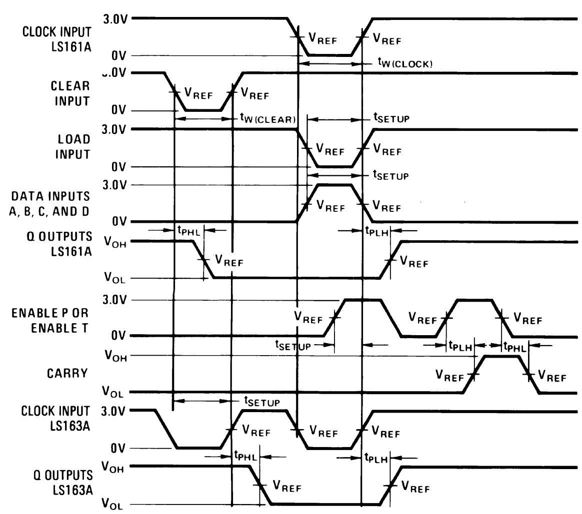
DS006397-3

Note 15: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note 16: Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

Note 17: V_{REF} = 1.5V.

Switching Time Waveforms



DS006397-4

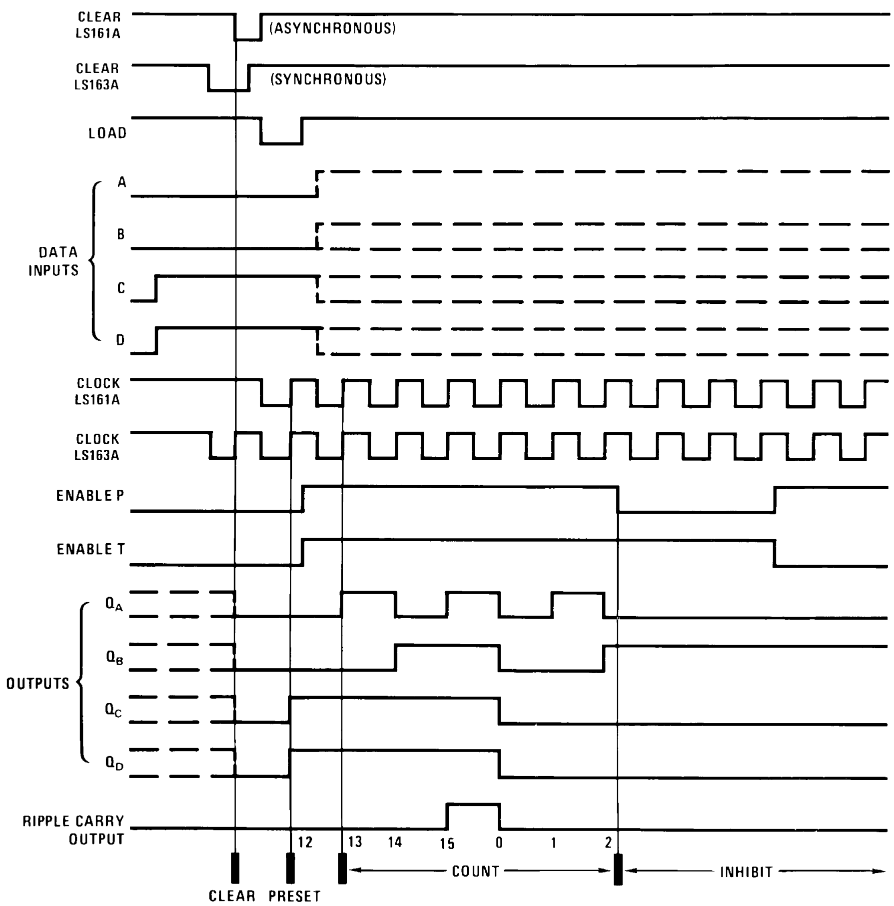
Note 18: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

Note 19: Enable P and enable T setup times are measured at t_{n+0}.

Note 20: V_{REF} = 1.3V.

Timing Diagram

LS161A, LS163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences

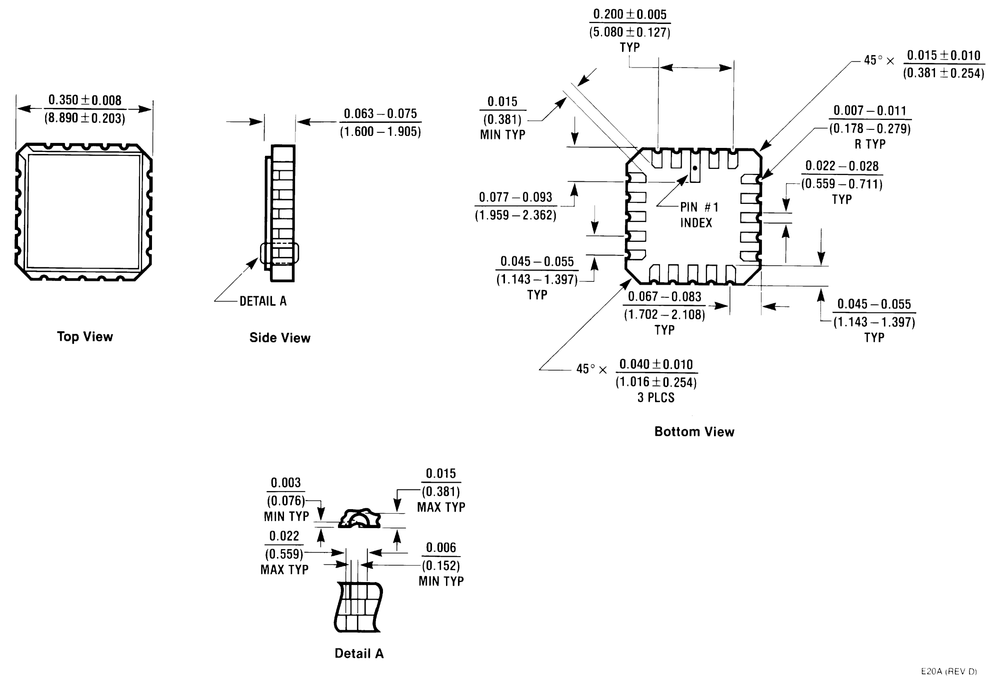


DS006397-5

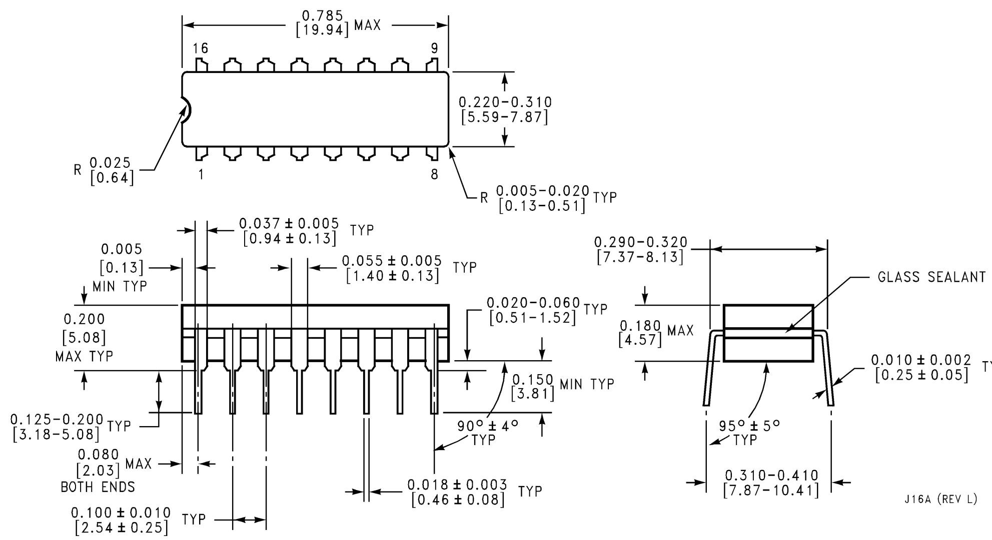
Sequence:

(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one, and two
(4) Inhibit

Physical Dimensions inches (millimeters) unless otherwise noted

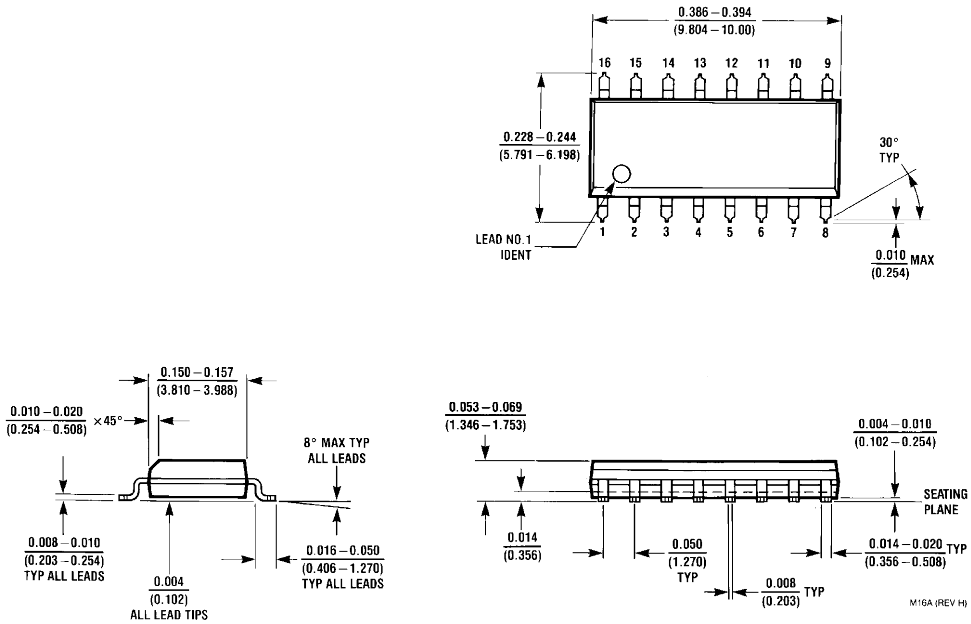


Ceramic Leadless Chip Carrier Package (E)
Order Numbers 54LS161ALMQB or 54LS163ALMQB
Package Number E20A

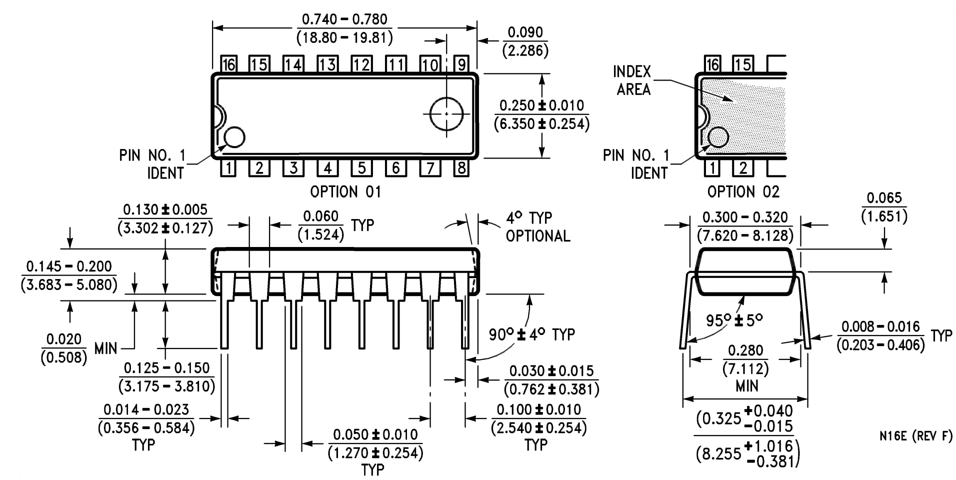


16-Lead Ceramic Dual-In-Line Package (J)
Order Numbers 54LS161ADMQB, 54LS163ADMQB, DM54LS161AJ or DM54LS163AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

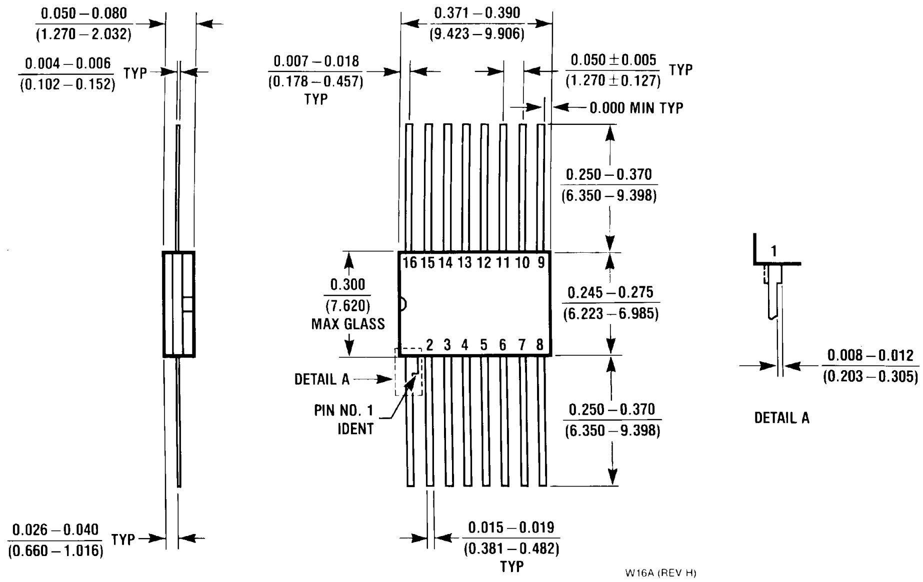


16-Lead Small Outline Molded Package (M)
Order Number DM74LS161AM or DM74LS163AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Numbers DM74LS161AN, DM74LS163AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Numbers 54LS161AFMQB, 54LS163AFMQB, DM54LS161AN or DM54LS163AW
Package Number W16A

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March 1998

DM74LS164
8-Bit Serial In/Parallel Out Shift Register

General Description

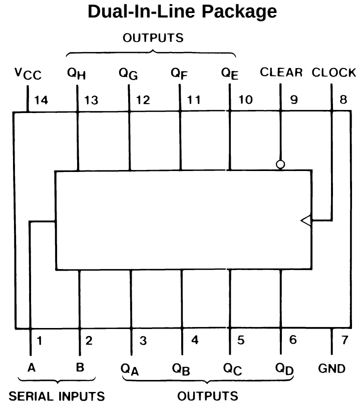
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW

Connection Diagram

Dual-In-Line Package



DS006398-1

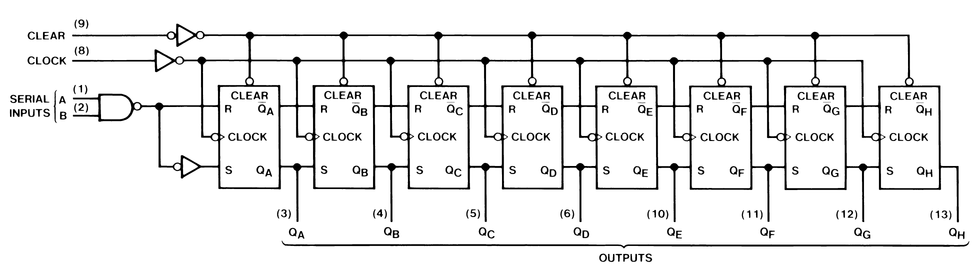
Order Number 54LS164DMQB, 54LS164FMQB, 54LS164LMQB, DM54LS164J, DM54LS164W, DM74LS164M or DM74LS164N
See Package Number E20A, J14A, M14A, N14A or W14B

Function Table

Inputs				Outputs			
Clear	**Clock**	**A**	**B**	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



DS006398-2

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 5)		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
	(Note 5)	Clear	20			20			
t_{SU}	Data Setup Time (Note 5)		17			17			ns
t_H	Data Hold Time (Note 5)		5			5			ns
t_{REL}	Clear Release Time (Note 5)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			16	27	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

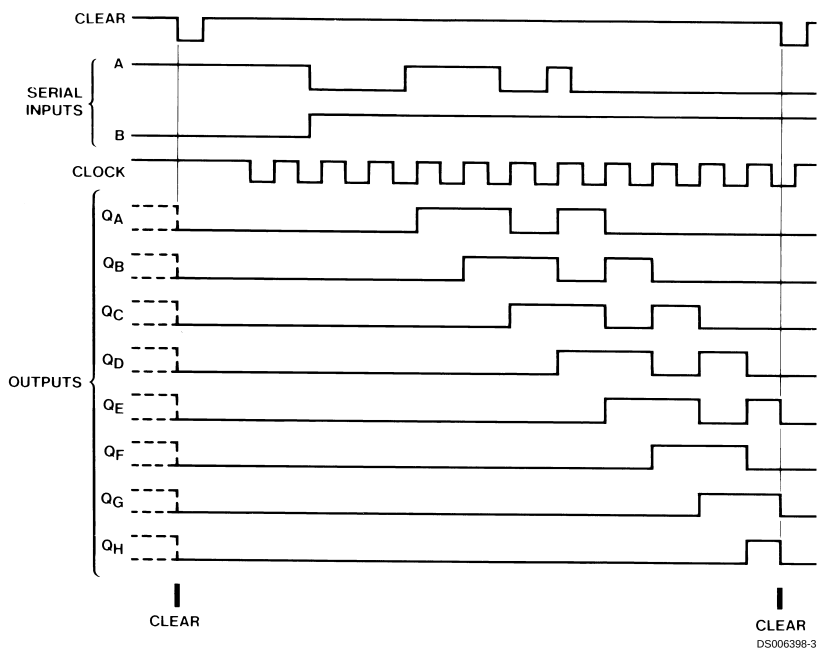
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics

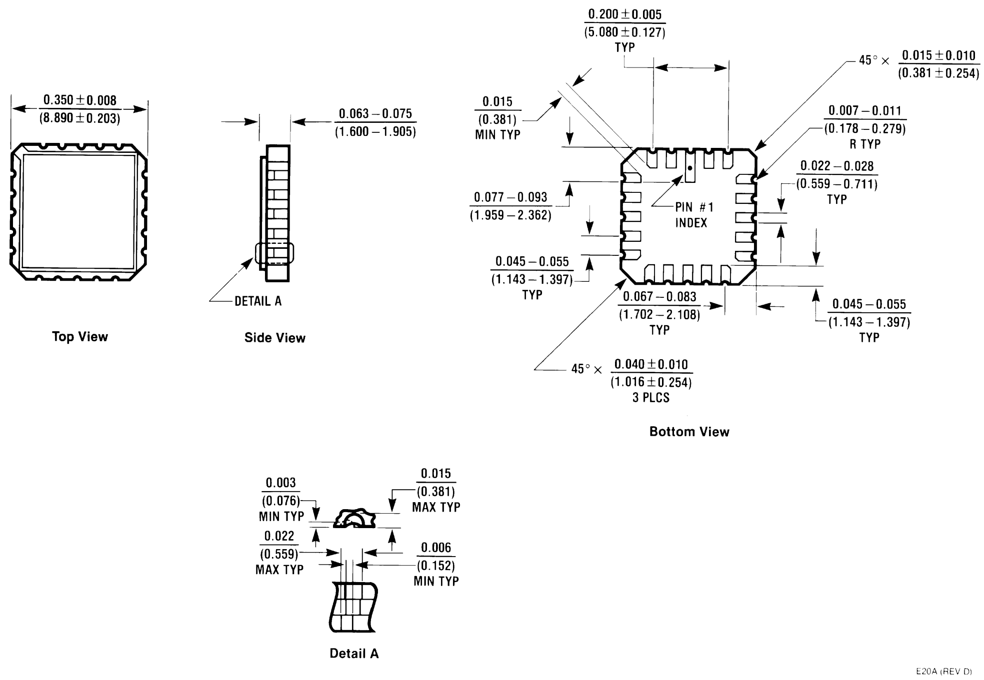
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

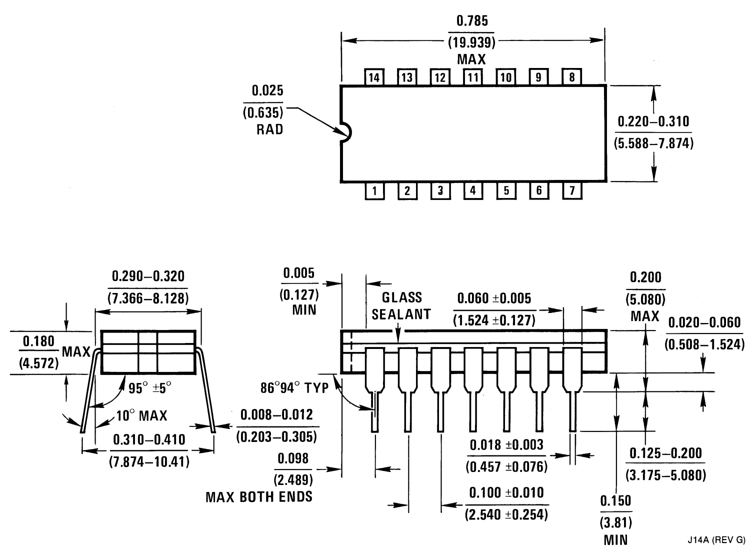
Timing Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

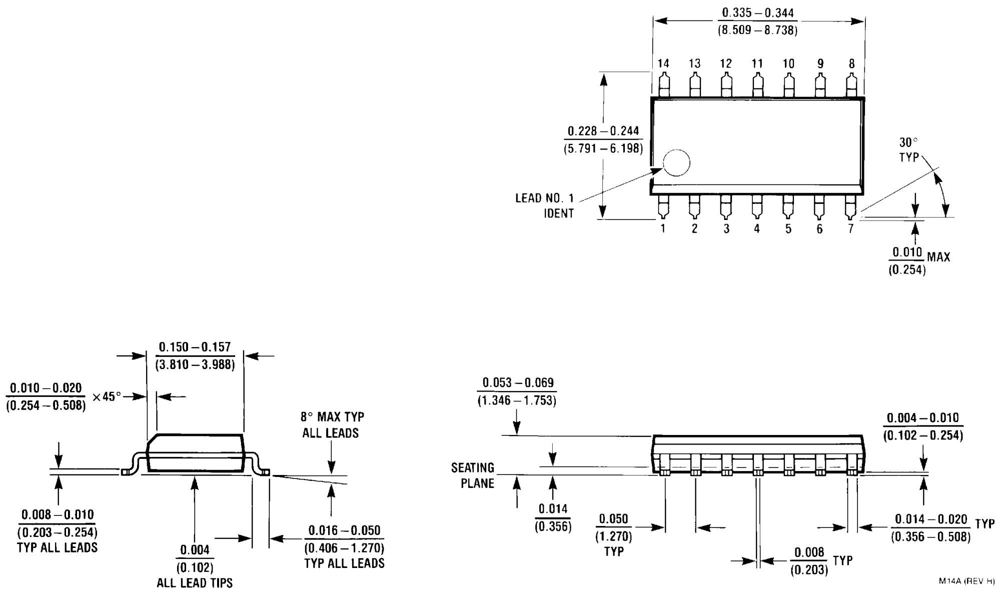


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS164LMQB
Package Number E20A

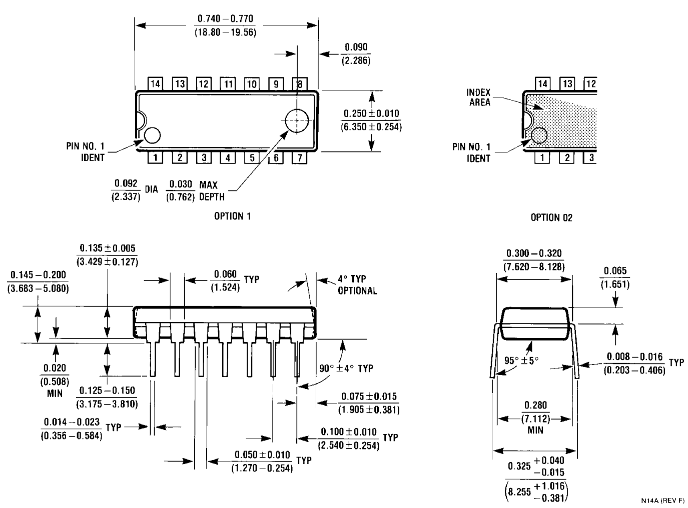


14-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS164DMQB or DM54LS164J
Package Number J14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

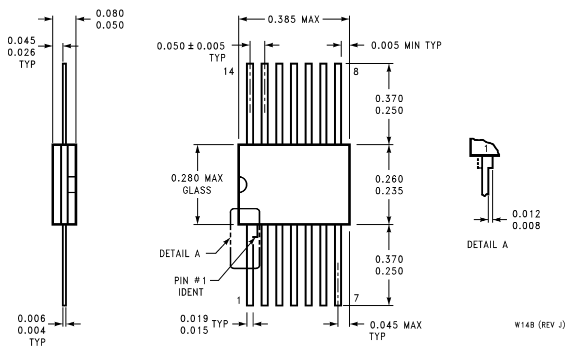


14-Lead Small Outline Molded Package (M)
Order Number DM74LS164M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS164N
Package Number N14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Ceramic Flat Package (W)
Order Number 54LS164FMQB or DM54LS164W
Package Number W14B

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April 1998

DM74LS165
8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

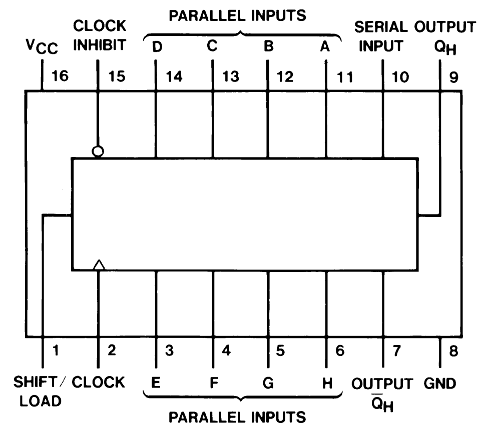
Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Connection Diagram

Dual-In-Line Package



Order Number DM54LS165J, DM54LS165W, DM74LS165WM or DM74LS165N
See Package Number J16A, M16B, N16E or W16A

Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low-to-high level
a...h = The level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS165			DM74LS165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)				30	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)					0		20	MHz
t_W	Pulse Width	Clock	18			25			ns
	(Note 3)	Load	15			15			
t_{SU}	Setup Time	Parallel	10			10			
	(Note 7)	Serial	10			20			ns
		Enable	10			30			
		Shift	10			45			
t_H	Hold Time (Note 7)		5			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5			V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max				0.4	
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max, V_I = 7V (DM74)	Shift/Load			0.3	mA
	Input Voltage	V_I = 10V (DM54)	Others			0.1	
I_{IH}	High Level Input	V_{CC} = Max	Shift/Load			60	μA
	Current	V_I = 2.7V	Others			20	
I_{IL}	Low Level Input	V_{CC} = Max	Shift/Load			−1.2	mA
	Current	V_I = 0.4V	Others			−0.4	
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 5)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			21	36	mA

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 4: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

Electrical Characteristics (Continued)

Note 7: $T_A = 25°C$ and $V_{CC} = 5V$.

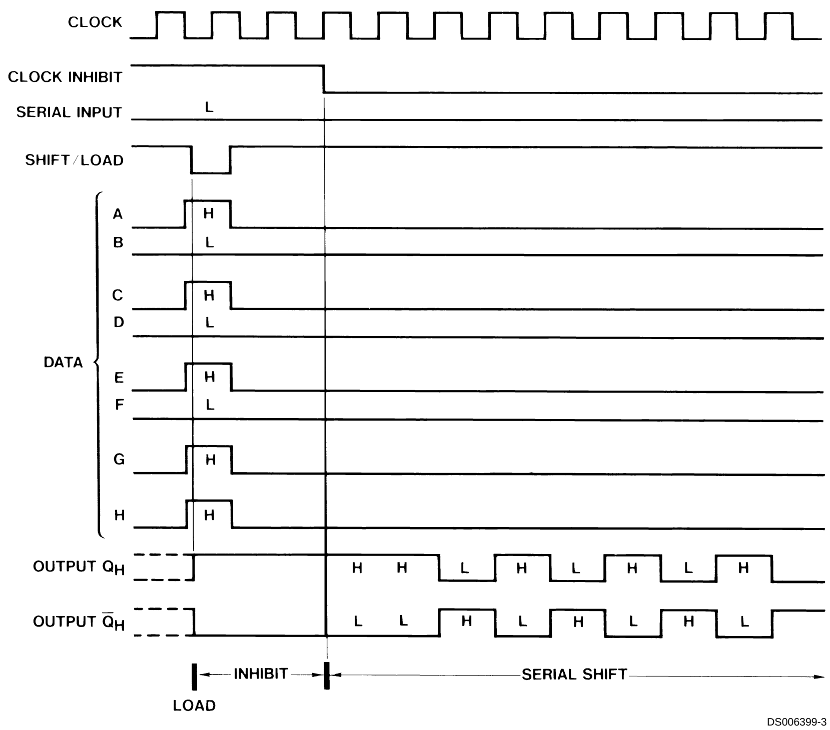
Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$

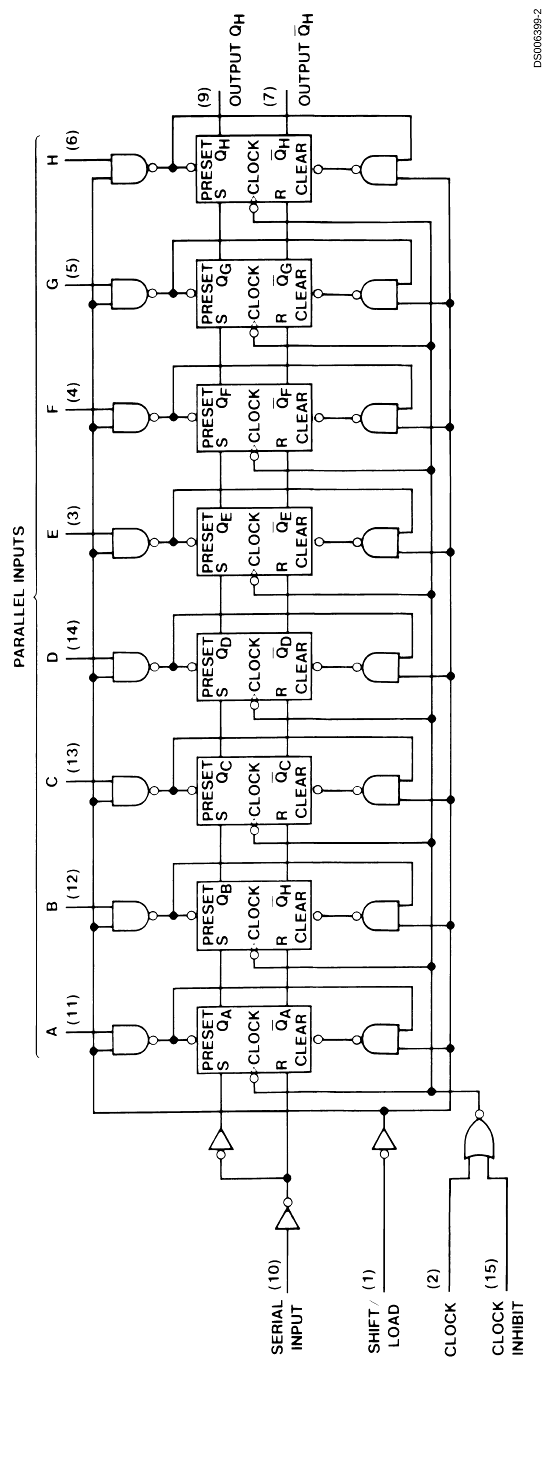
Symbol	Parameter	From (Input) To (Output)	DM54LS $C_L = 15$ pF		DM74LS $C_L = 15$ pF		DM74LS $R_L = 2$ kΩ $C_L = 50$ pF		Units
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		30		35		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		30		35		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		30		40		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		30		40		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		20		25		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		30		30		37	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		30		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		25		25		32	ns

Timing Diagram

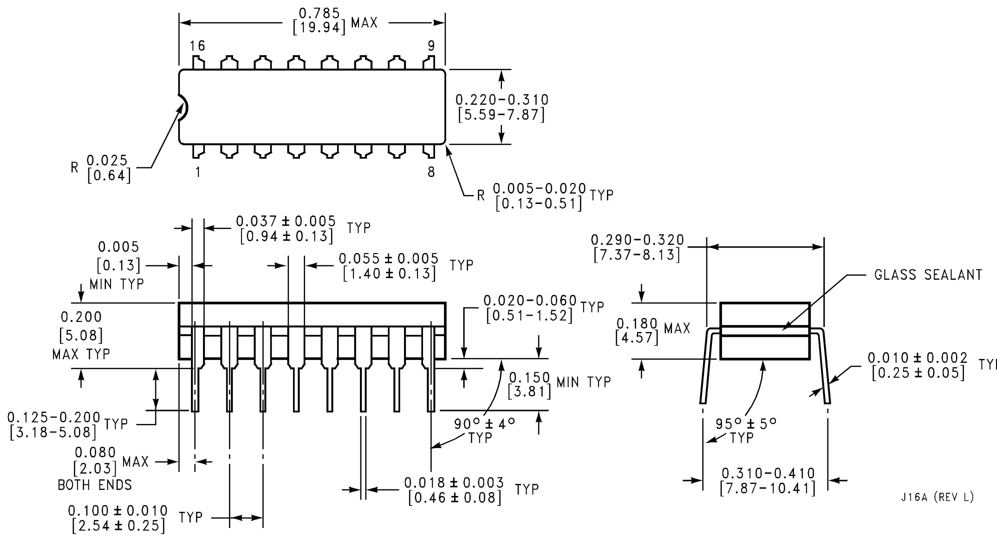
Typical Shift, Load, and Inhibit Sequences



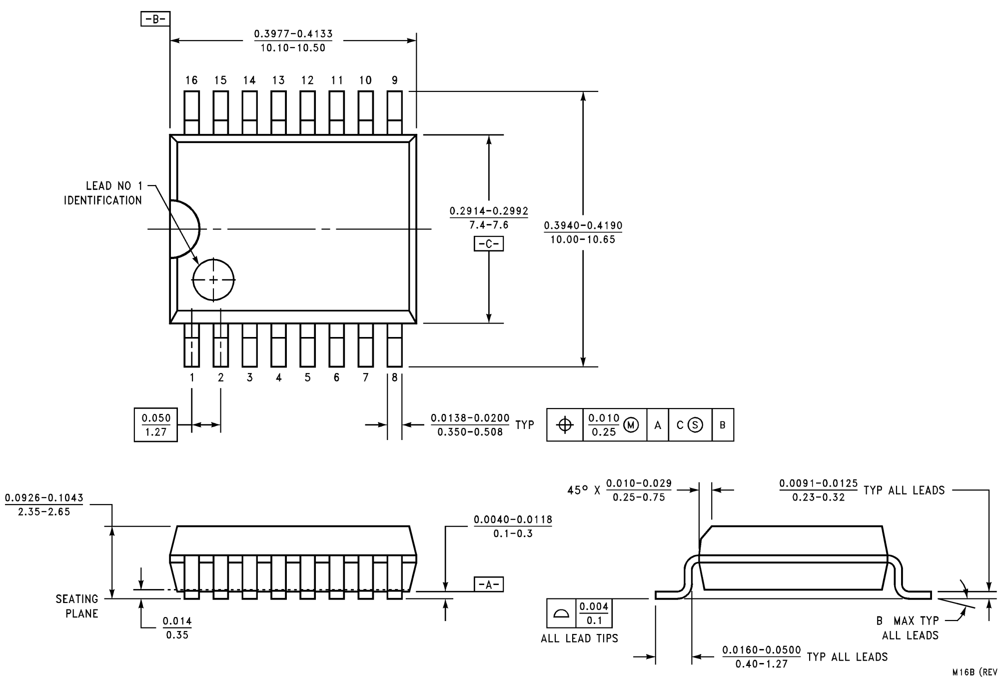
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

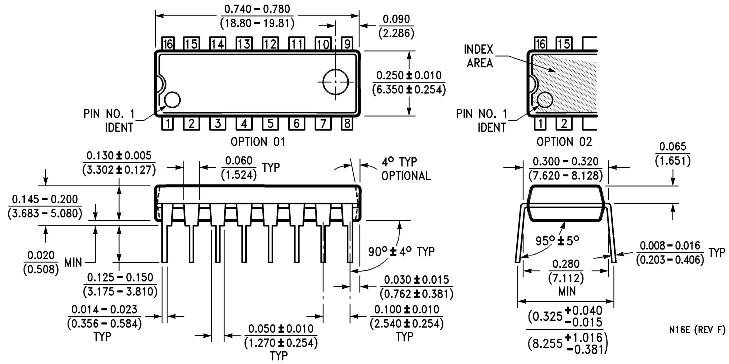


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS165J
Package Number J16A

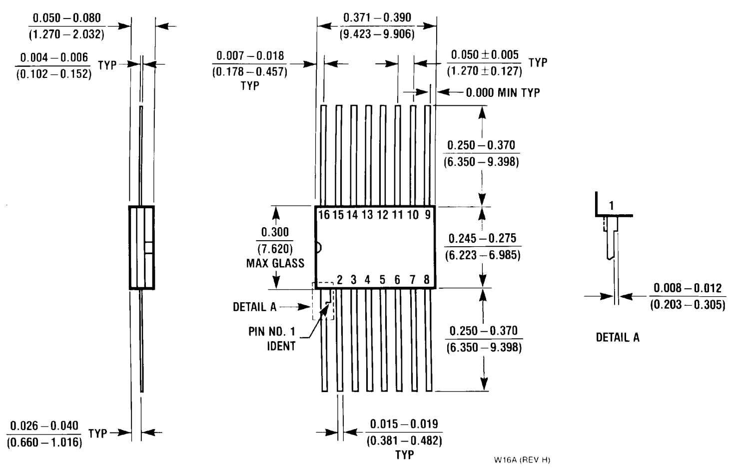


16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS165WM
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS165N
Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS165W
Package Number W16A

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April 1998

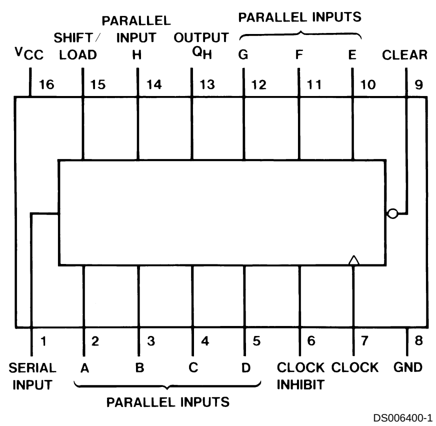
DM74LS166
8-Bit Parallel-In/Serial-Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



Order Number DM74LS166WM or DM74LS166N
See Package Number M16B or N16A

Function Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A…H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a…h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a…h = The level of steady-state input at inputs A through H, respectively
Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Gn}, = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM74LS166 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	MHz
	Clock Frequency (Note 3)		0		20	MHz
t_W	Pulse Width (Note 7)	Clock	20			ns
		Clear	20			
t_{SU}	Setup Time (Note 7)	Mode	30			ns
		Data	20			
t_H	Hold Time (Note 7)		0			ns
T_A	Free Air Operating Temperature		0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 6)		22	38	mA

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V is applied to the CLOCK.

Note 7: T_A = 25˚C and V_{CC} = 5V.

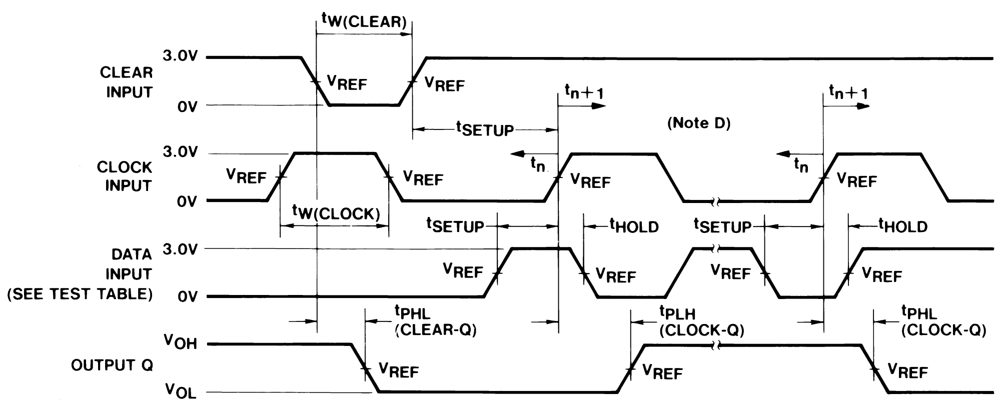
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	35		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	35		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output	6	30		36	ns

Parameter Measurement Information

Voltage Waveforms



DS006400-2

Test Table for Synchronous Inputs

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq$ 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq$ 20 ns and t_{HOLD} = 0 ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

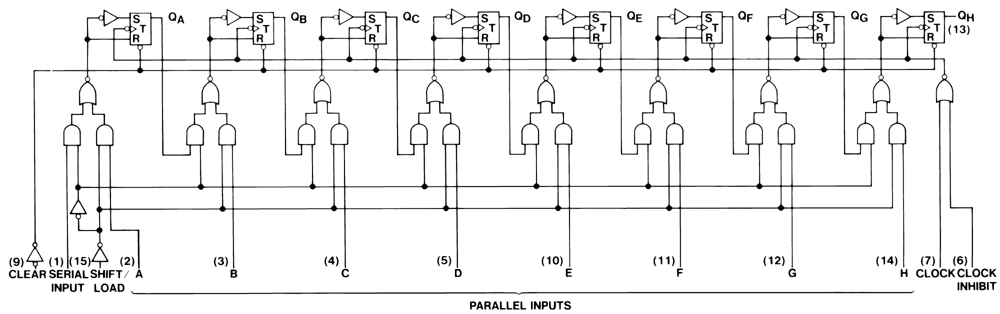
Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: V_{REF} = 1.3V.

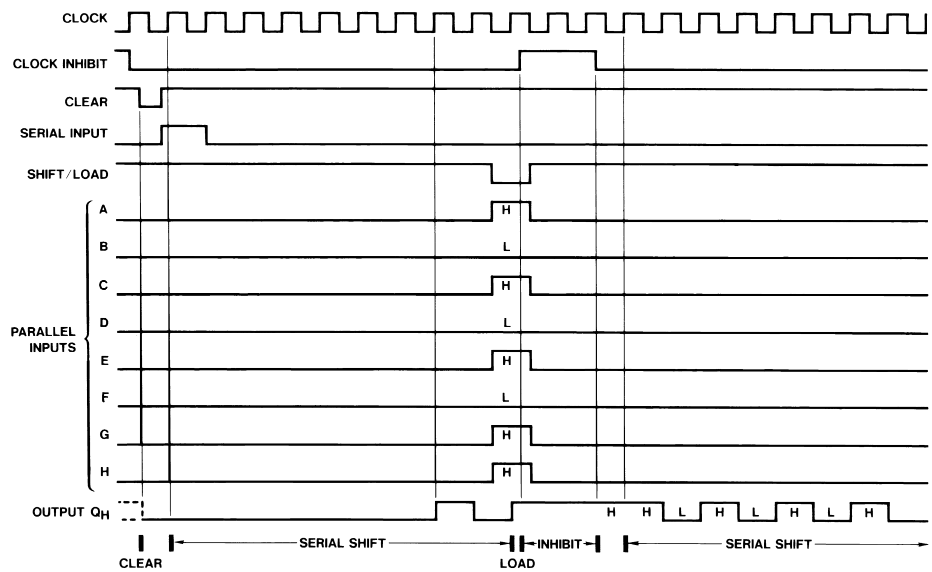
Logic Diagram



DS006400-3

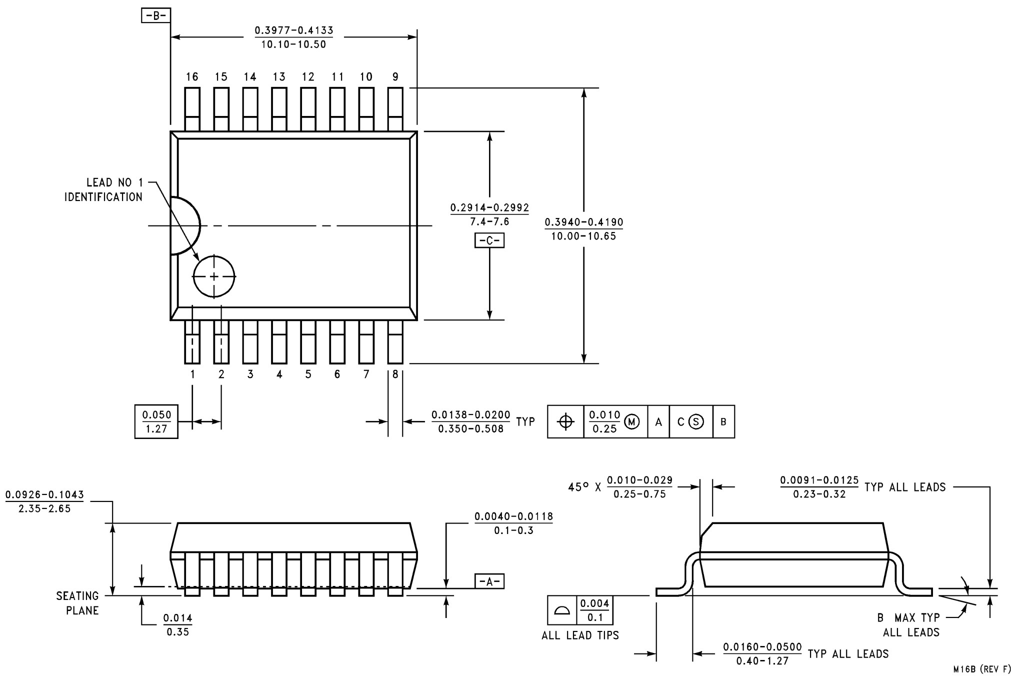
Timing Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences

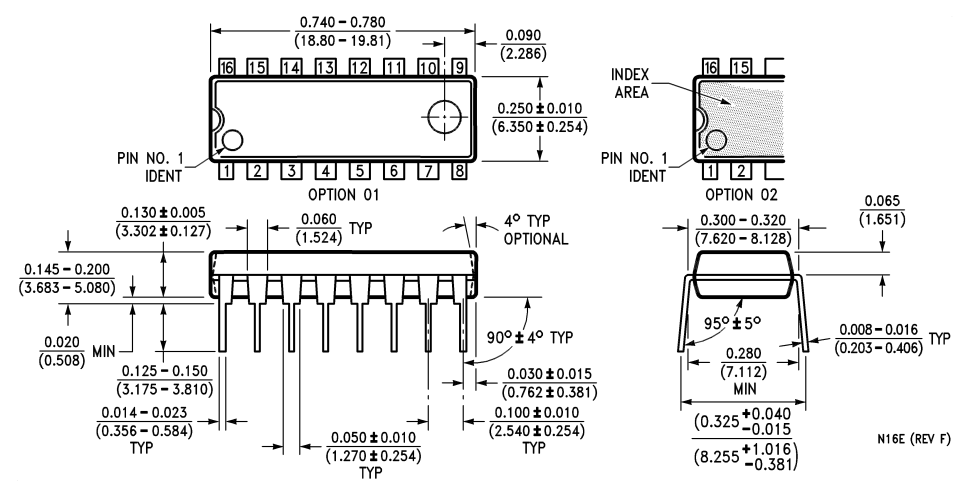


DS006400-4

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS166WM
Package Number M16B



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS166N
Package Number N16E

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April 1998

FAIRCHILD SEMICONDUCTOR ™

DM74LS169A
Synchronous 4-Bit Up/Down Binary Counter

General Description

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

This counter is fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

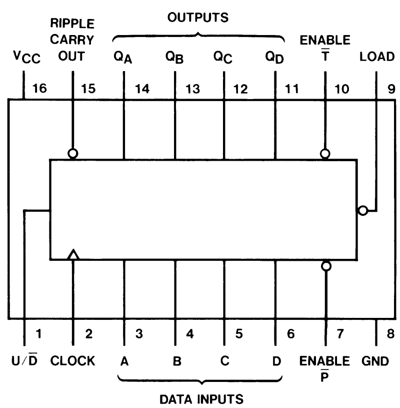
This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit

Connection Diagram

Dual-In-Line Package



DS006401-1

Order Number 54LS169DMQB, 54LS169FMQB, 54LS169LMQB, DM54LS169AJ, DM54LS169AW, DM74LS169AM or DM74LS169AN
See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS169A			DM74LS169A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Clock Pulse Width (Note 4)		25			25			ns
t_{SU}	Setup Time (Note 4)	Data	20			20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			20			ns
		Load	25			25			ns
		U/D	30			30			ns
t_H	Hold Time (Note 4)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 4: T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max	Enable $\overline{T}$			0.2	mA
		V_I = 7V	Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	Enable $\overline{T}$			40	µA
		V_I = 2.7V	Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max	Enable $\overline{T}$			−0.8	mA
		V_I = 0.4V	Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 6)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max(Note 7)			20	34	mA

Note 5: All typicals are at V_{CC} = 5V and T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.

Switching Characteristic

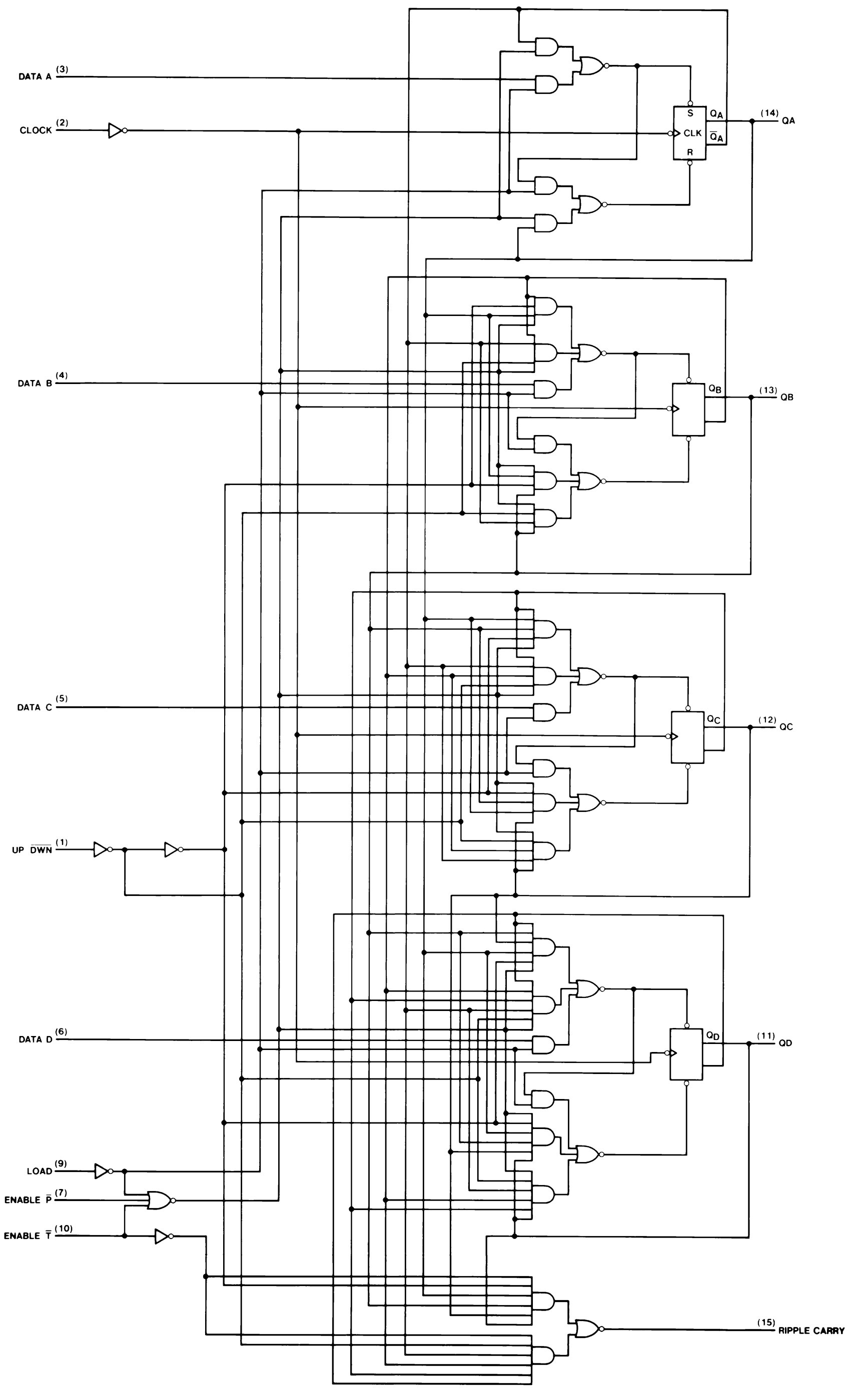
at V_{CC} = 5V and T_A = 25˚C (for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		35		39	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		23		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable $\overline{T}$ to Ripple Carry		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable $\overline{T}$ to Ripple Carry		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Carry (Note 8)		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Carry (Note 8)		29		38	ns

Note 8: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

Logic Diagram

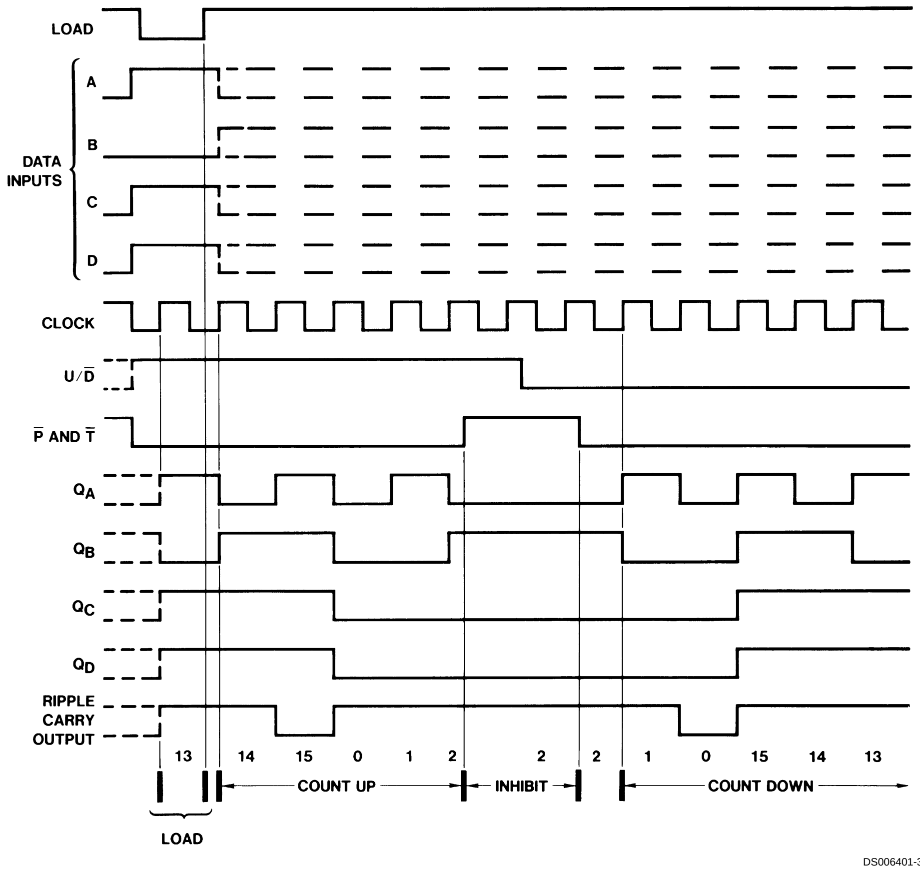
LS169A Binary Counter



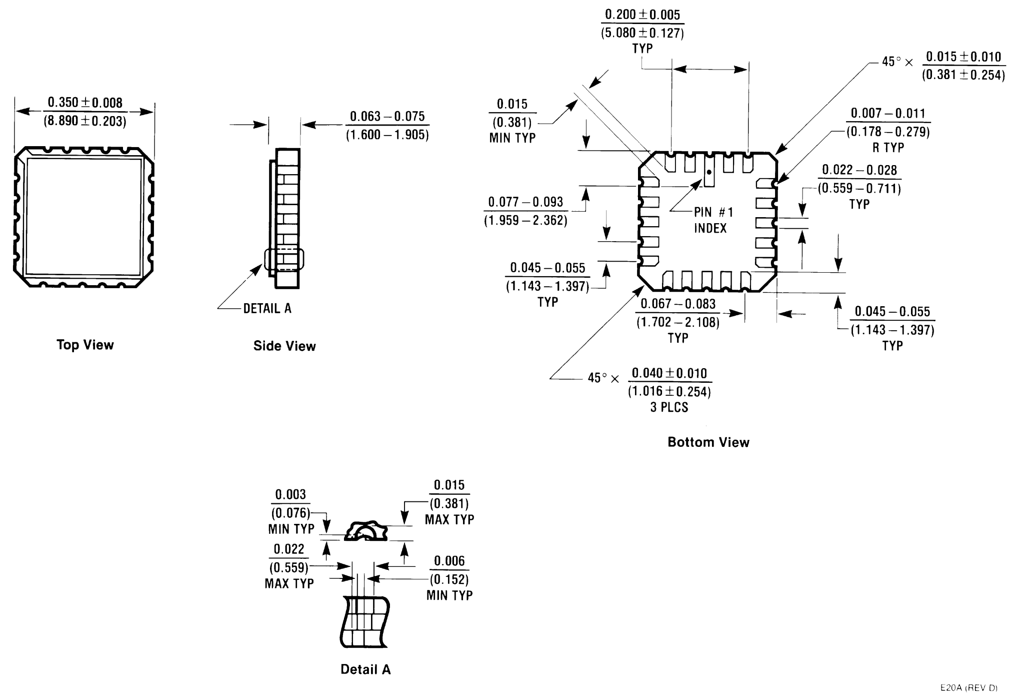
DS006401-2

Timing Diagram

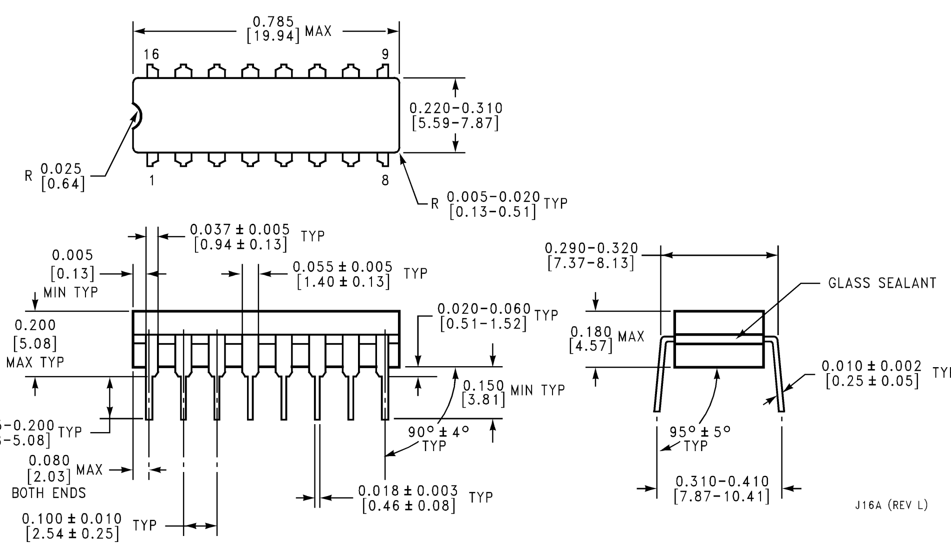
LS169A Binary Counters
Typical Load, Count, and Inhibit Sequences



Physical Dimensions inches (millimeters) unless otherwise noted

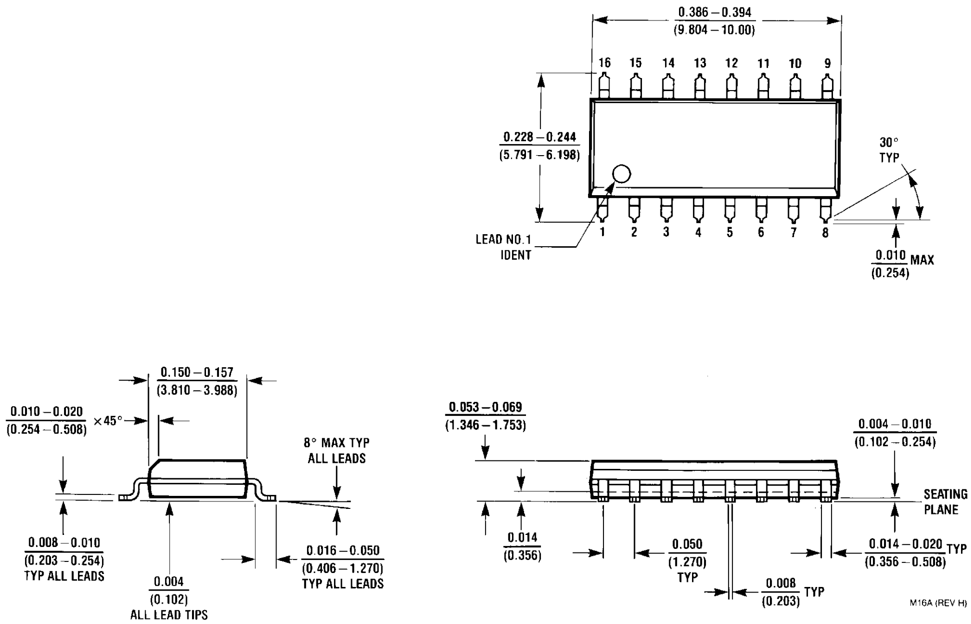


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS169LMQB
Package Number E20A

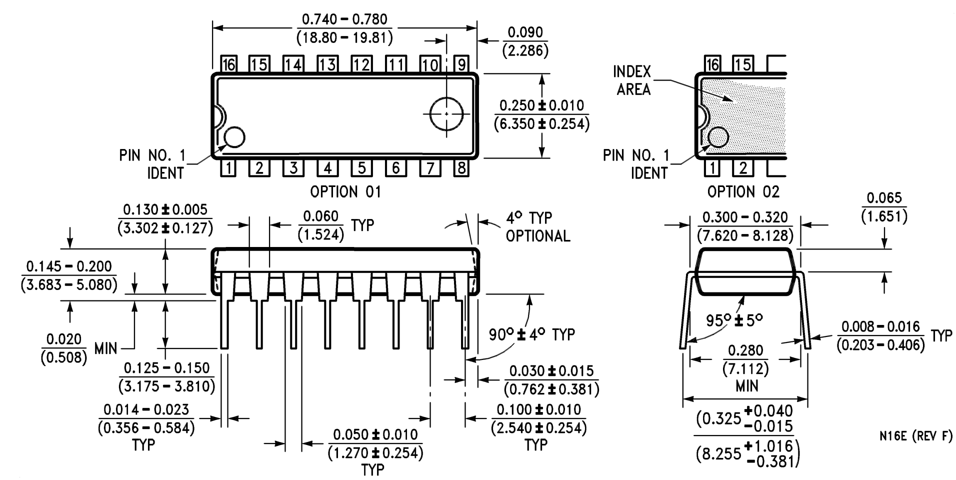


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS169DMQB or DM54LS169AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

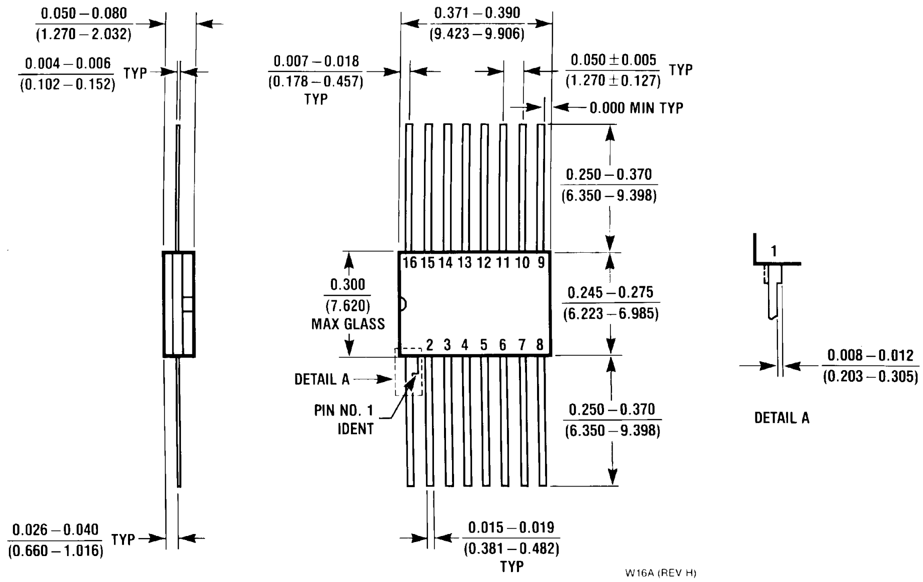


16-Lead Small Outline Molded Package (M)
Order Number DM74LS169AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS169AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS169FMQB or DM54LS169AW
Package Number W16A

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National Semiconductor

January 1992

DM74LS170
4 x 4 Register File with Open-Collector Outputs

General Description

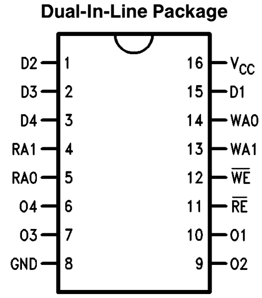
The 'LS170 contains 16 high speed, low power, transparent D-type latches arranged as four words of four bits each, to function as a 4 × 4 register file. Separate read and write inputs, both address and enable, allow simultaneous read and write operation. Open-collector outputs make it possible to connect up to 128 outputs in a wired-AND configuration to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length. The '670 provides a similar function to this device but it features TRI-STATE® outputs.

Features

- Simultaneous read/write operation
- Expandable to 512 words of n-bits
- Typical access time of 20 ns
- Low leakage open-collector outputs for expansion

Connection Diagram

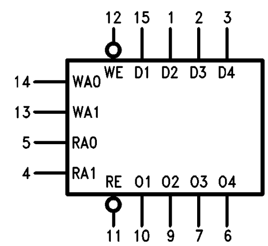
Dual-In-Line Package



TL/F/9820–1

Order Number DM74LS170WM or DM74LS170N
See NS Package Number M16B or N16E

Logic Symbol



TL/F/9820–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
D1–D4	Data Inputs
WA0–WA1	Write Address Inputs
$\overline{WE}$	Write Enable Input (Active LOW)
RA0, RA1	Read Address Inputs
$\overline{RE}$	Read Enable Input (Active LOW)
O1–O4	Data Outputs

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 RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS170			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s	Setup Time HIGH or LOW Dn to Rising $\overline{WE}$	10			ns
t_h	Hold Time HIGH or LOW Dn to Rising $\overline{WE}$	5.0			ns
t_s	Setup Time HIGH or LOW WAn to Falling $\overline{WE}$	10			ns
t_h	Hold Time HIGH or LOW WAn to Rising $\overline{WE}$	5.0			ns
t_w(L)	$\overline{WE}$ or $\overline{RE}$ Pulse Width LOW	25			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Uints
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V				20	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Dns, RAO, WA0			0.1	mA
			$\overline{WE}$, $\overline{RE}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{RE}$, $\overline{WE}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	$\overline{RE}$, $\overline{WE}$	−0.06		−0.8	mA
			RA1, WA1	−0.05		−0.4	
			DATA, RA0, WA0	−0.03		−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM74	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, Dn, $\overline{WE}$, $\overline{RE}$ = 4.5V, WAn, RAn = GND				40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	Conditions	$R_L = 2k$, $C_L = 15$ pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay* RA0 or RA1 to On			35 35	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{RE}$ to On			30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{WE}$ to On			35 35	ns
t_{PLH} t_{PHL}	Propagation Delay Dn to On			35 35	ns

*Measured at least 25 ns after entry of new data at selected location.

Switching Waveforms

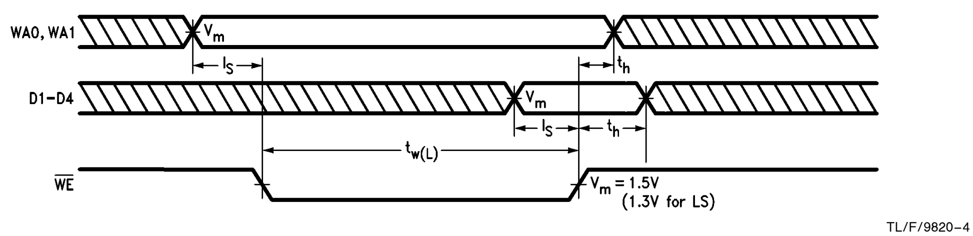


FIGURE a

Write Function Table

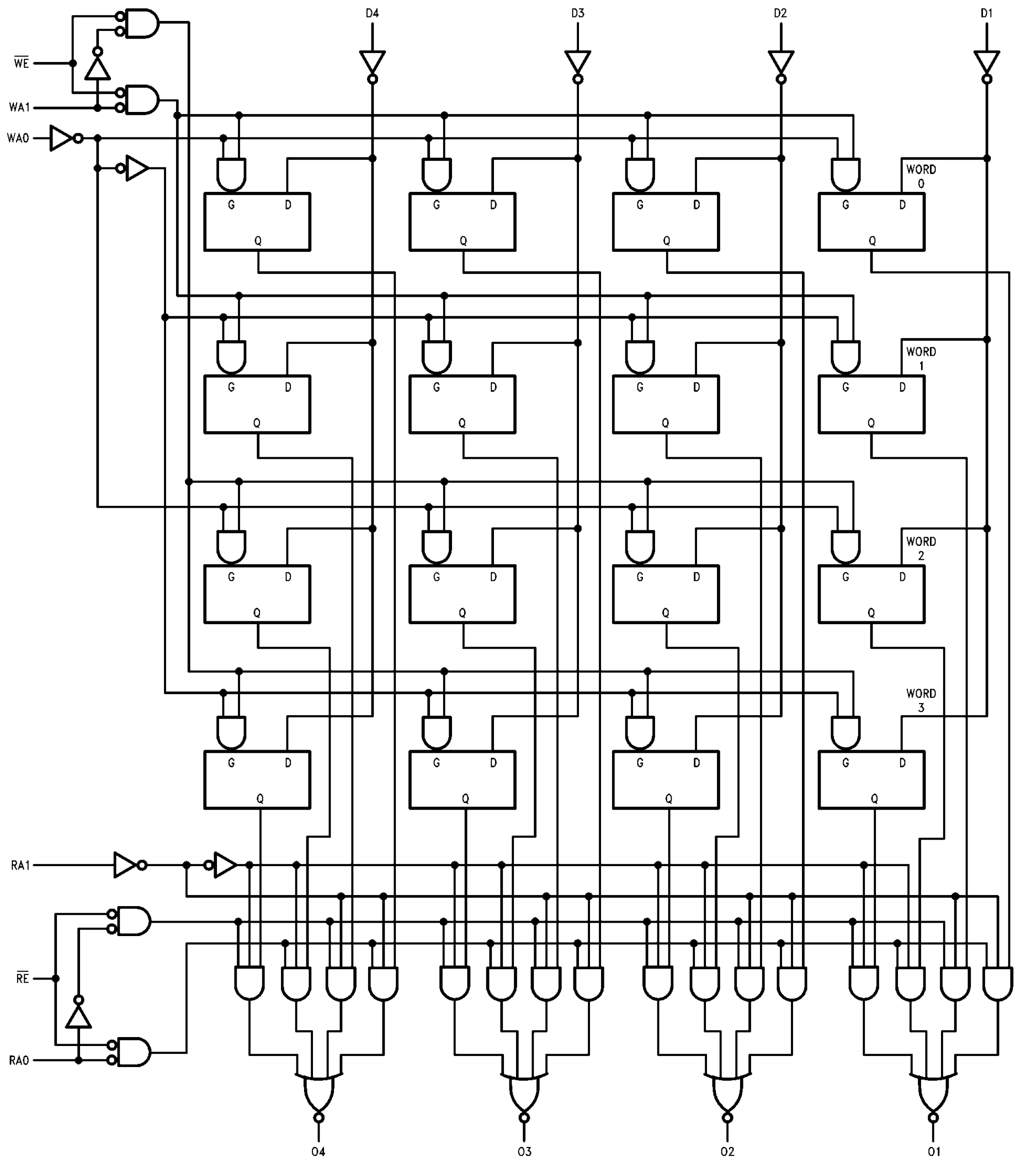
Write Inputs			D Inputs to
$\overline{WE}$	WA1	WA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (Hold)

Read Function Table

Read Inputs			Outputs from
$\overline{RE}$	RA1	RA0	
L	L	L	Word 0
L	L	H	Word 1
L	H	L	Word 2
L	H	H	Word 3
H	X	X	None (High Z)

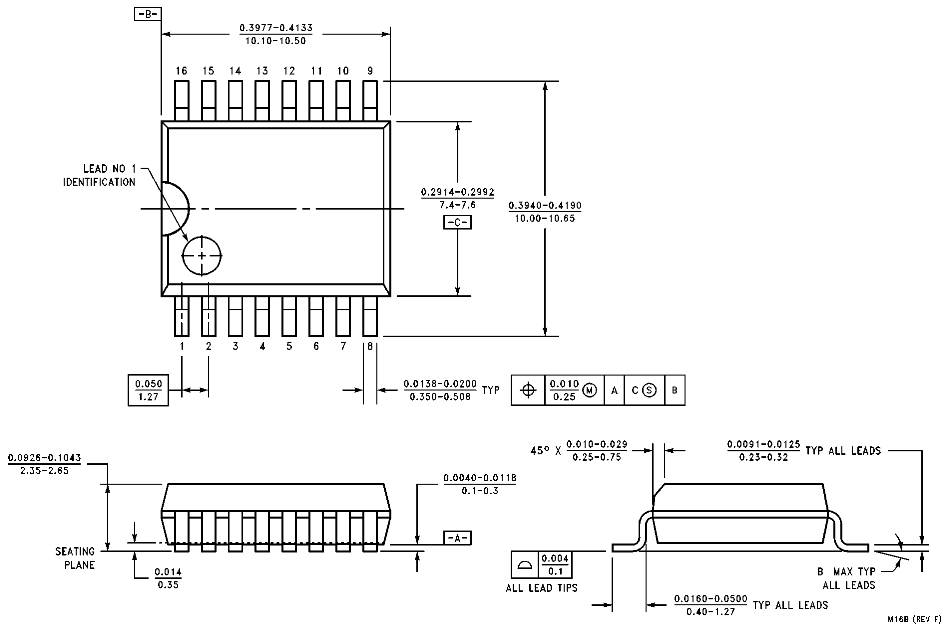
H = HIGH Voltage Level L = LOW Voltage Level X = Immaterial

Logic Diagram



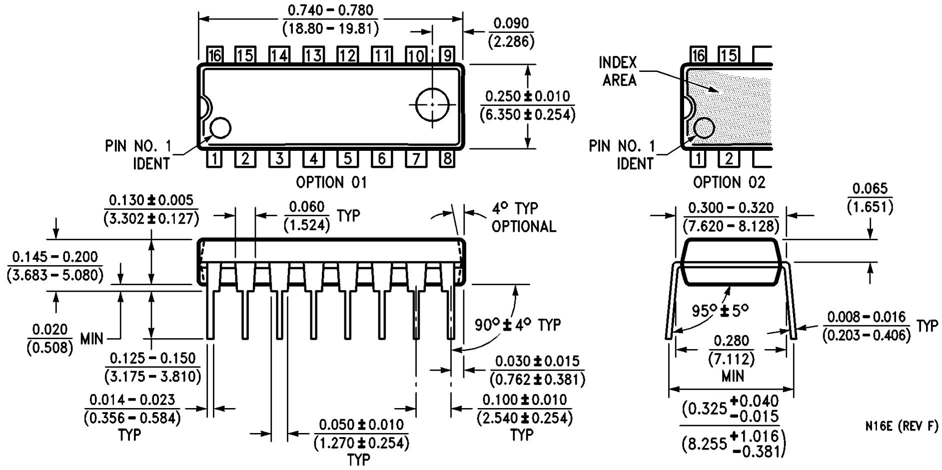
TL/F/9820–3

Physical Dimensions inches (millimeters)



16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS170WM
NS Package Number M16B

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS170N (N)
NS Package Number N16E

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National Semiconductor

May 1992

54LS173/DM74LS173A TRI-STATE® 4-Bit D-Type Register

General Description

This four-bit register contains D-type flip-flops with totem-pole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

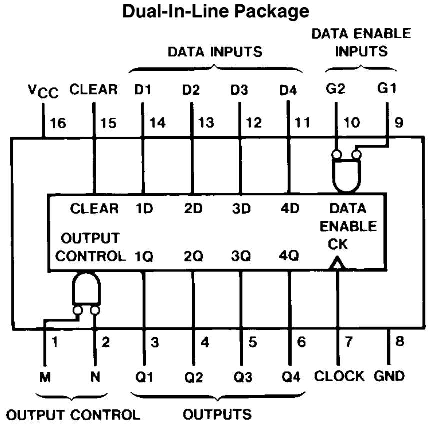
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  Parallel load
  Do nothing (hold)
- For application as bus buffer registers

Connection Diagram

Dual-In-Line Package



TL/F/6403–1

Order Number 54LS173DMQB, 54LS173FMQB, 54LS173LMQB, DM74LS173AM or DM74LS173AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs					Output Q
Clear	Clock	Data Enable		Data D	
		G1	G2		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H
When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.					

H = High Level (Steady State)
L = Low Level (Steady State)
↑ = Low-to-High Level Transition
X = Don't Care (Any Input Including Transitions)
Q_0 = The Level of Q Before the Indicated Steady State Input Conditions Were Established.

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS173			DM74LS173A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 1)		30			0		30	MHz
	Clock Frequency (Note 2)					0		20	MHz
t_W	Pulse Width (Note 3)	Clock	20			17			ns
		Clear	17			17			
t_{SU}	Setup Time (Note 3)	Enable	17			23			ns
		Data	15			15			
t_H	Hold Time (Note 3)	Enable	0			0			ns
		Data	5			0			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			17	30	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			$C_L = 50$ pF		$C_L = 50$ pF, $R_L = 667\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		28		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		28		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30		30	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control (M or N) to Any Q		23		26	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control (M or N) to Any Q		28		24	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 7)	Output Control (M or N) to Any Q		17		17	ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 7)	Output Control (M or N) to Any Q		23		25	ns

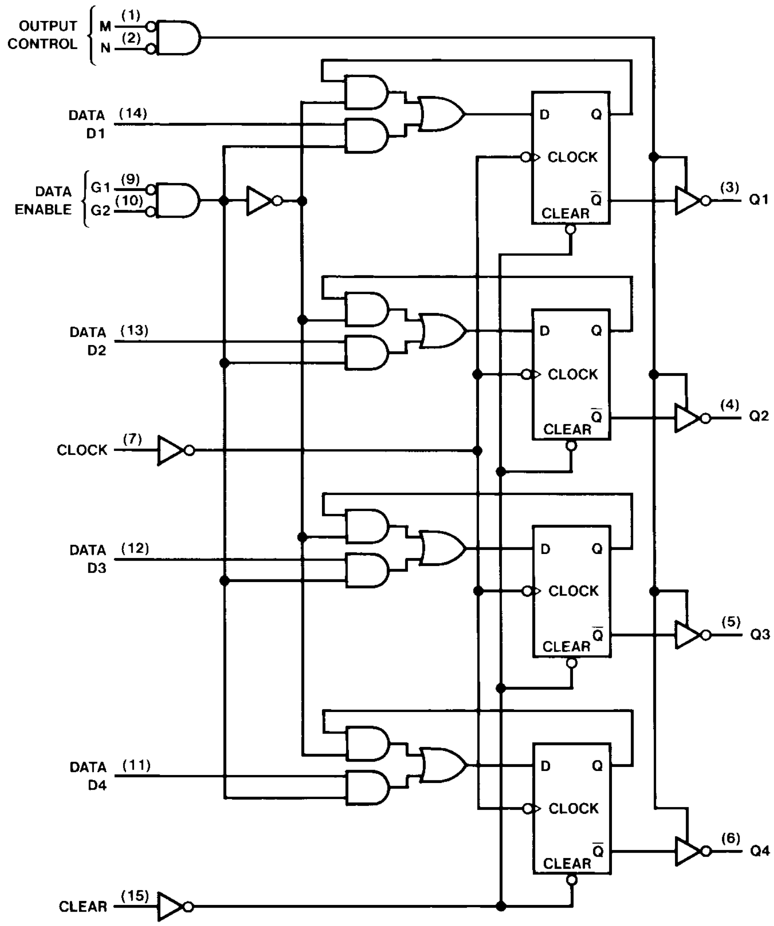
Note 4: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded: and the CLOCK and M input at 4.5V.

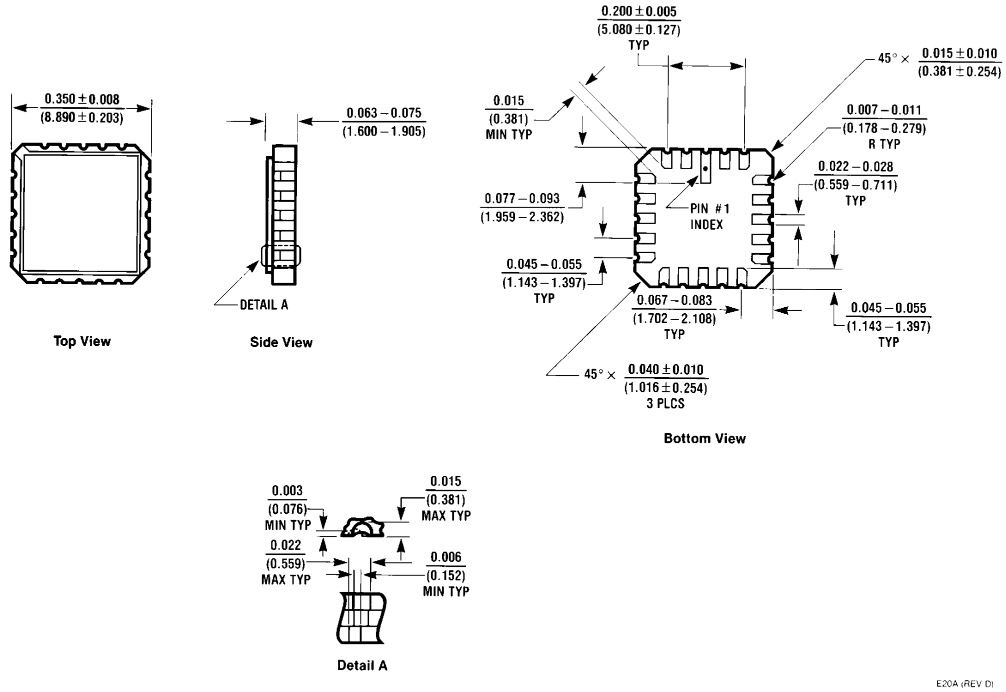
Note 7: $C_L = 5$ pF.

Logic Diagram

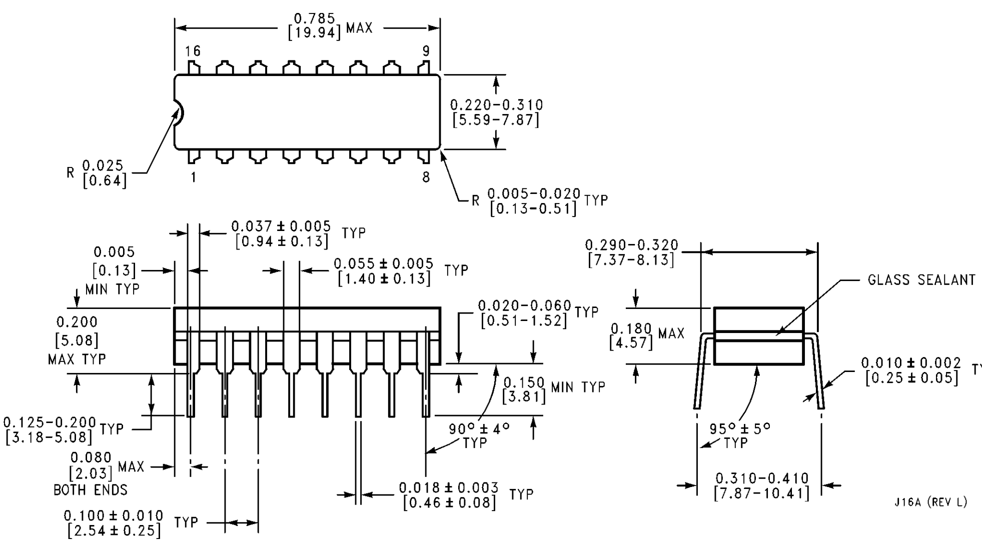


TL/F/6403–2

Physical Dimensions inches (millimeters)

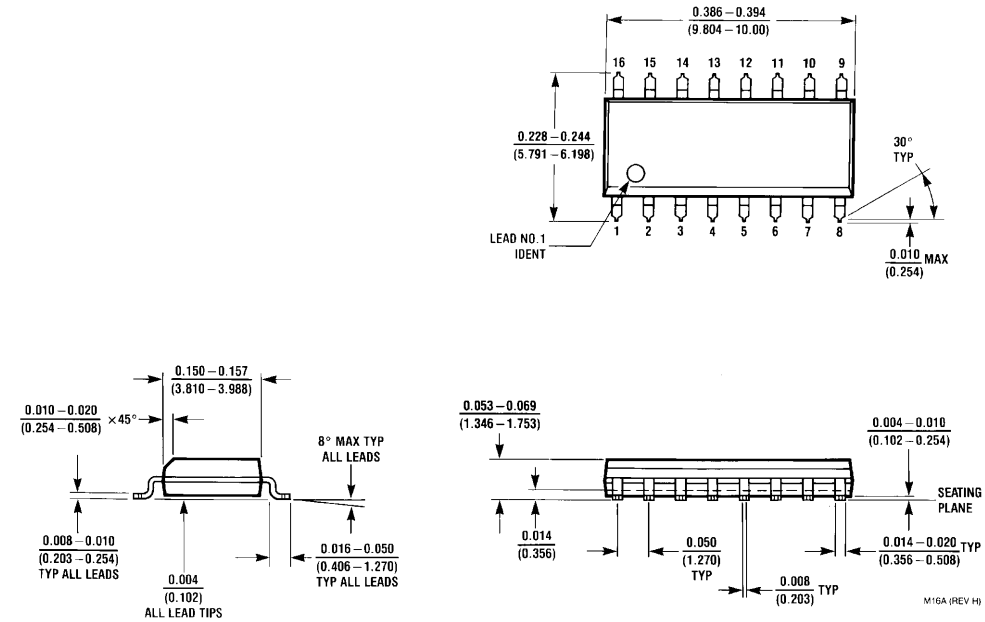


Chip Carrier Package (E)
Order Number 54LS173LMQB
NS Package Number E20A

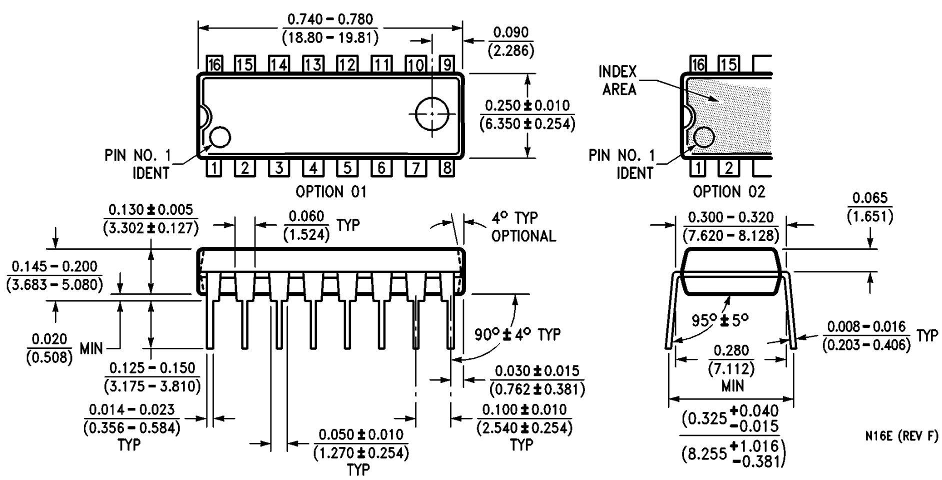


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS173DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

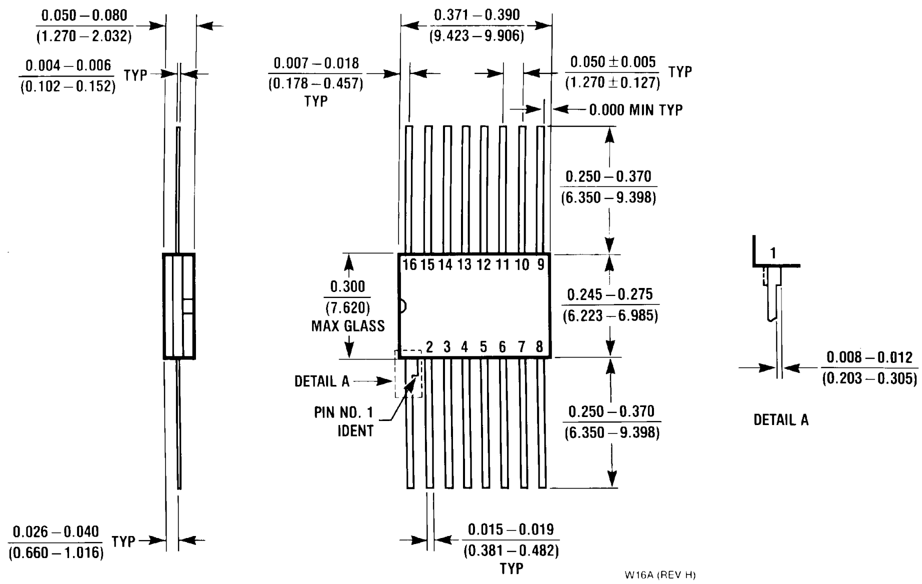


16-Lead Small Outline Molded Package (M)
Order Number DM74LS173AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS173AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS173FMQB
NS Package Number W16A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD SEMICONDUCTOR ™

April 1998

DM74LS174/DM74LS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

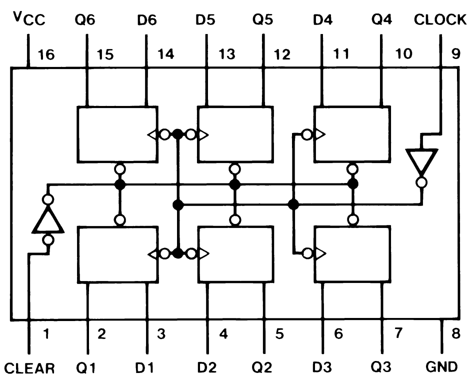
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- LS174 contains six flip-flops with single-rail outputs
- LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW
- Alternate Military/Aerospace device (54LS174, 54LS175) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

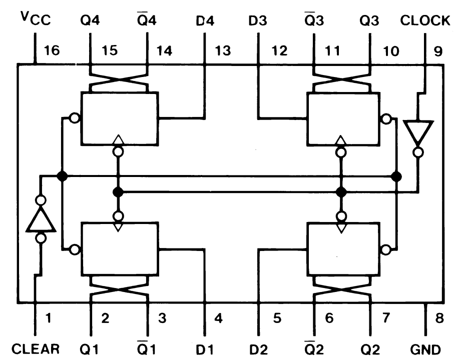
Dual-In-Line Package



DS006404-1

Order Number 54LS174DMQB, 54LS174FMQB, 54LS174LMQB, DM54LS174J, DM54LS174W, DM74LS174M or DM74LS174N
See Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



DS006404-2

Order Number 54LS175DMQB, 54LS175FMQB, 54LS175LMQB, DM54LS175J DM54LS175W, DM74LS175M or DM74LS175N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$ †
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = LS175 only

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS174			DM74LS174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width	Clock	20			20			ns
	(Note 7)	Clear	20			20			
t_{SU}	Data Setup Time (Note 7)		20			20			ns
t_H	Data Hold Time (Note 7)		0			0			ns
t_{REL}	Clear Release Time (Note 7)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

'LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input	V_{CC} = Max	Clock			−0.4	
	Current	V_I = 0.4V	Clear			−0.4	mA
			Data			−0.36	
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 5)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			16	26	mA

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

Note 7: T_A = 25˚C and V_{CC} = 5V.

'LS174 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		30		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35		42	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS175			DM74LS175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 8)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 9)		0		25	0		25	MHz
t_W	Pulse Width (Note 10)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 10)		20			20			ns
t_H	Data Hold Time (Note 10)		0			0			ns
t_{REL}	Clear Release Time (Note 10)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 8: C_L = 15 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 9: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 10: T_A = 25˚C and V_{CC} = 5V.

’LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 11)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	Clock			−0.4	mA
		V_I = 0.4V	Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 12)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 13)			11	18	mA

’LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C (See Section 1 for Test Waveforms and Output Load)

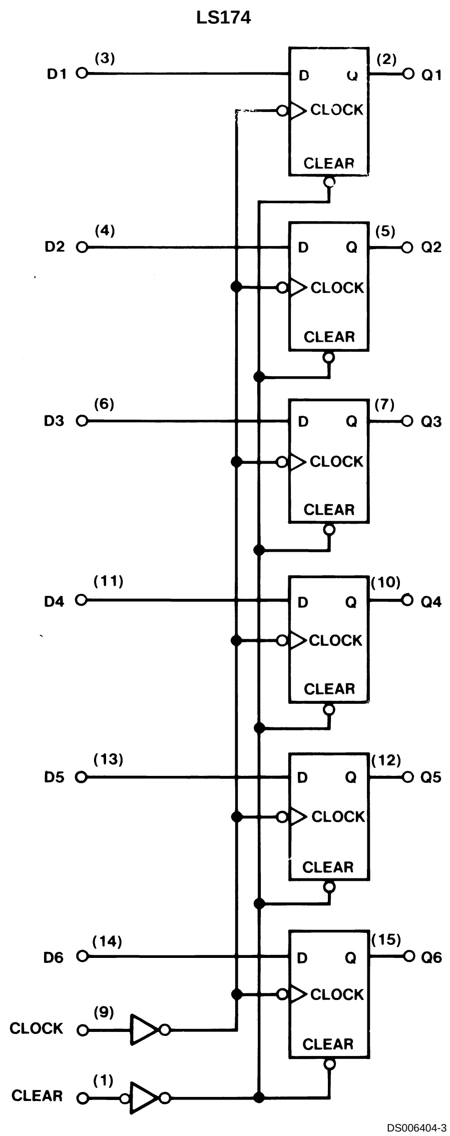
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35		42	ns

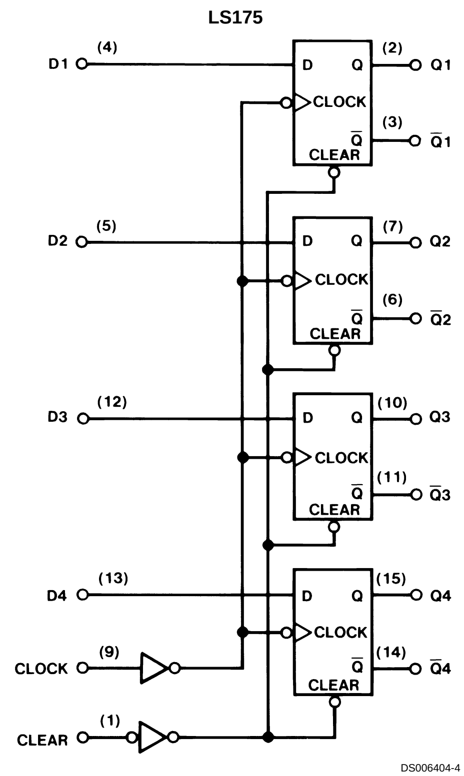
Note 11: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 12: Not more than one output should be shorted at a time, and the duration should not exceed one second.

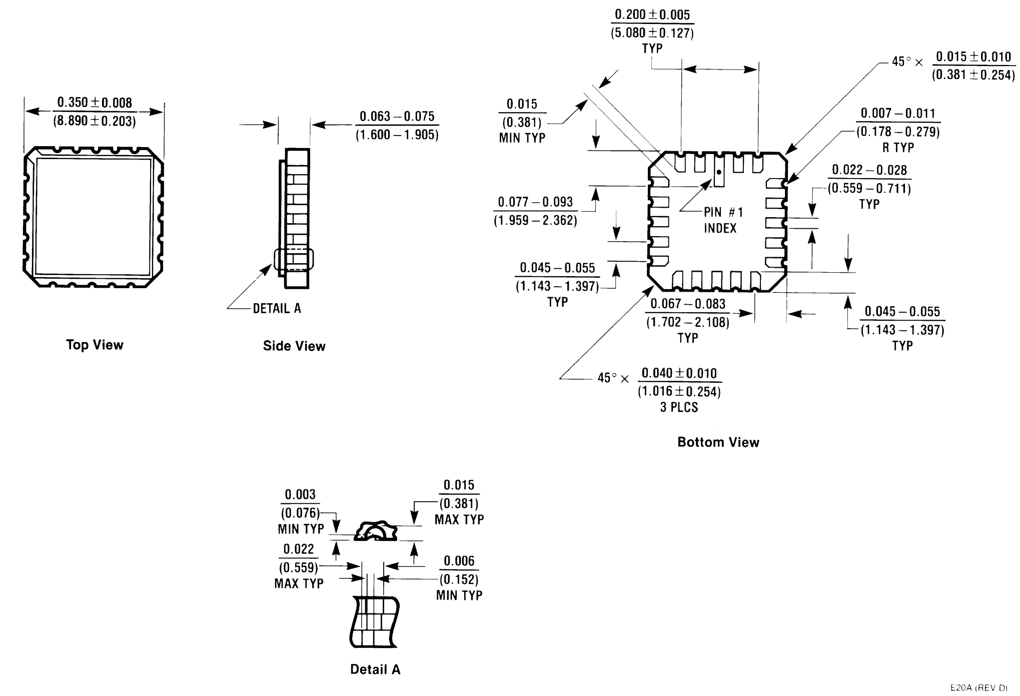
Note 13: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

Logic Diagrams

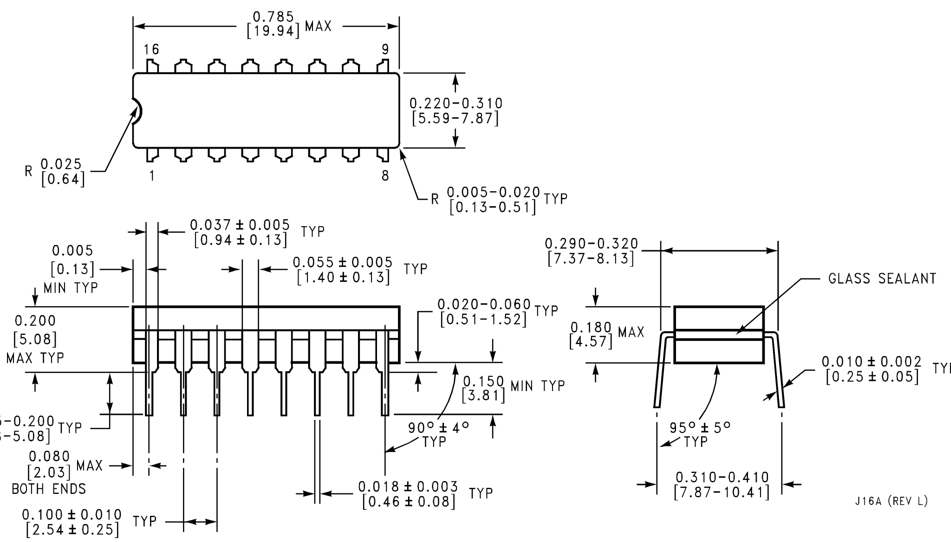




Physical Dimensions inches (millimeters) unless otherwise noted

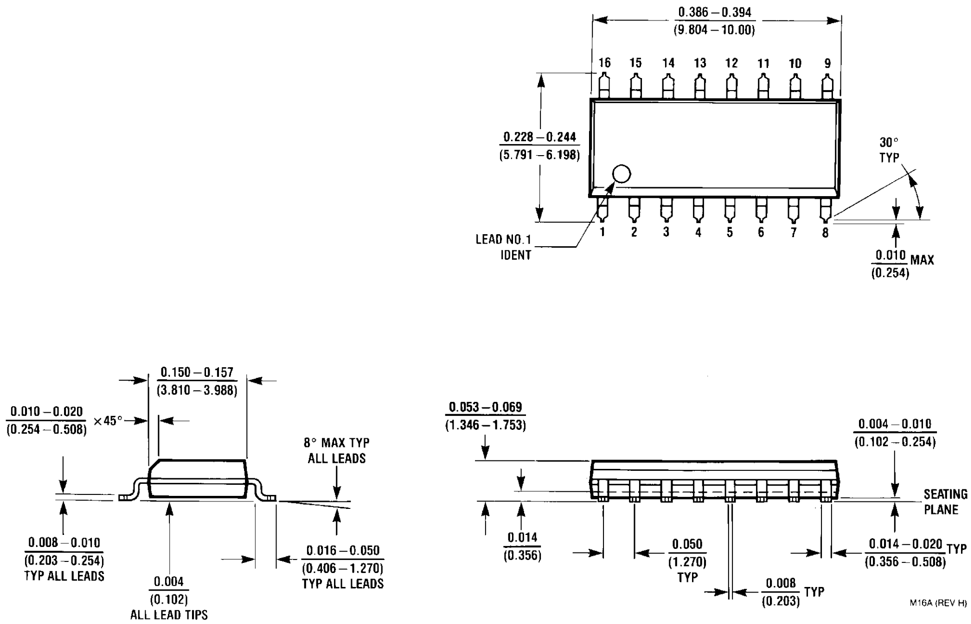


Ceramic Leadless Chip Carrier (E)
Order Number 54LS174LMQB or 54LS175LMQB
Package Number E20A

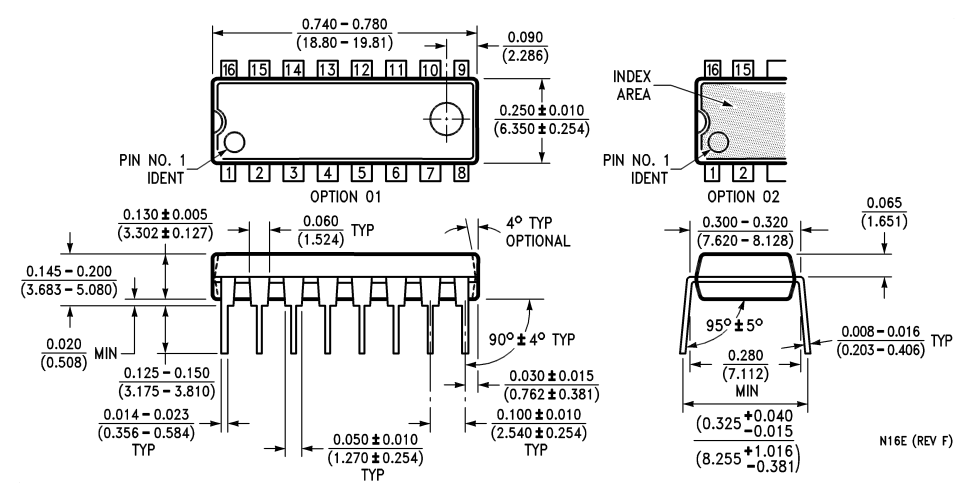


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS174DMQB, 54LS175DMQB, DM54LS174J or DM54LS175J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

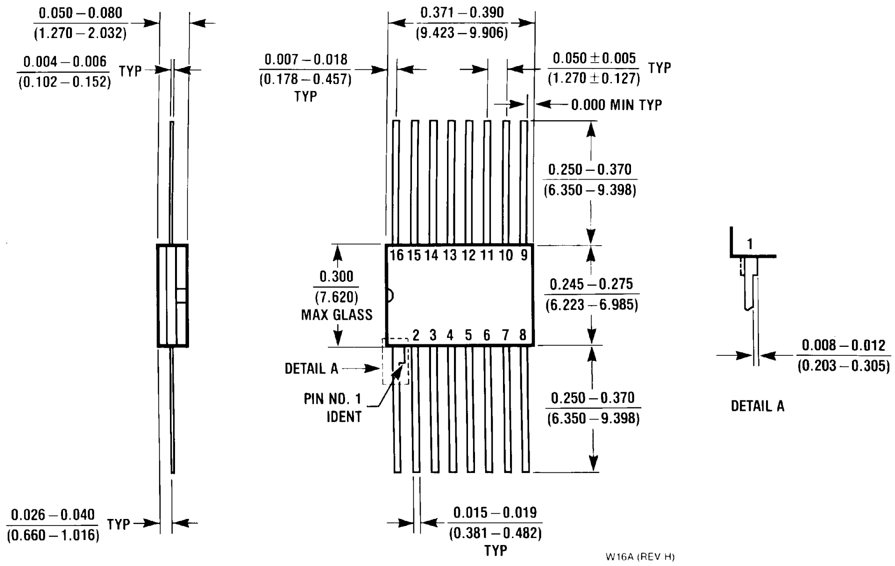


16-Lead Small Outline Molded Package (M)
Order Number DM74LS174M or DM74LS175M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS174N or DM74LS175N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS174FMQB, 54LS175FMQB, DM54LS174W or DM54LS175W
Package Number W16A

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March 1998

DM74LS181
4-Bit Arithmetic Logic Unit

General Description

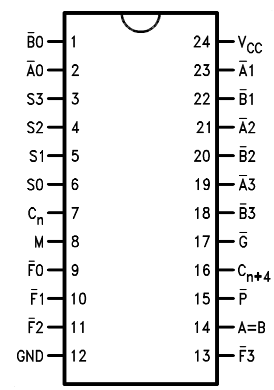
The 'LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations.

Features

- Provides 16 arithmetic operations: add, subtract, compare, double, plus twelve other arithmetic operations
- Provides all 16 logic operations of two variables: exclusive-OR, compare, AND, NAND, OR, NOR, plus ten other logic operations
- Full lookahead for high speed arithmetic operation on long words

Connection Diagram

Dual-In-Line Package



DS009821-1

Order Number DM54LS181J, DM54LS181W or DM74LS181N
See Package Number J24A, N24A or W24C

Pin Names	Description
$\overline{A}0$–$\overline{A}3$	Operand Inputs (Active LOW)
$\overline{B}0$–$\overline{B}3$	Operand Inputs (Active LOW)
S0–S3	Function Select Inputs
M	Mode Control Input
C_n	Carry Input
$\overline{F}0$–$\overline{F}3$	Function Outputs (Active LOW)
A = B	Comparator Output
$\overline{G}$	Carry Generate Output (Active LOW)
$\overline{P}$	Carry Propagate Output (Active LOW)
C_{n+4}	Carry Output

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS181		DM74LS181			Units
		Min	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2		2			V
V_{IL}	Low Level Input Voltage		0.7			0.8	V
I_{OH}	High Level Output Current		−0.4			−0.4	mA
I_{OL}	Low Level Output Current		4			8	mA
T_A	Free Air Operating Temperature	−55	125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (DM54)	M input			0.1	mA
			$\overline{A}_n$, $\overline{B}_n$			0.3	
			S_n			0.4	
			C_n			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	M input			20	µA
			$\overline{A}_n$, $\overline{B}_n$			60	
			S_n			80	
			C_n			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	M input			−0.4	mA
			$\overline{A}_n$, $\overline{B}_n$			−1.2	
			S_n			−1.6	
			C_n			−2.0	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, $\overline{B}_n$, C_n = GND S_n, M, $\overline{A}_n$ = 4.5V	DM54			35	mA
			DM74			37	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics:

for test waveforms and output load. V_{CC} = 5V, T_A = 25˚C

Symbol	Parameter	Conditions	DM54/DM74LS C_L = 15 pF		Units
			Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}	M = GND		27 20	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	M = GND		26 20	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Sum)	M, S_1, S_2 = GND; S_1, S_3 = 4.5V		29 23	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 26	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		30 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$ (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		30 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$(Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		32 25	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$(Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		32 33	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$ (Logic)	M = 4.5V		33 29	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Sum)	M, S_1, S_2 = GND; S_0, S_3 = 4.5V		38 38	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4} (Diff)	M, S_0, S_3 = GND; S_1, S_2 = 4.5V		41 41	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	M, S_0, S_3 = GND; S_1, S_2 = 4.5V; R_L = 2 kΩ to 5.0V		50 62	ns

Sum Mode Test Table 1 Function Inputs

S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}

Sum Mode Test Table 1 Function Inputs (Continued)

S0 = S3 = 4.5V, S1 = S2 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

Diff Mode Test Table 2 Function Inputs

S1 = S2 = 4.5V, S0 = S3 = M = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}$	None	$\overline{B}$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}$	None	$\overline{A}$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	C_{n+4}

Logic Mode Test Table 3 Function Inputs

S1 = S2 = M = 4.5V, S0 = S3 = 0V

Symbol	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	$\overline{A}$	$\overline{B}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$
t_{PLH} t_{PHL}	$\overline{B}$	$\overline{A}$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	Any $\overline{F}$

Functional Description

The 'LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the ADD mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the SUBTRACT mode, $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of four 'LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate $A > B$ and $A < B$.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

Function Table

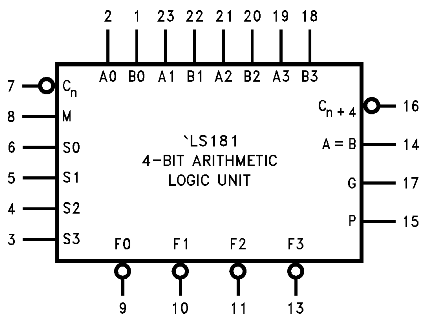
Mode Select Inputs				Active LOW Operands & F_n Outputs		Active HIGH Operands & F_n Outputs	
				Logic	Arithmetic (Note 5)	Logic	Arithmetic (Note 5)
S3	S2	S1	S0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A + B}$	A + B
L	L	H	L	$\overline{A + B}$	$A\overline{B}$ minus 1	$\overline{A}$ B	A + $\overline{B}$
L	L	H	H	Logic 1	minus 1	Logic 0	minus 1
L	H	L	L	$\overline{A + B}$	A plus (A + $\overline{B}$)	$\overline{AB}$	A plus $A\overline{B}$
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)	$\overline{B}$	(A + B) plus $A\overline{B}$
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}$ B	A plus (A + B)	$\overline{A}$ + B	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	$A\overline{B}$ plus (A + B)	B	(A + $\overline{B}$) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logic 0	A plus A (Note 4)	Logic 1	A plus A (Note 4)
H	H	L	H	$A\overline{B}$	AB plus A	A + $\overline{B}$	(A + B) plus A
H	H	H	L	AB	$A\overline{B}$ minus A	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A	A	A minus 1

Note 4: Each bit is shifted to the next most significant position.

Note 5: Arithmetic operations expressed in 2s complement notation.

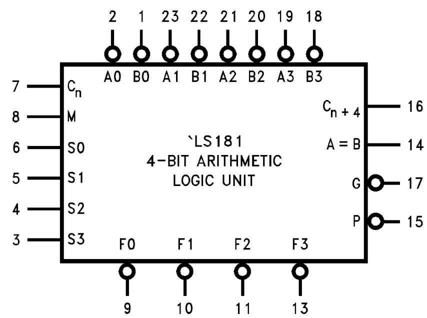
Logic Symbols

Active High Operands



DS009821-3

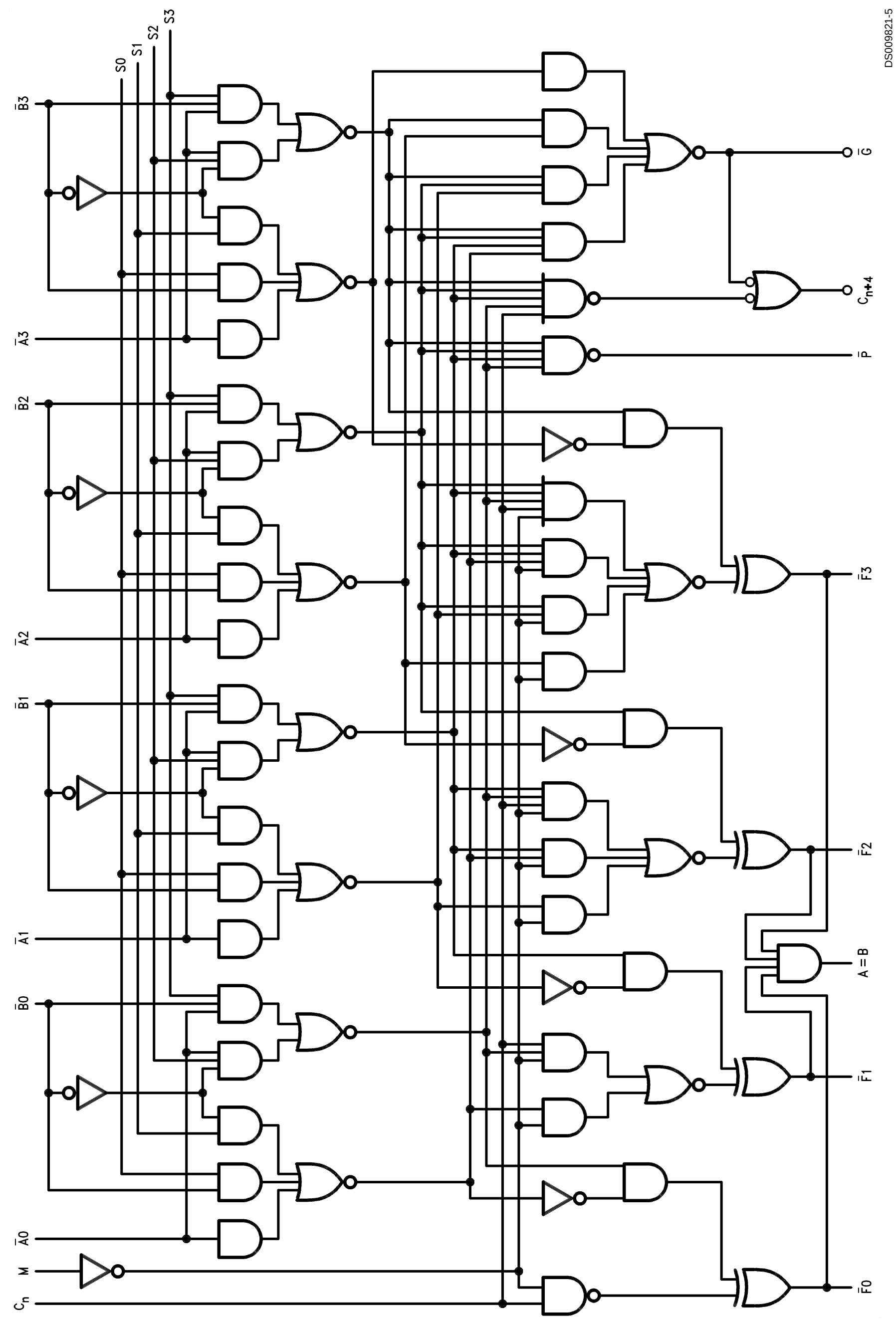
Active Low Operands



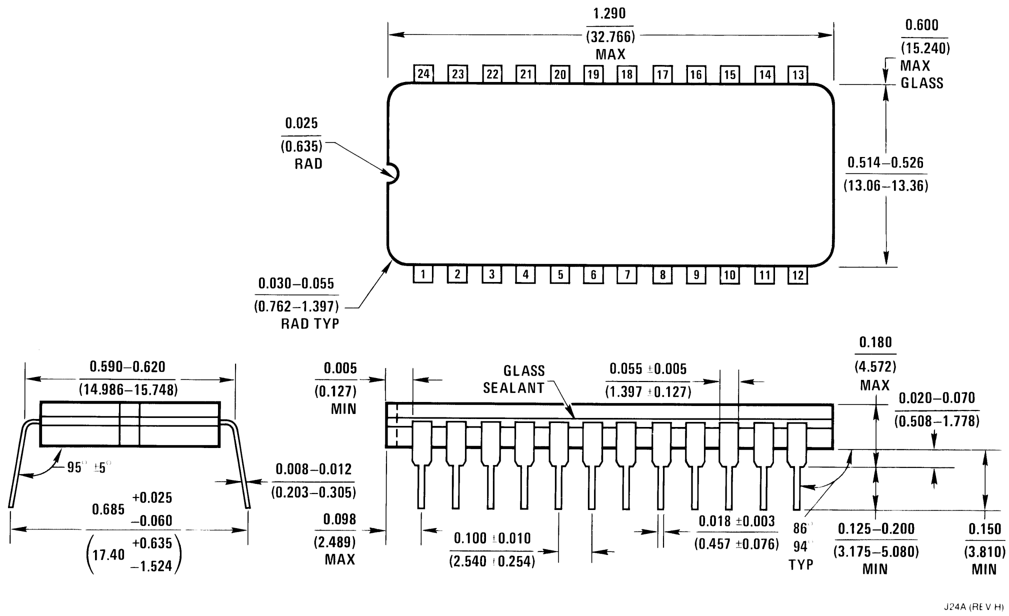
DS009821-4

V_{CC} = Pin 24
GND = Pin 12

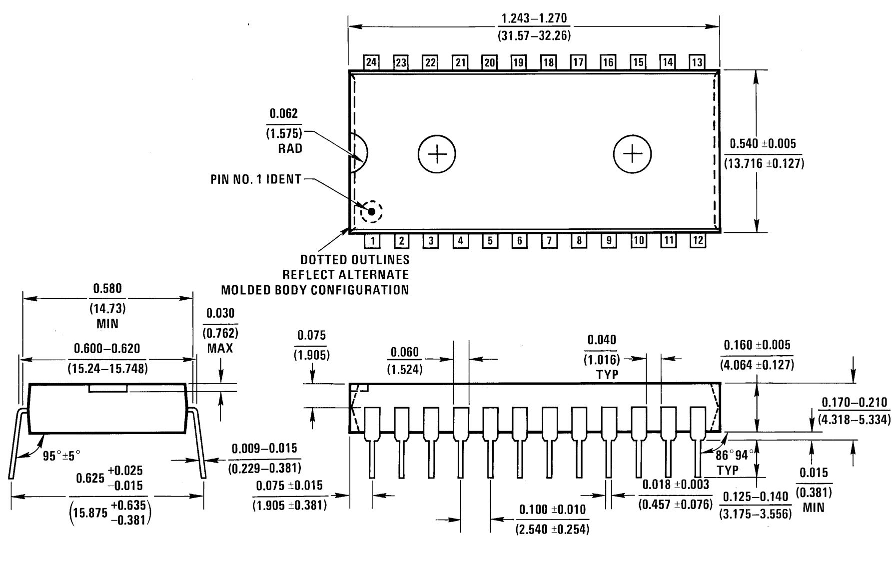
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

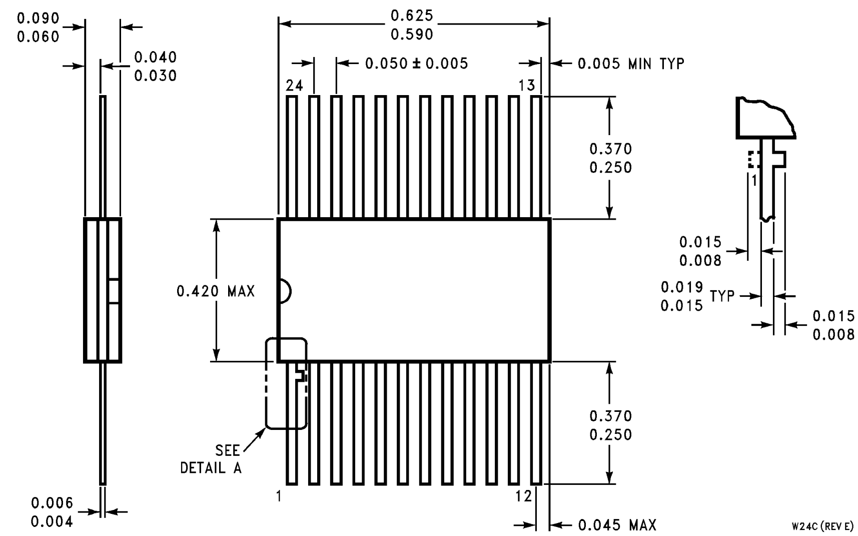


Package (J)
Order Number DM54LS181J
Package Number J24A



24-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS181N
Package Number N24A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Package (W)
Order Number DM54LS181W
Package Number W24C

LIFE SUPPORT POLICY

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May 1989

DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

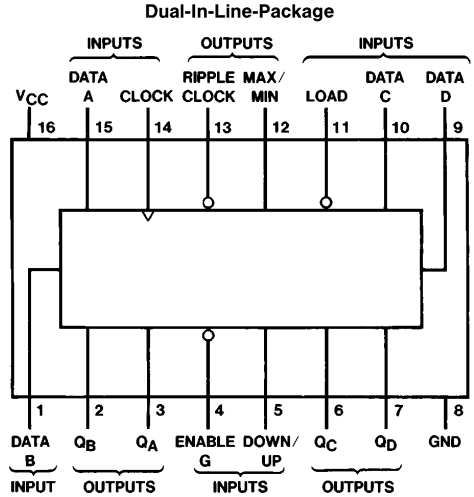
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Connection Diagram

Dual-In-Line-Package



TL/F/6405-1

Order Number DM54LS190J, DM54LS191J, DM54LS190W, DM54LS191W, DM74LS190M, DM74LS191M, DM74LS190N, or DM74LS191N
See NS Package Number
J16A, M16A, N16A or W16A

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS190, LS191			DM74LS190, LS191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock	25			25			ns
		Load	35			35			ns
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{EN}	Enable Time to Clock (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS190 and 'LS191 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Enable			0.3	mA
			Others			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Enable			60	μA
			Others			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable			−1.08	mA
			Others			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			20	35	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

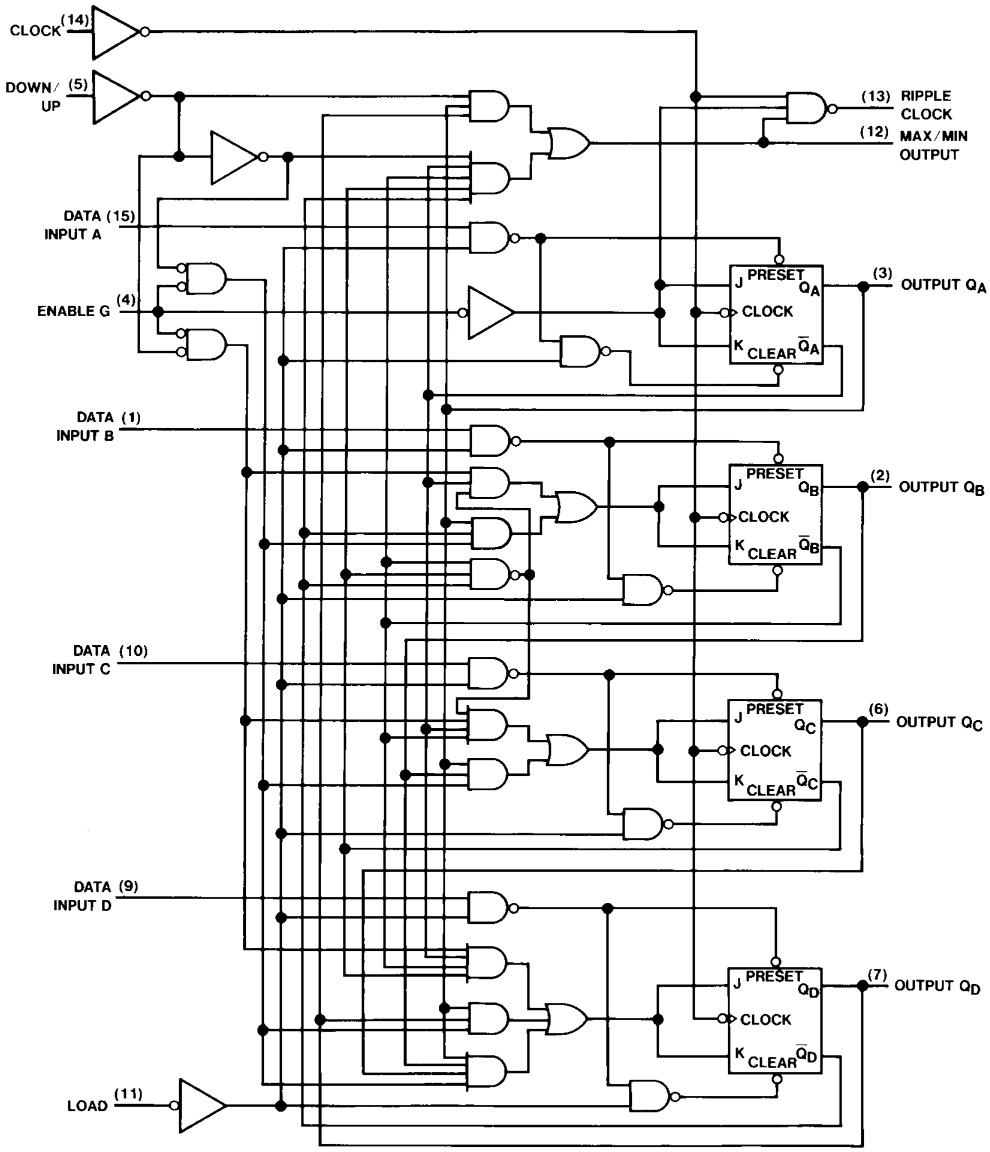
’LS190 and ’LS191 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		20		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33		43	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		50		59	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		50		62	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Clock		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Clock		24		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52		65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Clock		45		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Clock		45		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Ripple Clock		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Ripple Clock		33		42	ns

Logic Diagrams

LS190 Decade Counters

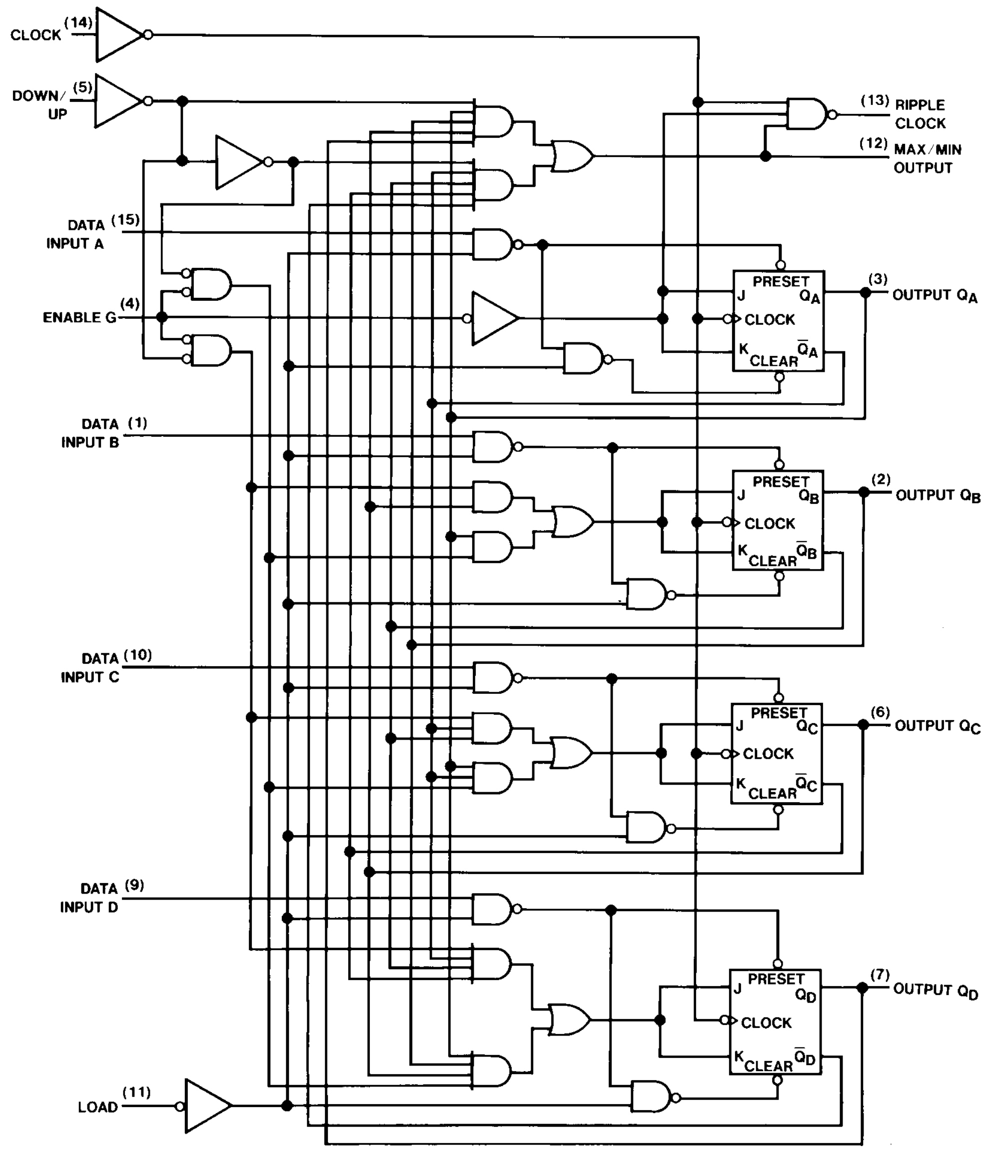


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6405-2

Logic Diagrams (Continued)

LS191 Binary Counters

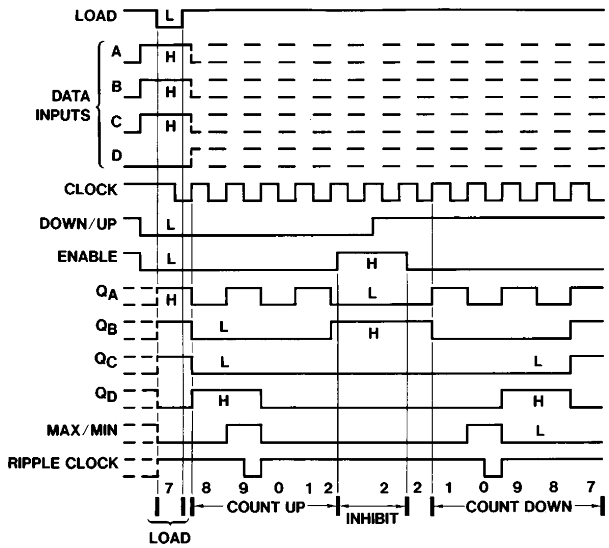


TL/F/6405–3

Pin (16) = V_{CC}, Pin (8) = GND

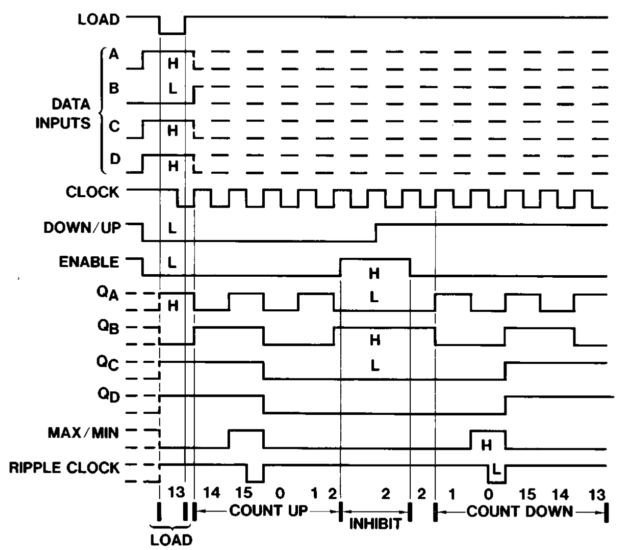
Timing Diagrams

LS190 Decade Counters
Typical Load, Count, and Inhibit Sequences



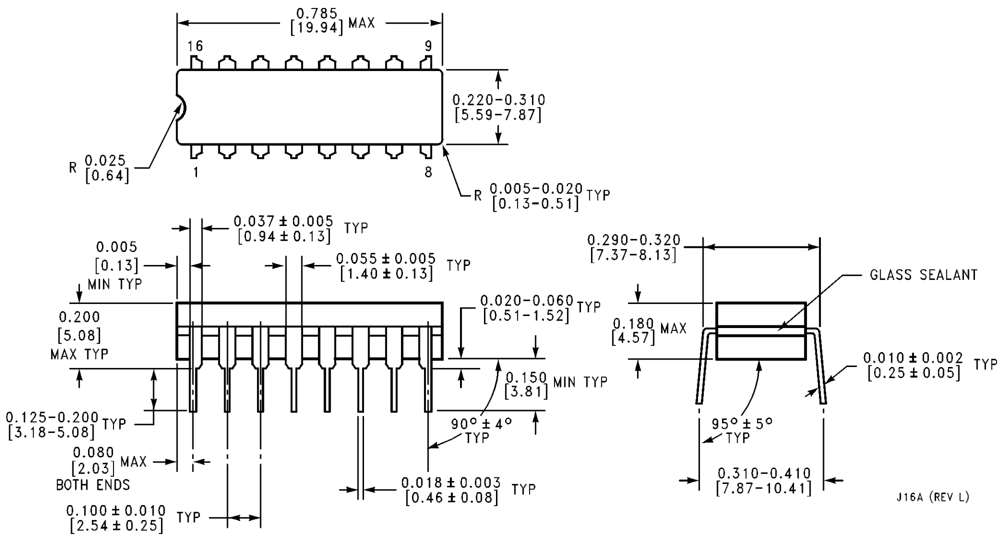
TL/F/6405–4

LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences

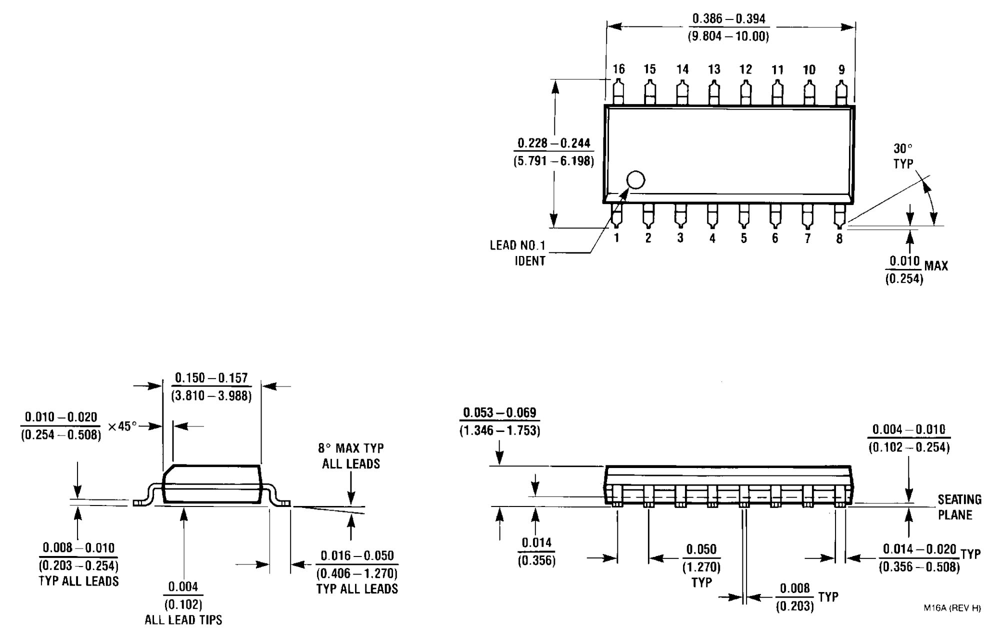


TL/F/6405–5

Physical Dimensions inches (millimeters)

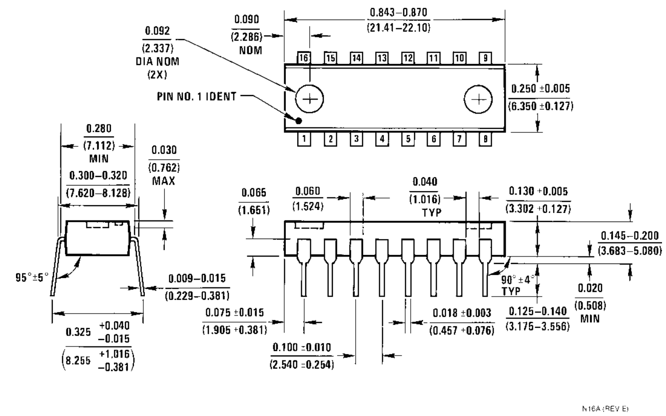


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS190J, DM54LS191J
NS Package Number J16A

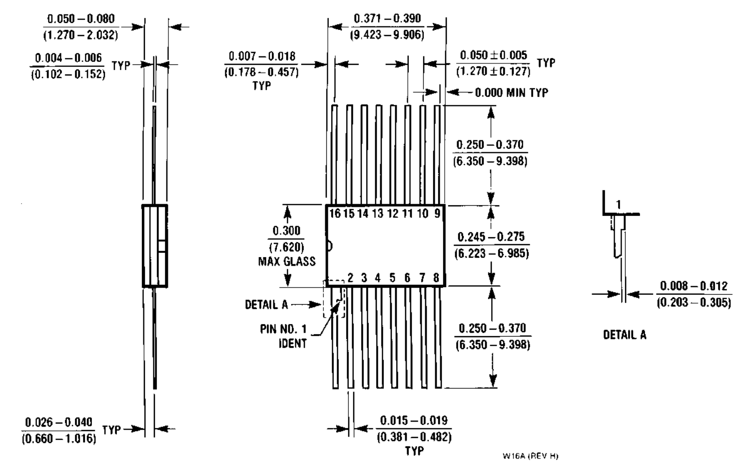


16-Lead Small Outline Molded Package (M)
Order Number DM74LS190M, DM74LS191M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS190N, DM74LS191N
NS Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS190W or DM54LS191W
NS Package Number W16A

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National Semiconductor

May 1992

54LS192/DM74LS192 Up/Down Decade Counter with Separate Up/Down Clocks

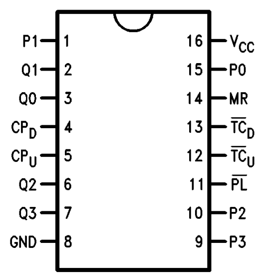
General Description

The 'LS192 is an up/down BCD decade (8421) counter. Separate Count Up and Count Down Clocks are used and in either counting mode the circuits operate synchronously. The outputs change state synchronous with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided which are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuits to be used as programmable counters. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

Connection Diagram

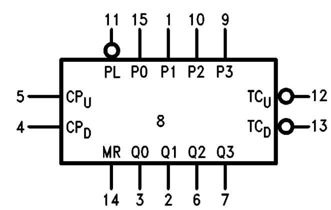
Dual-In-Line Package



TL/F/10178–1

Order Number 54LS192DMQB, 54LS192FMQB, 54LS192LMQB, DM74LS192M or DM74LS192N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



TL/F/10178–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
CP_U	Count Up Clock Input (Active Rising Edge)
CP_D	Count Down Clock Input (Active Rising Edge)
MR	Asynchronous Master Reset Input (Active HIGH)
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
P0–P3	Parallel Data Inputs
Q0–Q3	Flip-Flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output (Active LOW)
$\overline{TC}_U$	Terminal Count Up (Carry) Output (Active LOW)

Mode Select Table

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	↑	H	Count Up
L	H	H	↑	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS192			DM74LS192			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{PL}$	20 20			20 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{PL}$	3 3			3 3			ns
t_w (L)	CP Pulse Width LOW	17			17			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	20			20			ns
t_w (H)	MR Pulse Width HIGH	15			15			ns
t_{rec}	Recovery Time, MR to CP	3			3			ns
t_{rec}	Recovery Time, $\overline{PL}$ to CP	10			10			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	54LS			0.4	V
		V_{IH} = Min	DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V V_I = 7V	DM54 DM74			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, MR, $\overline{PL}$ = GND Other Inputs = 4.5V				31	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characterisitcs

V_{CC} = +0.5V, T_A = +25°C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2k, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Count Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP_U or CP_D to Q_n		31 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP_U to $\overline{TC}_U$		16 21	ns
t_{PLH} t_{PHL}	Propagation Delay CP_D to $\overline{TC}_D$		16 24	
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		20 30	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		32 30	ns
t_{PHL}	Propagation Delay, MR to Q_n		25	

Functional Description

The '192 is an asynchronously presettable decade and 4-bit binary synchronous up/down (reversible) counter. The operating modes of the '192 decade counter and the '193 binary counter are identical, with the only difference being the count sequences as noted in the State Diagram. Each circuit contains four master/slave flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up, and count down operations.

Each flip-flop contains JK feedback from slave to master such that a LOW-to-HIGH transition on its T input causes the slave, and thus the Q output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW.

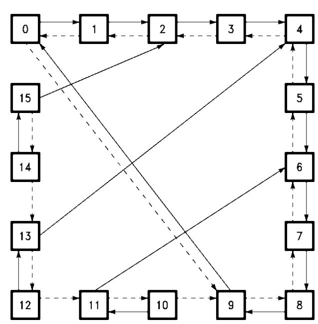
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When a circuit has reached the maximum count state (9 for the '192, 15 for the '193), the next HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q0 \bullet Q3 \bullet \overline{CP}_U$$

$$\overline{TC}_D = \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2} \bullet \overline{Q3} \bullet \overline{CP}_D$$

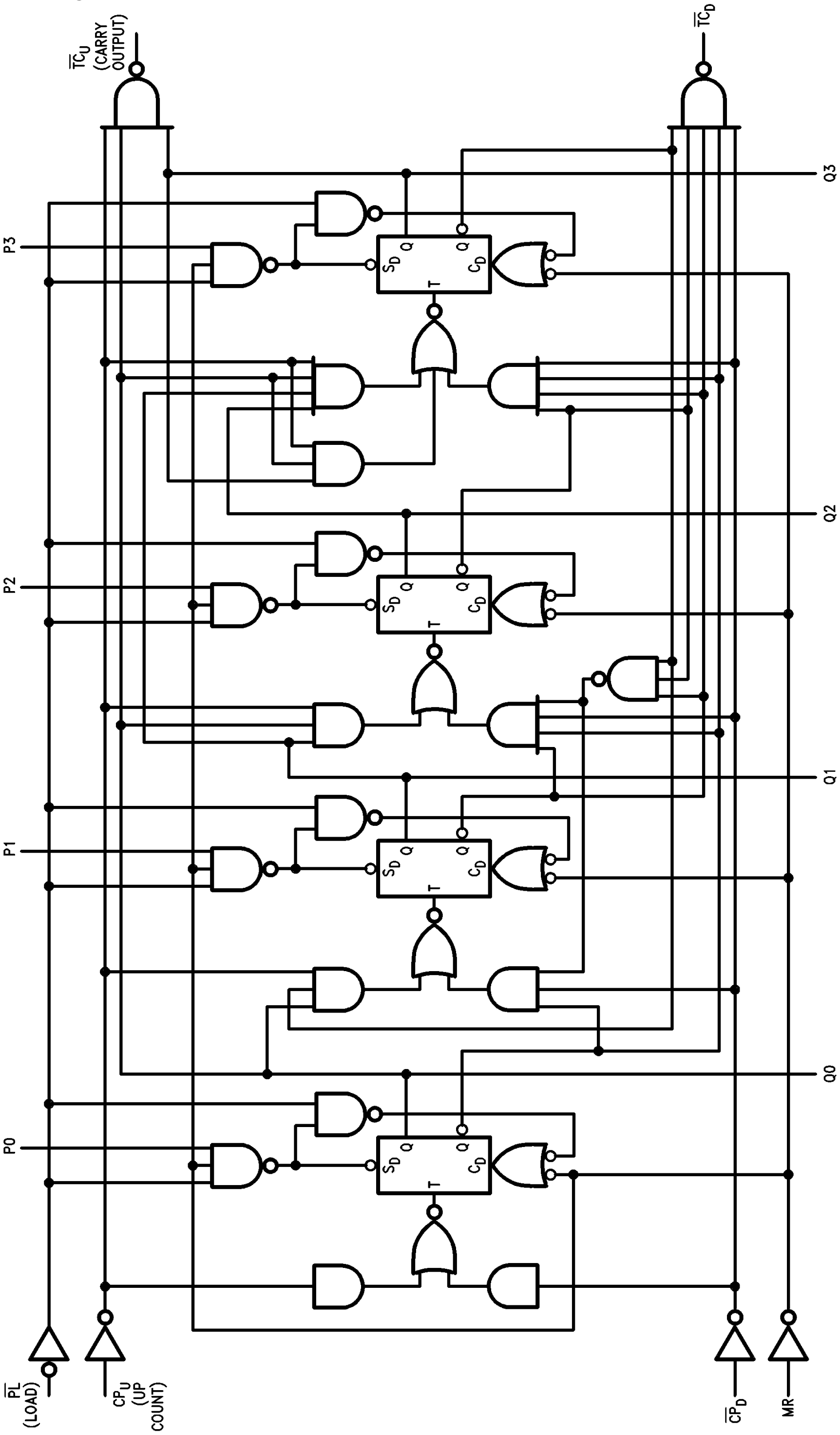
Each circuit has an asynchronous parallel load capability permitting the counter to be reset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data inputs (P0–P3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both Clock inputs, and latch each Q output in the LOW state. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that Clock will be interpreted as a legitimate signal and will be counted.

State Diagram



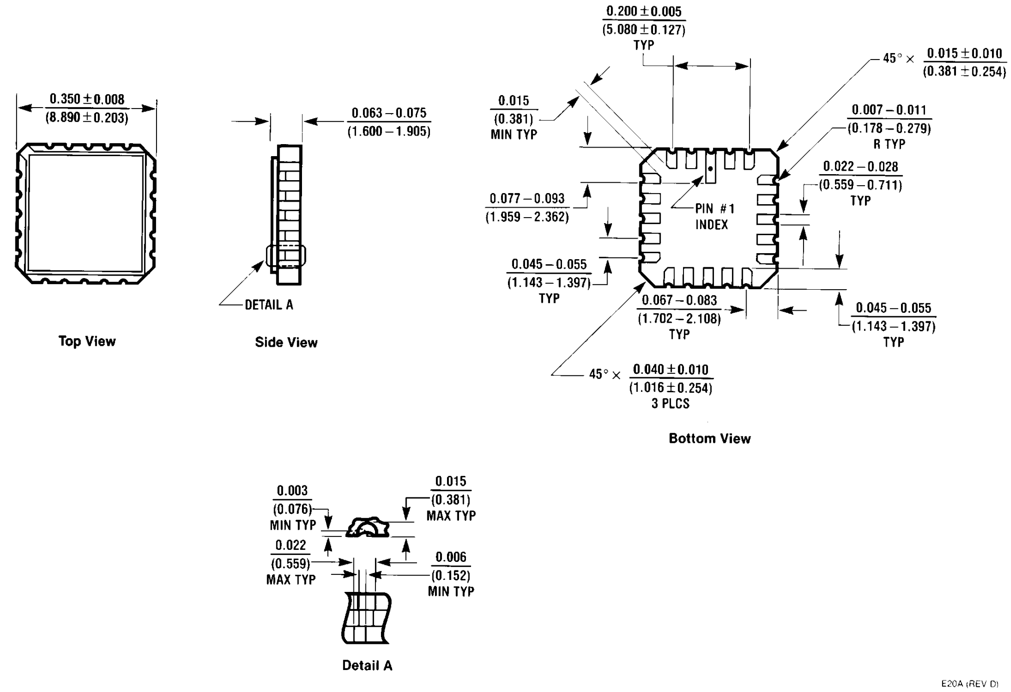
TL/F/10178–4

Logic Diagram

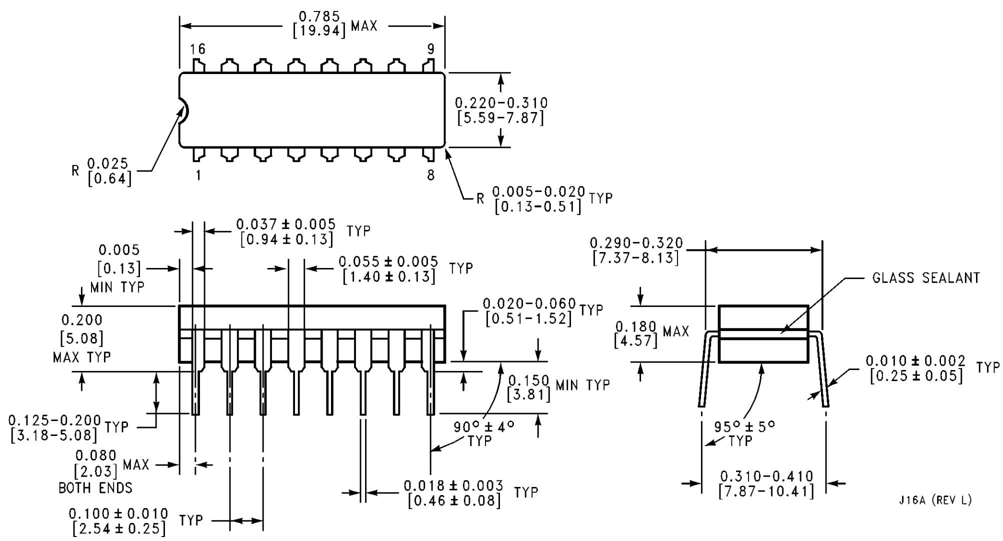


TL/F/10178–3

Physical Dimensions inches (millimeters)

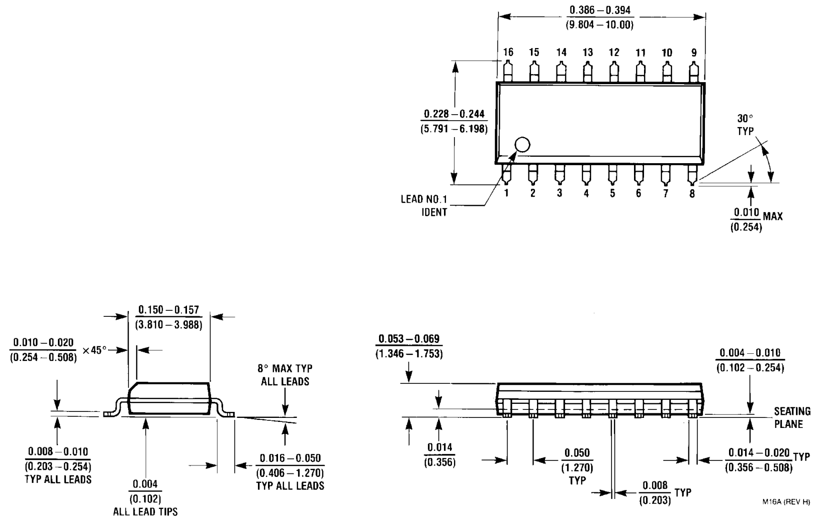


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS192LMQB
NS Package Number E20A

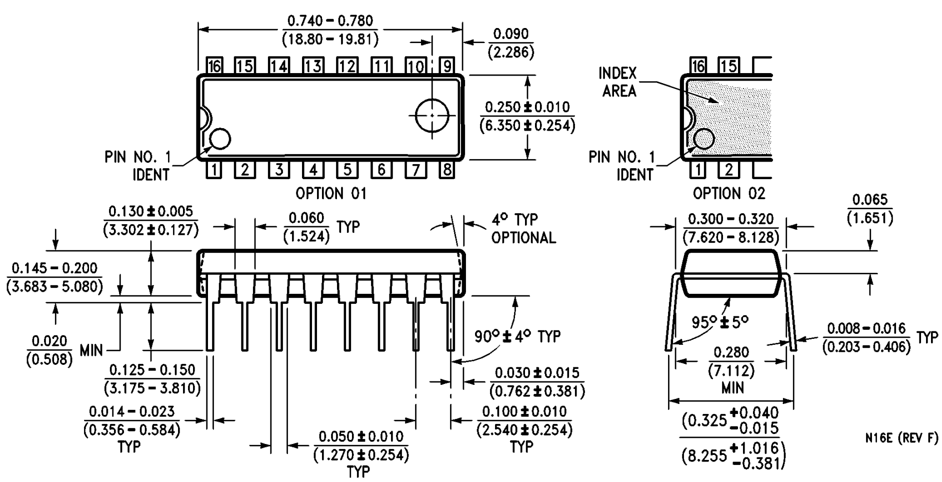


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS192DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

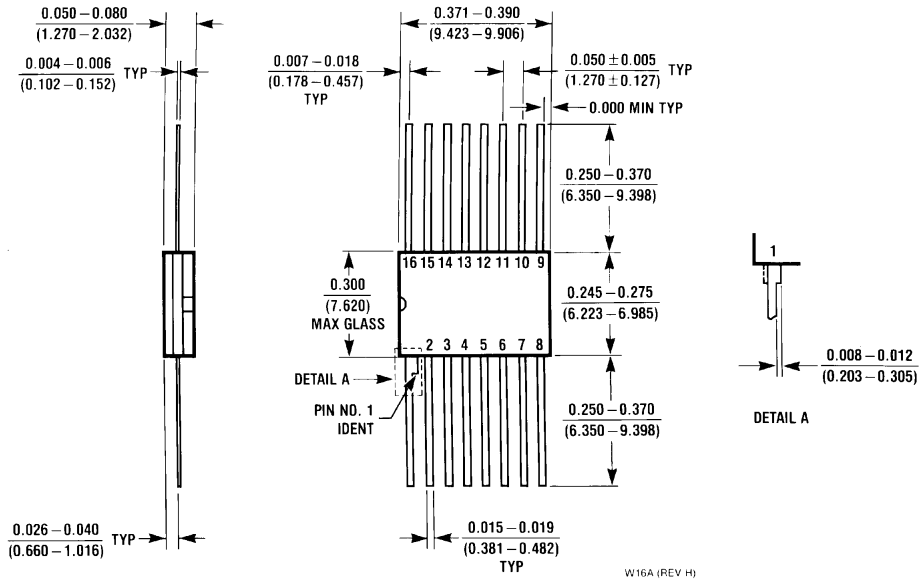


16-Lead Small Outline Molded Package (M)
Order Number DM74LS192M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS192N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS192FMQB
NS Package Number W16A

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September 1986
Revised February 1999

DM74LS193
Synchronous 4-Bit Binary Counters with Dual Clock

General Description

The DM74LS193 circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a LOW-to-HIGH level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held HIGH.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is LOW. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

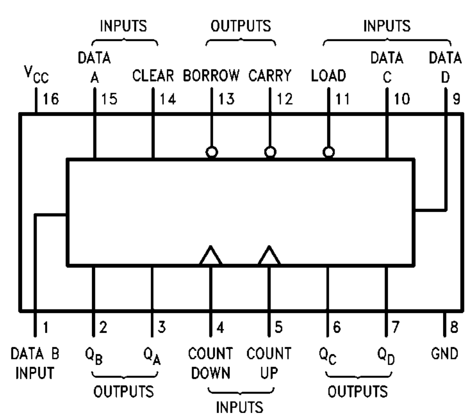
Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

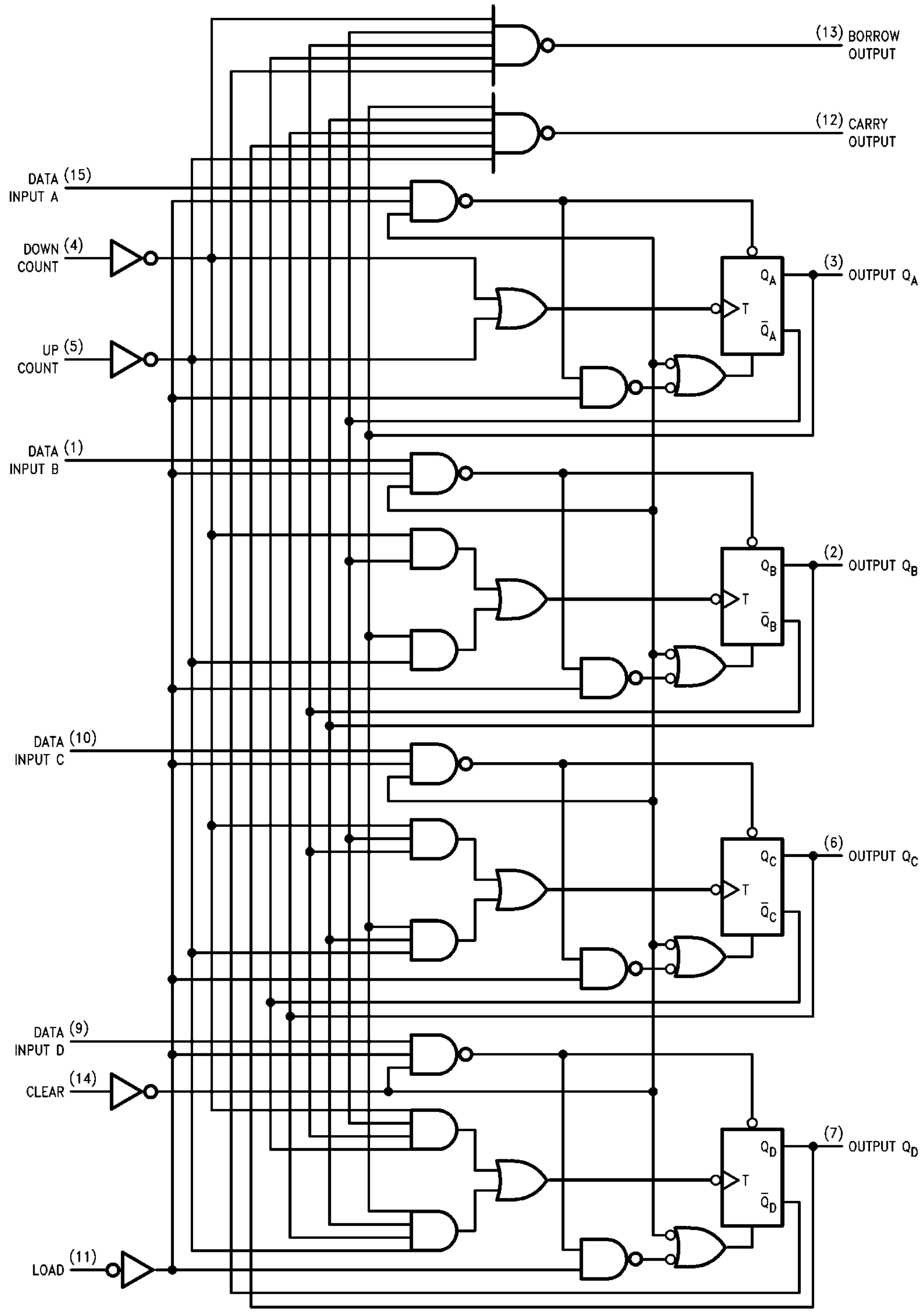
Ordering Code:

Order Number	Package Number	Package Description
DM74LS193N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
DM74LS193M	M16A	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-012, 0.150” Narrow Body

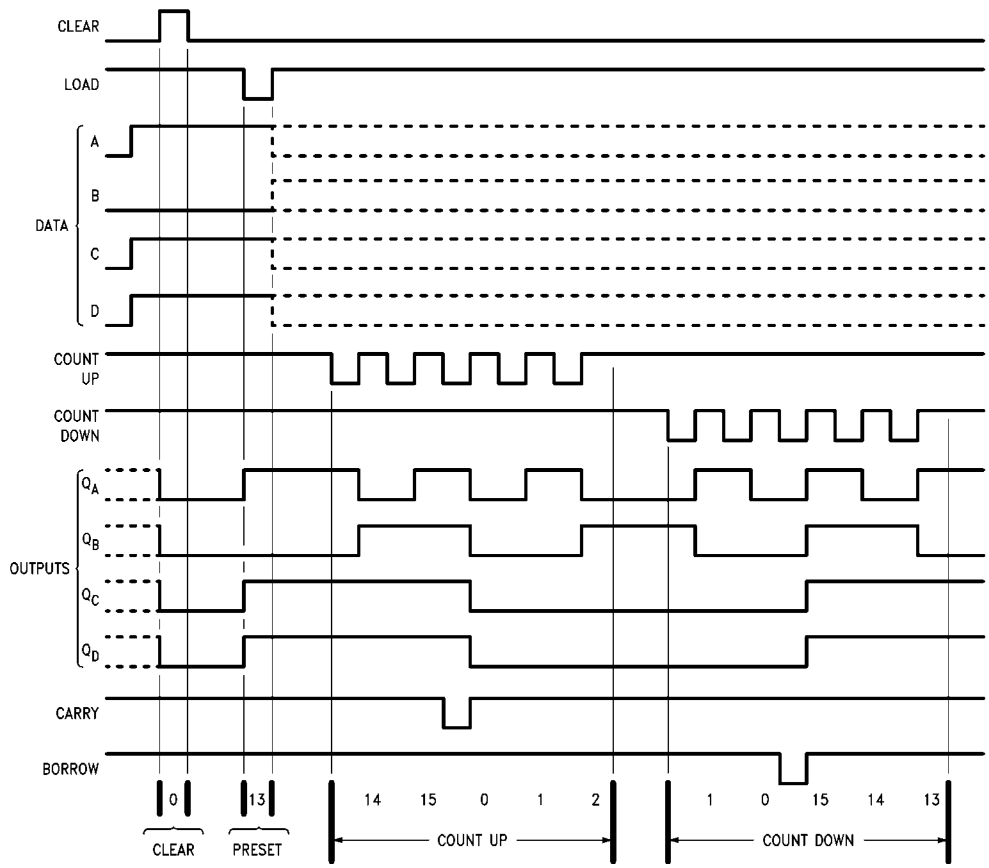
Connection Diagram



Logic Diagram



Timing Diagram



Note A: Clear overrides load, data, and count inputs

Note B: When counting up, count-down input must be HIGH; when counting down, count-up input must be HIGH.

Absolute Maximum Ratings(Note 1)

Operating Free Air Temperature Range	–0°C to +70°C
Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	–65°C to +125°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the abbsolute maximum ratings. The "Reccommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			–0.4	mA
I_{OL}	LOW Level Output Current			8	mA
f_{CLK}	Clock Frequency (Note 2)	0		25	MHz
	Clock Frequency (Note 3)				
t_W	Pulse Width of any Input (Note 4)	20			ns
t_{SU}	Data Setup Time (Note 4)	20			ns
t_H	Data Hold Time (Note 4)	0			ns
t_{EN}	Enable Time to Clock (Note 4)	40			ns
T_A	Free Air Operating Temperature	0		70	°C

Note 2: C_L = 15 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = –18 mA			–1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	2.7	3.4		
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			–0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	–20		–100	mA
		(Note 6)	–20		–100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)		19	34	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

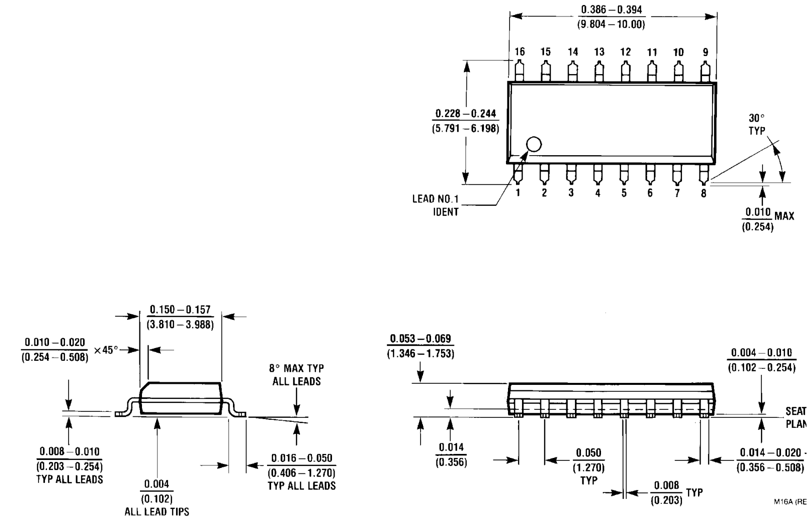
Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

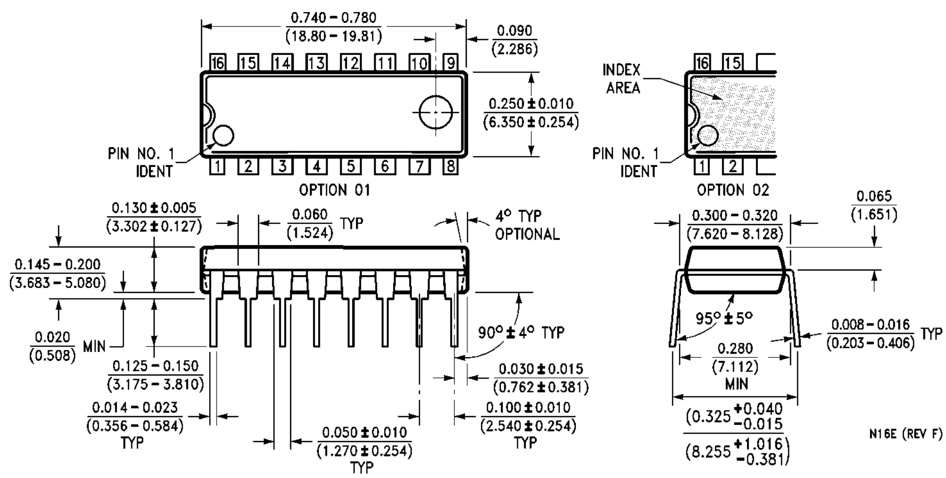
AC Electrical Characteristics

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$, $C_L = 15$ pF Min	$C_L = 15$ pF Max	$C_L = 50$ pF Min	$C_L = 50$ pF Max	Units
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Count Up to Carry		26		30	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Count Up to Carry		24		36	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Count Down to Borrow		24		29	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Count Down to Borrow		24		32	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Either Count to Any Q		38		45	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Either Count to Any Q		47		54	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Load to Any Q		40		41	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Load to Any Q		40		47	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Any Q		35		44	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit(SOIC), JEDEC MS-012, 0150” Narrow Body
Package Number M16A



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300” Wide
Package Number N16E

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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April 1998

DM74LS194A
4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load

Shift right (in the direction Q_A toward Q_D)

Shift left (in the direction Q_D toward Q_A)

Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

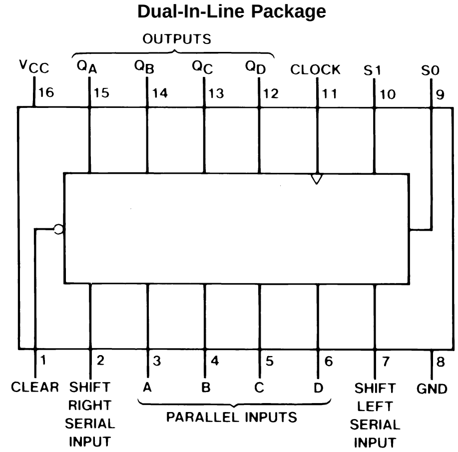
Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

Connection Diagram

Dual-In-Line Package



DS006407-1

Order Number 54LS194ADMQB, 54LS194AFMQB, 54LS194ALMQB, DM74LS194AM or DM74LS194AN
See Package Number E20A, J16A, M16A, N16E or W16A

 DS006407

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		54LS194A			DM74LS194A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		30		0	0		25	MHz
	Clock Frequency (Note 3)		22			0		20	
t_W	Pulse Width (Note 4)	Clock	17			20			ns
		Clear	12			20			
t_{SU}	Setup Time (Note 4)	Mode	25			30			ns
		Data	16			20			
t_H	Hold Time (Note 4)		0			0			ns
t_{REL}	Clear Release Time (Note 4)		18			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: C_L = 15 pF, T_A = 25˚C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25˚C and V_{CC} = 5V.

Note 4: T_A = 25˚C and V_{CC} = 5V.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	54LS	2.5			V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	54LS			0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min				0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			15	23	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

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Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C (See for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS C_L = 50 pF R_L = 2 kΩ		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		21		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		24		35	ns
t_{PHL}	Propagation Delay Time High to Low Output	Clear to Any Q		26		38	ns

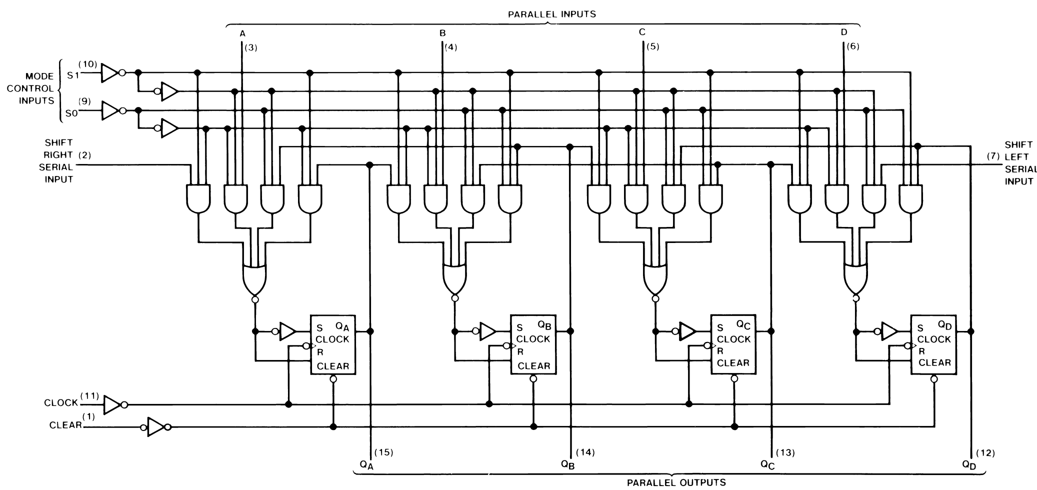
Note 8: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 9: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 10: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Logic Diagram

LS194A



DS006407-2

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Function Table

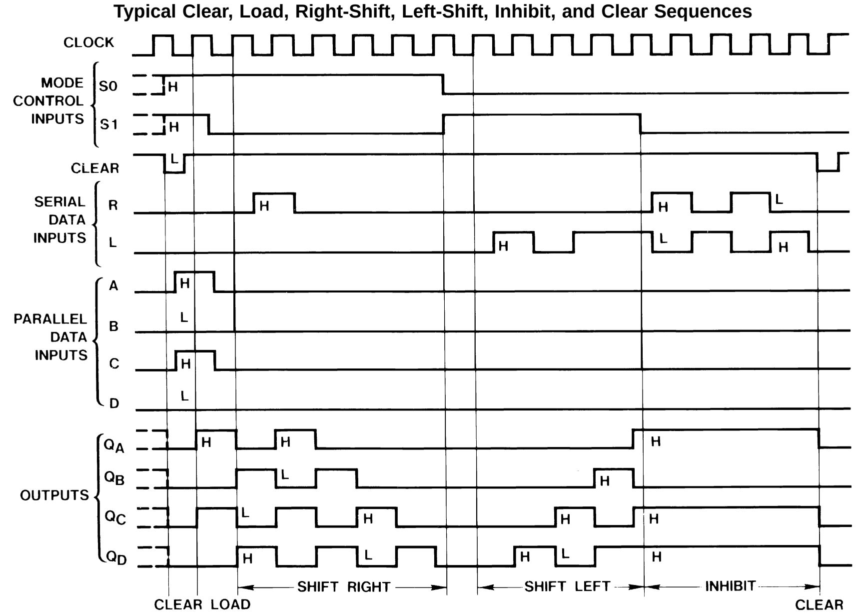
Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)
↑ = Transition from low to high level
a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Timing Diagram

Book
Extract
End

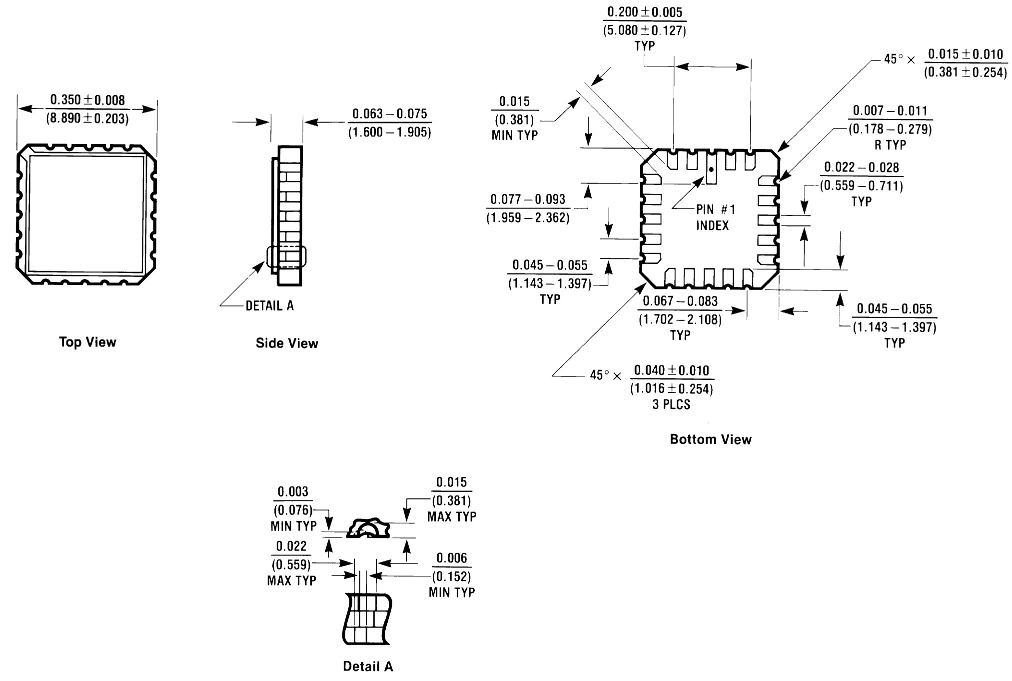
Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



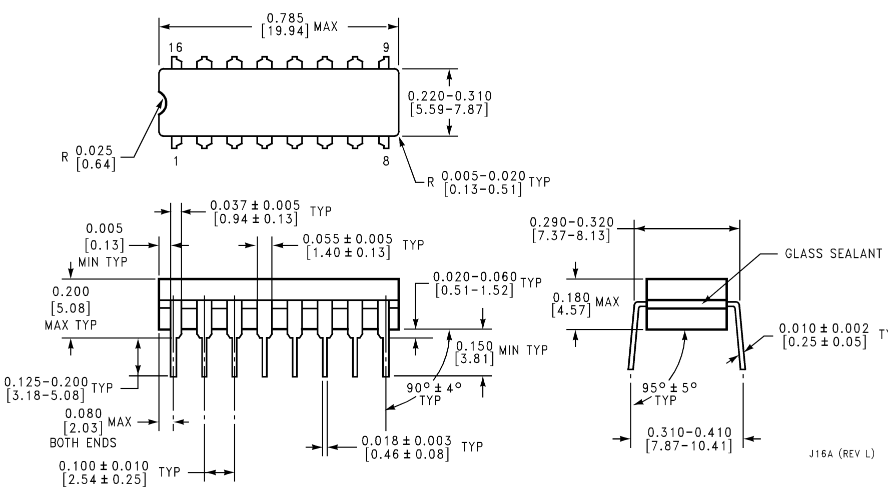
DS006407-3

PrintDate=1998/03/26 PrintTime=10:40:55 37023 ds006407 Rev. No. 3 cmserv **Proof** 4

Physical Dimensions inches (millimeters) unless otherwise noted



Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS194ALMQB
Package Number E20A



16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS194ADMQB
Package Number J16A

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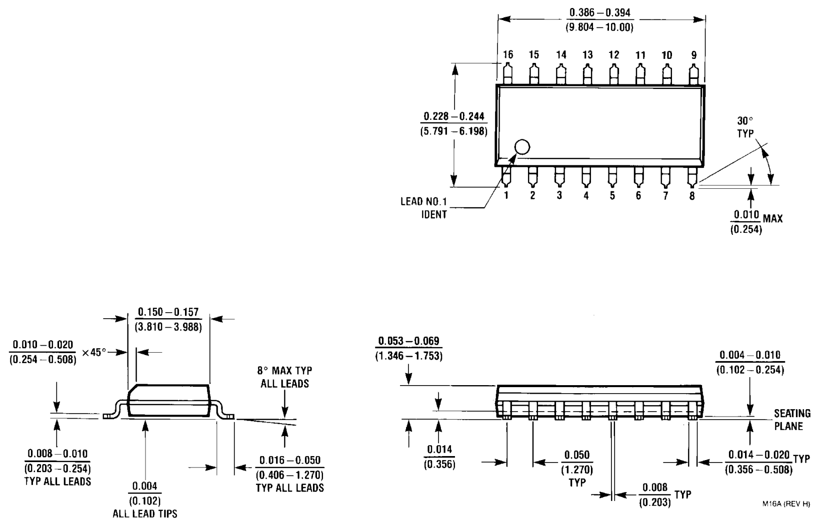
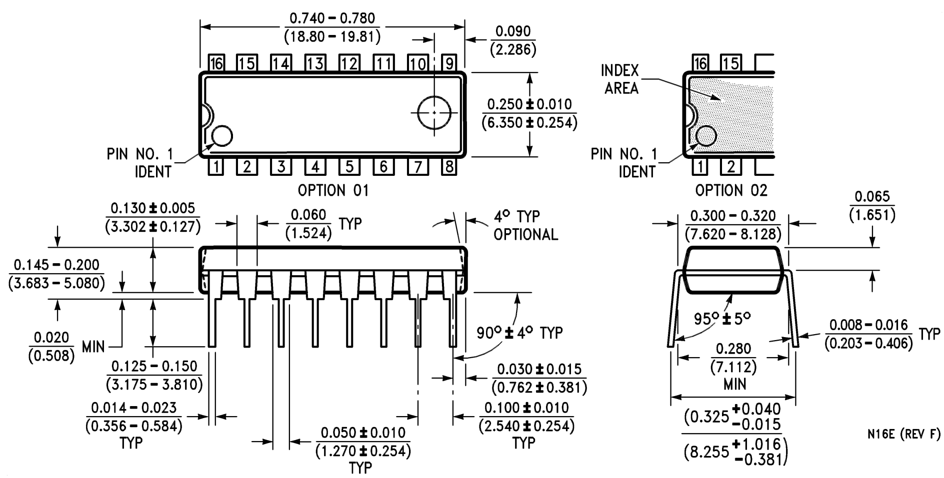
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

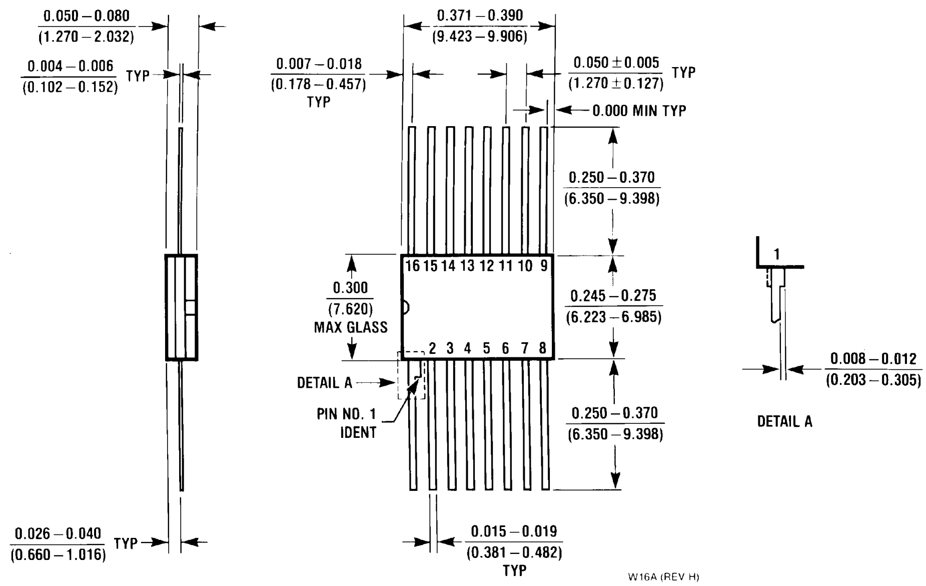


16-Lead Small Outline Molded Package (M)
Order Number DM74LS194AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS194AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS194AFMQB
Package Number W16A

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National Semiconductor

June 1989

54LS195A/DM74LS195A
4-Bit Parallel Access Shift Register

General Description

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

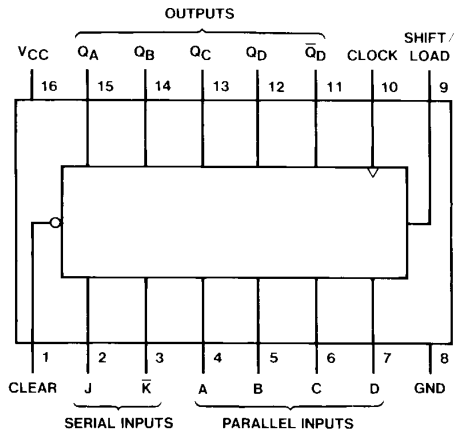
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 70 mW

Connection Diagram

Dual-In-Line Package



TL/F/6408–1

Order Number 54LS195ADMQB, 54LS195AFMQB, 54LS195ALMQB, DM74LS195AM or DM74LS195AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS195A			DM74LS195A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		30		0	0		30	MHz
	Clock Frequency (Note 2)		30		0	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	16			16			ns
		Clear	14			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Shift/Load Release Time (Note 3)		10			10			ns
	Clear Release Time (Note 3)		25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74LS	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74LS		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	54LS	−20		−100	mA
			DM74LS	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 6)			14	21	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			$C_L = 15$ pF		$R_L = 2$ kΩ, $C_L = 50$ pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		21		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		24		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		26		38	ns

Function Table

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

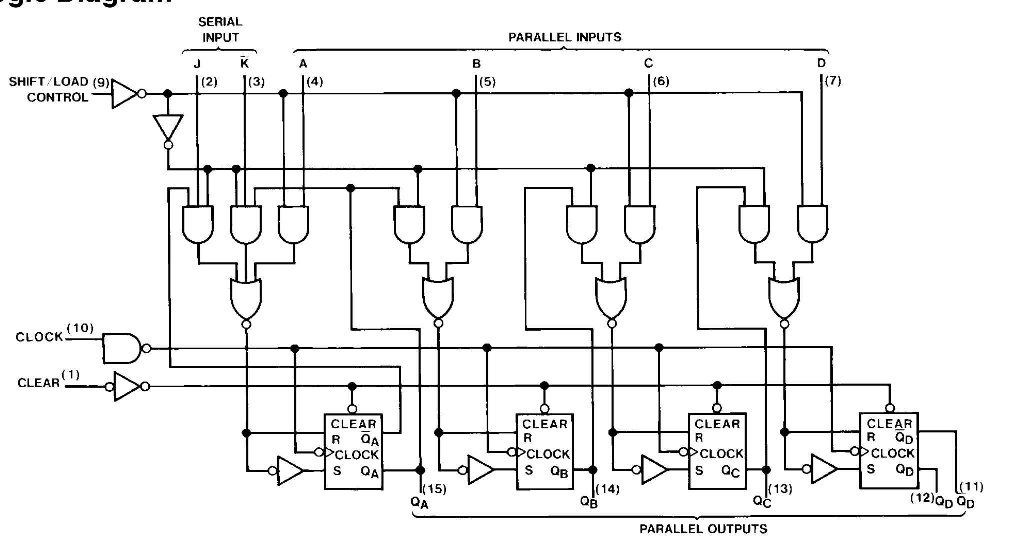
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

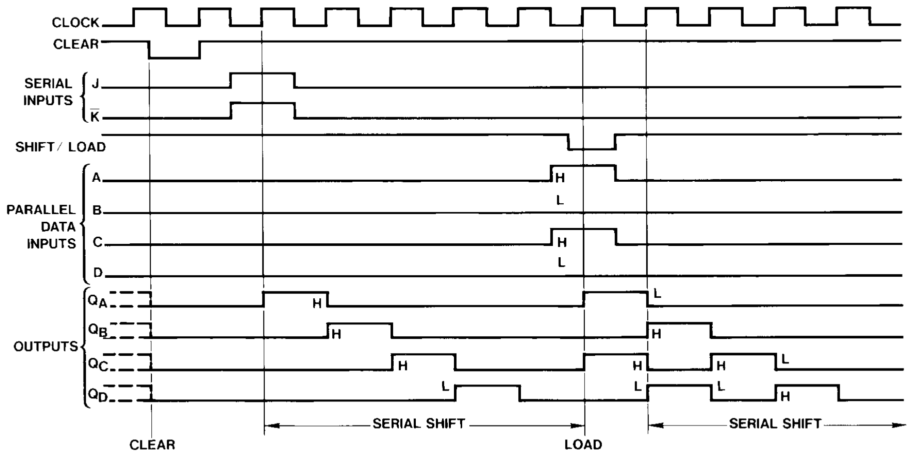
Logic Diagram



TL/F/6408–2

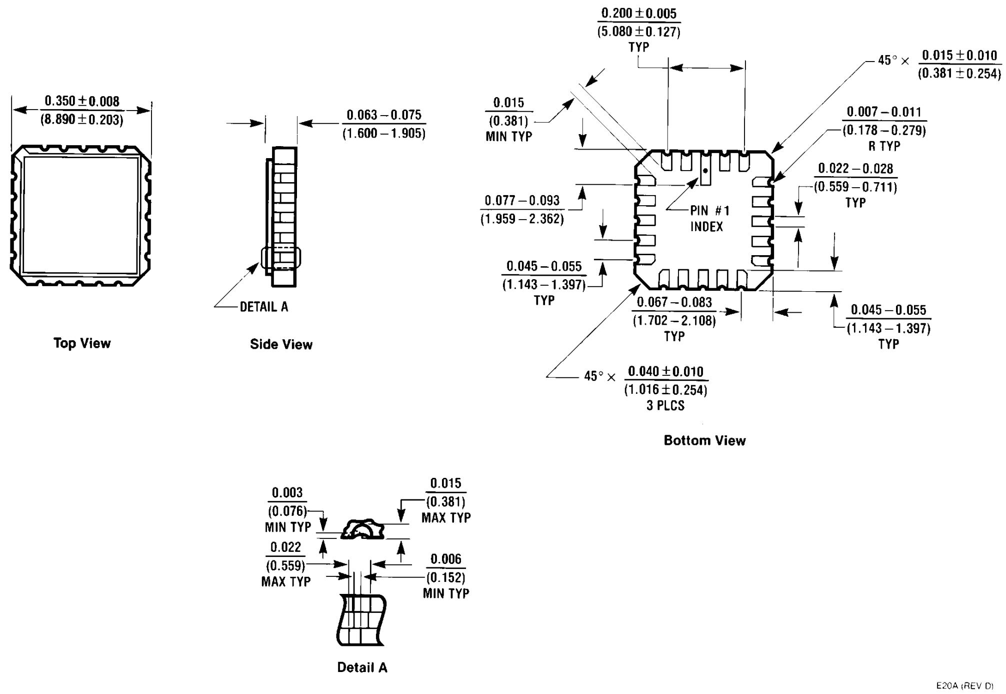
Timing Diagram

Typical Clear, Shift, and Load Sequences

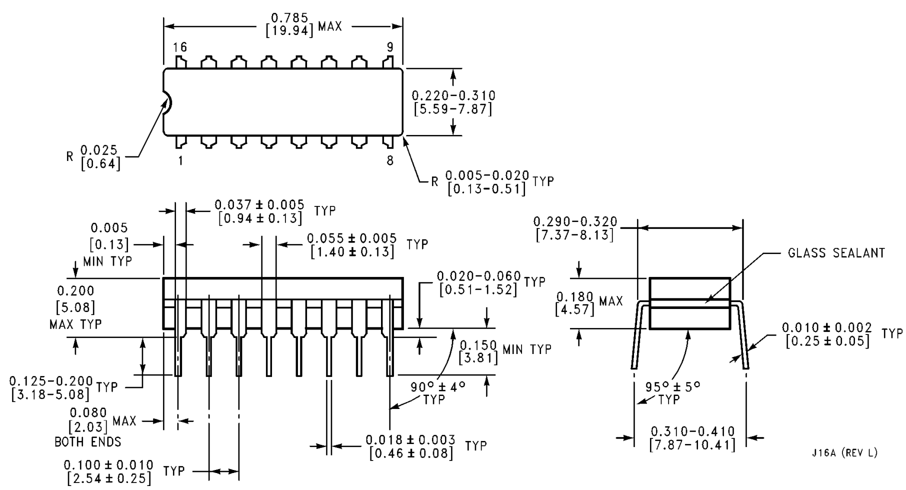


TL/F/6408–3

Physical Dimensions inches (millimeters)

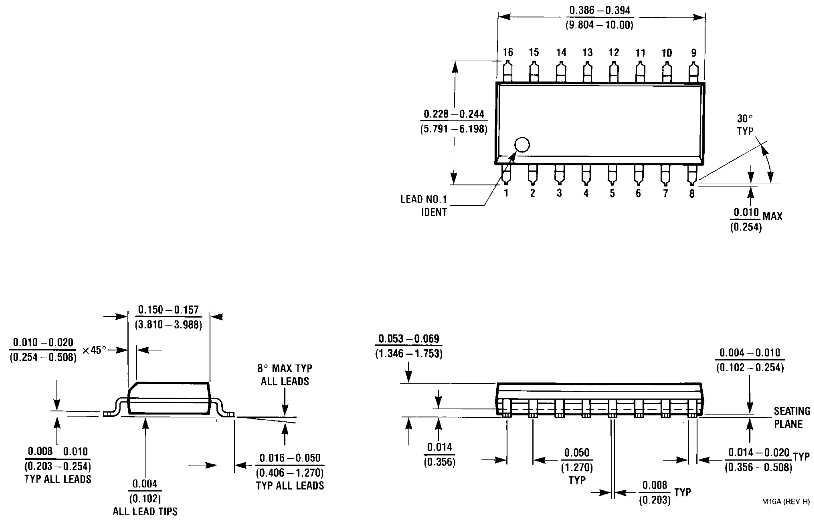


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS195ALMQB
NS Package Number E20A

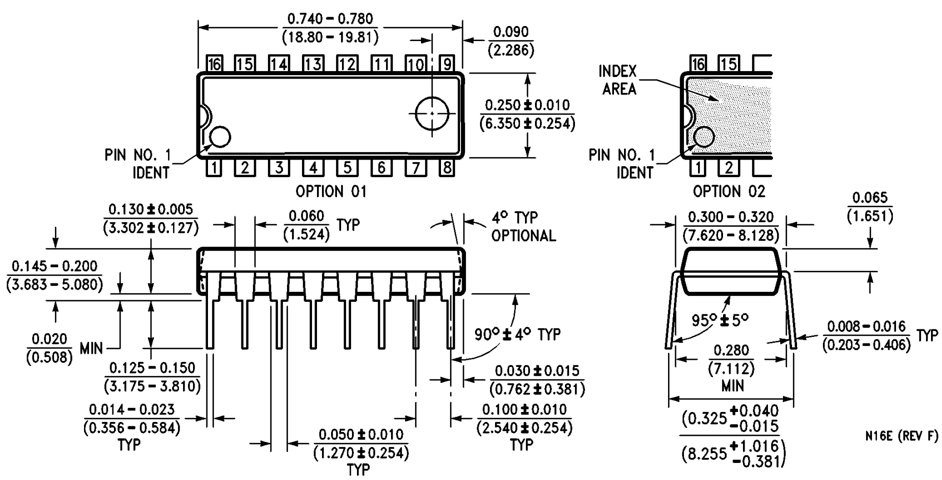


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS195ADMQB
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

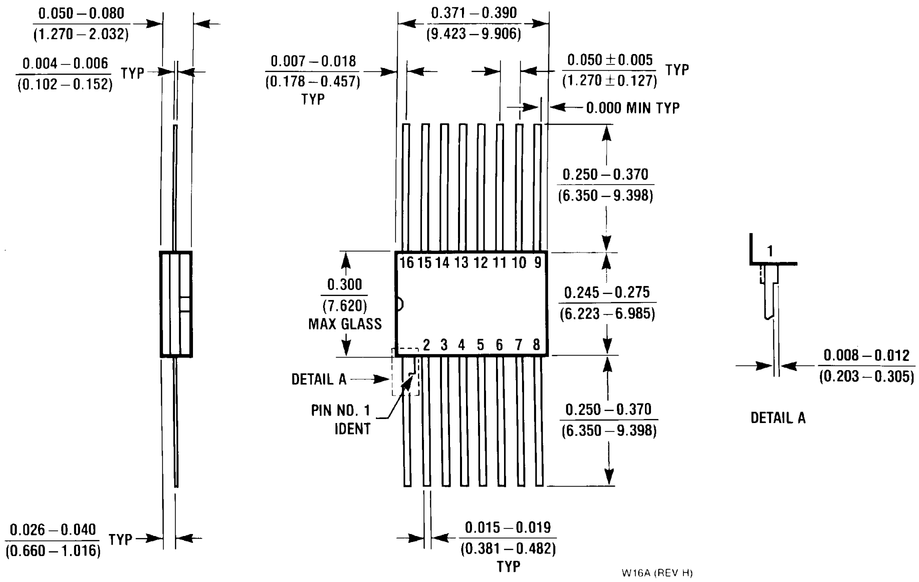


16-Lead Small Outline Molded Package (M)
Order Number DM74LS195AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS195AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS195AFMQB
NS Package Number W16A

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National Semiconductor

January 1992

DM74LS196 Presettable Decade Counter

General Description

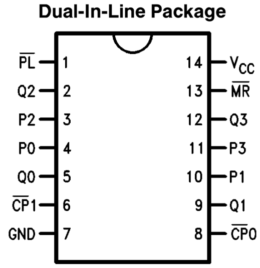
The 'LS196 decade ripple counter is partitioned into divide-by-two and divide-by-five sections which can be combined to count either in BCD (8421) sequence or in a bi-quinary mode producing a 50% duty cycle output. Both circuit types have a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (Pn) into the flip-flops. This preset feature makes the circuits usable as programmable counters. The circuits can also be used as 4-bit latches, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. In the counting modes, state changes are initiated by the falling edge of the clock.

Features

- High counting rates—typically 60 MHz
- Choice of counting modes—BCD, bi-quinary, binary
- Asynchronous preset and master reset

Connection Diagram

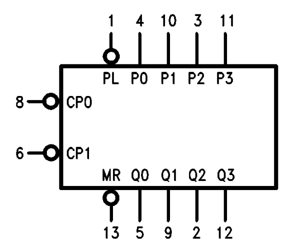
Dual-In-Line Package



TL/F/10179–1

Order Number DM74LS196M or DM74LS196N
See NS Package Number M14A or N14A

Logic Symbol



TL/F/10179–2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
$\overline{CP0}$	÷2 Section Clock Input (Active Falling Edge)
$\overline{CP1}$	÷5 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0–Q3	Flip-Flop Outputs

 TL/F/10179 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS196			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW Pn to $\overline{PL}$	8 12			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW Pn to $\overline{PL}$	0 6			ns
t_w (H)	$\overline{CP}$0 Pulse Width HIGH	12			ns
t_w (H)	$\overline{CP}$1 Pulse Width HIGH	24			ns
t_w (L)	$\overline{PL}$ Pulse Width LOW	18			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	12			ns
t_{rec}	Recovery Time $\overline{PL}$ to $\overline{CP}$n	16			ns
t_{rec}	Recovery Time $\overline{MR}$ to $\overline{CP}$n	18			ns

Electrical Characteristics Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 5.5V, $\overline{CP}$1			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{IN} = GND			20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2k$, $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Count Frequency at $\overline{CP}0$	45		MHz
f_{max}	Maximum Count Frequency at $\overline{CP}1$	22.5		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}0$ to Q0		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q1		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q2		34 34	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}1$ to Q3		15 21	ns
t_{PLH} t_{PHL}	Propagation Delay Pn to Qn		25 35	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Qn		31 37	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Qn		42	ns

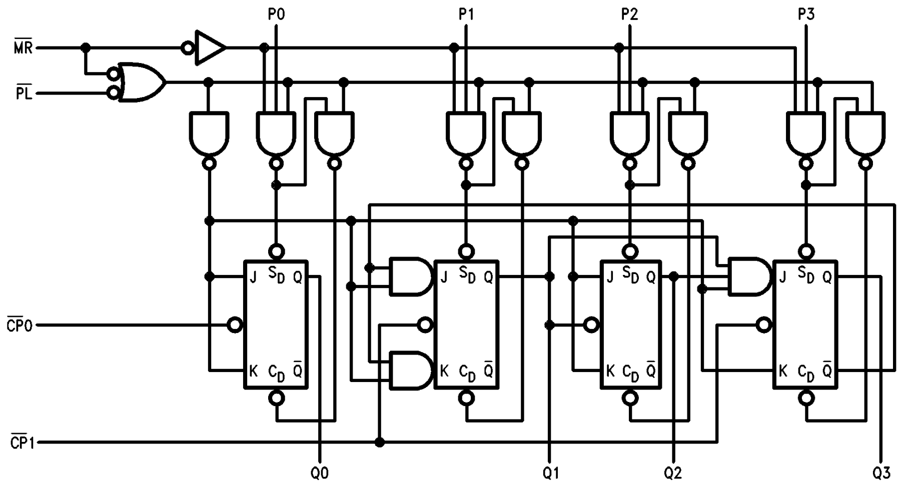
Functional Description

The '196 and '197 are asynchronous presettable decade and binary ripple counters. The '196 decade counter is partitioned into divide-by-two and divide-by-five sections while the '197 is partitioned into divide-by-two and divide-by-eight sections, with all sections having a separate Clock input. In the counting modes, state changes are initiated by the HIGH-to-LOW transition of the clock signals. State changes of the Q outputs, however, do not occur simultaneously because of the internal ripple delays. When using external logic to decode the Q outputs, designers should bear in mind that the unequal delays can lead to decoding spikes and thus a decoded signal should not be used as a clock or strobe. The $\overline{CP}0$ input serves the Q0 flip-flop in both circuit types while the $\overline{CP}1$ input serves the divide-by-five or divide-by-eight section. The Q0 output is designed and specified to drive the rated fan-out plus the $\overline{CP}1$ input. With the input frequency connected to $\overline{CP}0$ and with Q0 driving $\overline{CP}1$, the '197 forms a straight forward modulo-16 counter, with Q0 the least significant output and Q3 the most significant output.

The '196 decade counter can be connected up to operate in two different count sequences. With the input frequency connected to $\overline{CP}0$ and with Q0 driving $\overline{CP}1$, the circuit counts in the BCD (8421) sequence. With the input frequency connected to $\overline{CP}1$ and Q3 driving $\overline{CP}0$, Q0 becomes the low frequency output and has a 50% duty cycle waveform. Note that the maximum counting rate is reduced in the latter (bi-quinary) configuration because of the interstage gating delay within the divide-by-five section.

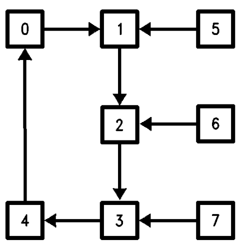
The '196 and '197 have an asynchronous active LOW Master Reset input ($\overline{MR}$) which overrides all other inputs and forces all outputs LOW. The counters are also asynchronously presettable. A LOW on the Parallel Load input ($\overline{PL}$) overrides the clock inputs and loads the data from Parallel Data (P0–P3) inputs into the flip-flops. While $\overline{PL}$ is LOW, the counters act as transparent latches and any change in the Pn inputs will be reflected in the outputs. In order for the intended parallel data to be entered and stored, the recommended setup and hold times with respect to the rising edge of $\overline{PL}$ should be observed.

Logic Diagram



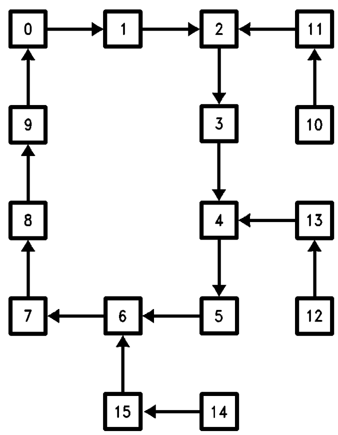
TL/F/10179–3

÷5 State Diagram



TL/F/10179–4

BCD State Diagram



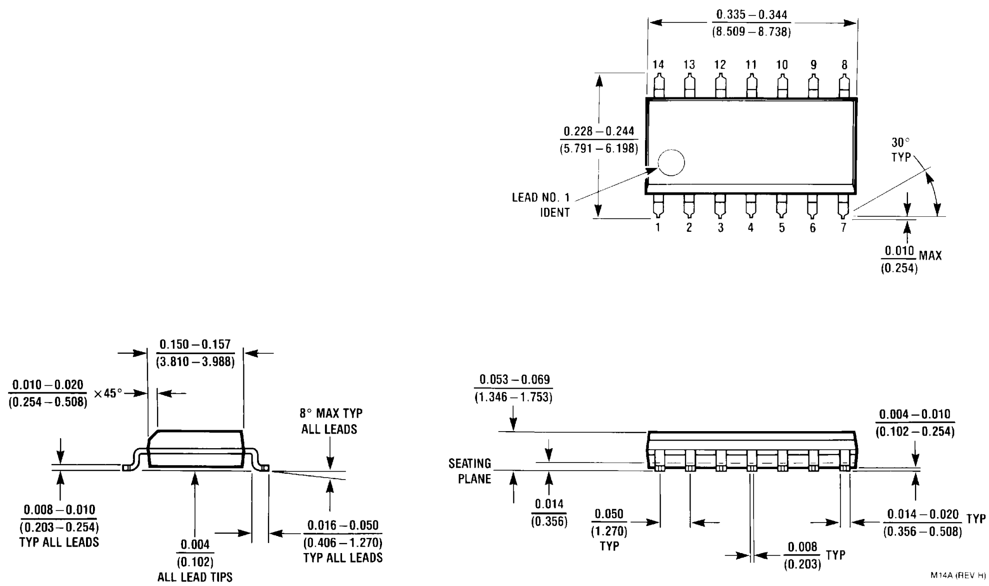
TL/F/10179–5

Mode Select Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Qn forced LOW
H	L	X	Pn → Qn
H	H	⌐_	Count Up

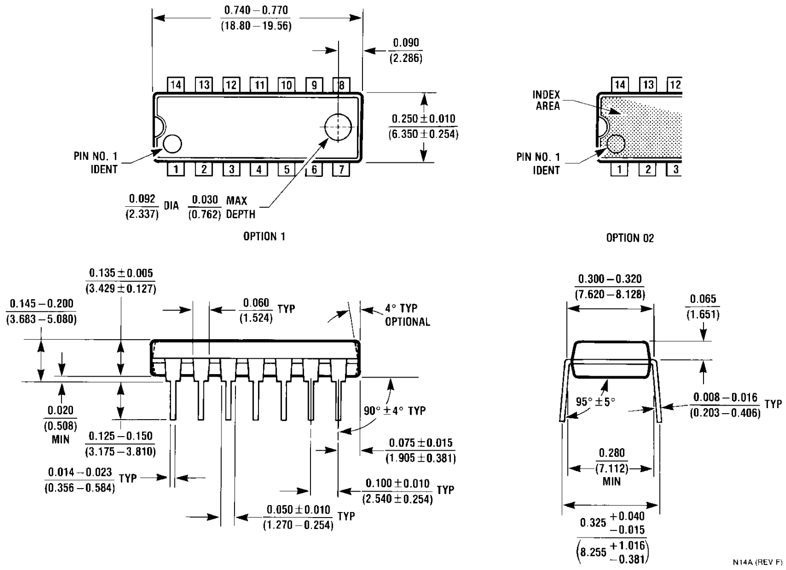
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS196M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS196N
NS Package Number N14A

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National Semiconductor

February 1992

DM74LS197 Presettable Binary Counters

General Description

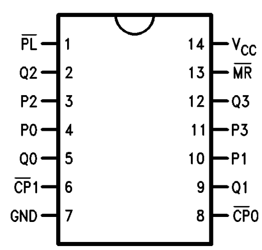
The 'LS197 ripple counter contains divide-by-two and divide-by-eight sections which can be combined to form a modulo-16 binary counter. State changes are initiated by the falling edge of the clock. The 'LS197 has a Master Reset ($\overline{MR}$) input which overrides all other inputs and asynchronously forces all outputs LOW. A Parallel Load input ($\overline{PL}$) overrides clocked operations and asynchronously loads the data on the Parallel Data inputs (P_n) into the flip-flops. This preset feature makes the circuit usable as a programmable counter. The circuit can also be used as a 4-bit latch, loading data from the Parallel Data inputs when $\overline{PL}$ is LOW and storing the data when $\overline{PL}$ is HIGH. For detail specifications and functional description, please refer to the 'LS196 data sheet.

Features

- High counting rates—Typically 70 MHz
- Asynchronous preset
- Asynchronous master reset

Connection Diagram

Dual-In-Line Package



TL/F/10180–1

Order Number DM74LS197M or DM74LS197N
See NS Package Number M14A or N14A

Pin Names	Description
$\overline{CP0}$	÷2 Section Clock Input (Active Falling Edge)
$\overline{CP1}$	÷8 Section Clock Input (Active Falling Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
P0–P3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
Q0	÷2 Section Output*
Q1–Q3	÷8 Section Outputs

*Q0 output is guaranteed to drive the full rated fan-out plus the $\overline{CP1}$ input.

Mode Select Table

Inputs			Response
$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	
L	X	X	Qn Forced LOW
H	L	X	Pn → Qn
H	H	⌐_	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM74LS197			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Voltage			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

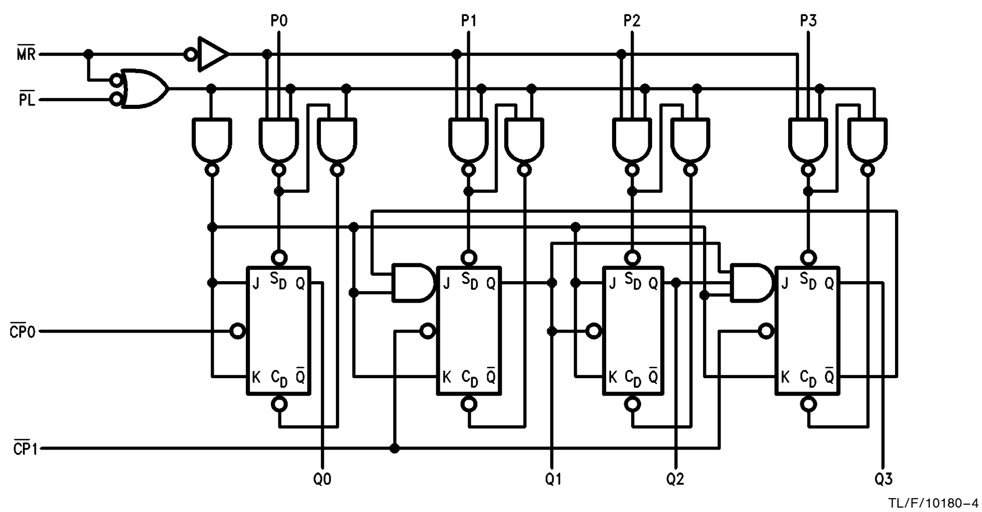
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

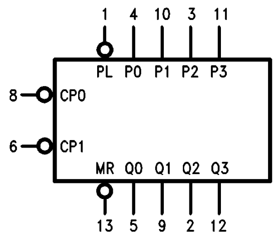
$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$		Units
		Min	Max	
f_{MAX}	Max CLK Frequency	55		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP0}$ to Q0		15 15	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q2		34 34	ns
t_{PLH} t_{PHL}	Propagation Delay P2 to Q2		27 44	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q2		39 45	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q1		15 17	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP1}$ to Q3		55 63	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q3		42	ns

Logic Diagram



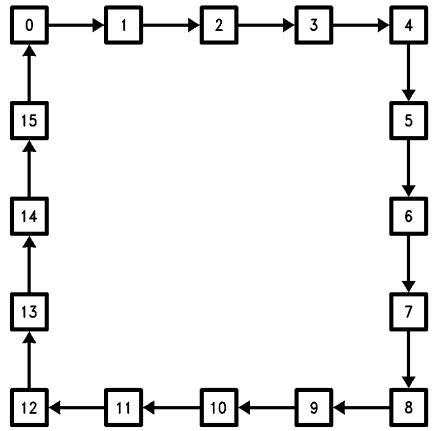
Logic Symbol



TL/F/10180–2

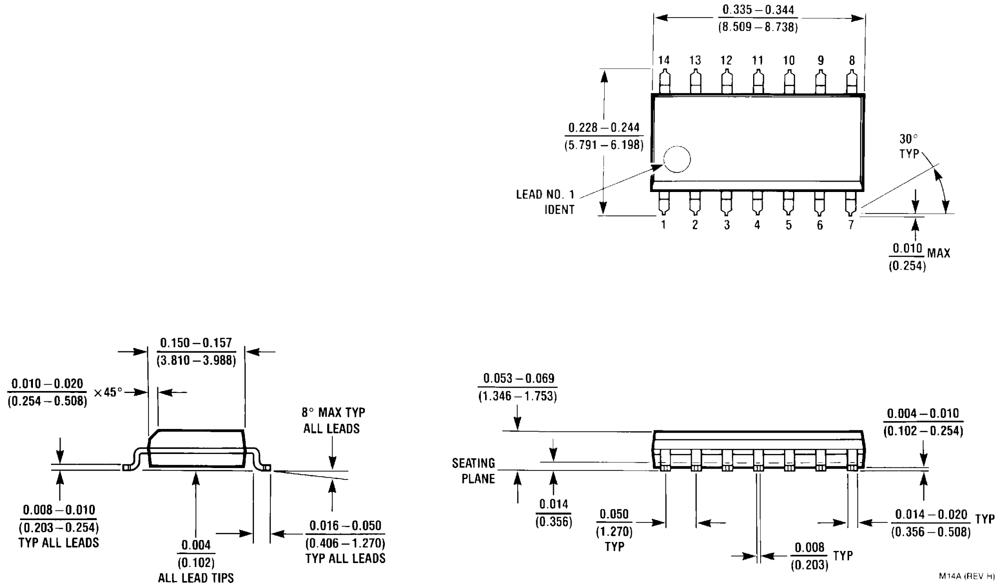
V_{CC} = Pin 14
GND = Pin 7

÷ 16 State Diagram



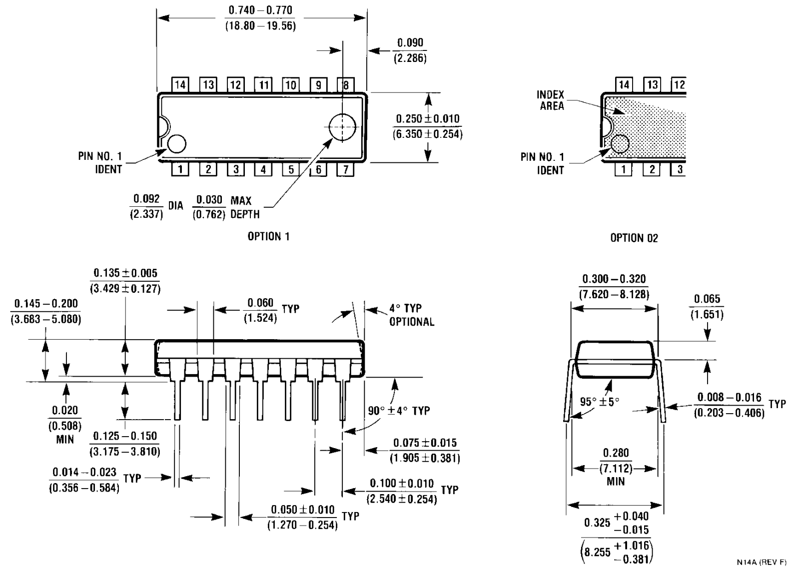
TL/F/10180–3

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS197M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS197N
NS Package Number N14A

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FAIRCHILD
SEMICONDUCTOR ™

March 1998

DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin (B) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations
- Pin-out identical to 'LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity
- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

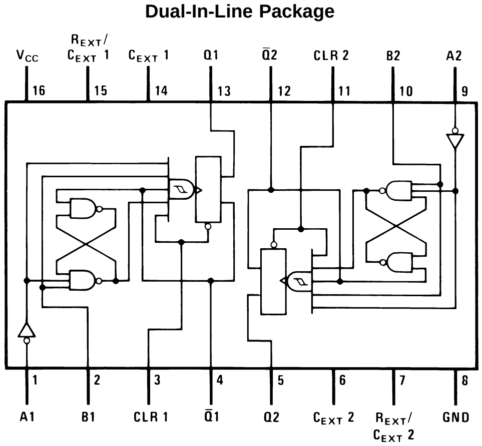
Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Note 1: The pin-out is identical to 'LS123 but, functionally it is not; refer to Operating Rules #10 in this datasheet.

Connection Diagram

Dual-In-Line Package



DS006409-1

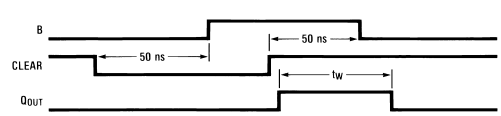
Order Number DM74LS221M or DM74LS221N
See Package Number M16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊔
H	↓	H	⊓	⊔
↑ (Note 2)	L	H	⊓	⊔

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⊓ = A Positive Pulse
⊔ = A Negative Pulse

Note 2: This mode of triggering requires first the B input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.



DS006409-2

 DS006409

Absolute Maximum Ratings (Note 4)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM74LS221			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	0.9		V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width (Note 3)	Data	40			ns
		Clear	40			
t_{REL}	Clear Release Time (Note 3)		15			ns
$\frac{dV}{dt}$	Rate of Rise or Fall of Schmitt Input (B) (Note 3)				1	$\frac{V}{s}$
$\frac{dV}{dt}$	Rate of Rise or Fall of Logic Input (A) (Note 3)				1	$\frac{V}{\mu s}$
R_{EXT}	External Timing Resistor (Note 3)		1.4		100	kΩ
C_{EXT}	External Timing Capacitance (Note 3)		0		1000	µF
DC	Duty Cycle (Note 3)	R_T = 2 kΩ			50	%
		$R_T = R_{EXT}$ (Max)			60	
T_A	Free Air Operating Temperature		0		70	˚C

Note 3: T_A = 25˚C and V_{CC} = 5V.

Note 4: *The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the “Electrical Characteristics” table are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min		0.35	0.5	V
		V_{CC} = Min, I_{OL} = 4 mA			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A1, A2			−0.4	mA
			B			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 6)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		4.7	11	mA
			Triggered		19	27	

Note 5: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF, R_{EXT} = 2 kΩ, C_L = 15 pF, R_L = 2 kΩ		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to Q			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			65	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q			55	ns
$t_{W(out)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0, R_{EXT} = 2 kΩ, R_L = 2 kΩ, C_L = 15 pF	20	70	ns
$t_{W(out)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF, R_{EXT} = 10 kΩ, R_L = 2 kΩ, C_L = 15 pF	600	750	ns
			C_{EXT} = 1 µF, R_{EXT} = 10 kΩ, R_L = 2 kΩ, C_L = 15 pF	6	7.5	ms
			C_{EXT} = 80 pF, R_{EXT} = 2 kΩ, R_L = 2 kΩ, C_L = 15 pF	70	150	ns

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to approximately 1000 µF. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS221 one-shot and should not be used.

   Furthermore, if a polarized timing capacitor is used on the 'LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin (*Figure 1*).
3. For $C_X >> 1000$ pF, the output pulse width (T_W) is defined as follows:

   $T_W = KR_X\ C_X$

   where [R_X is in kΩ]

   [C_X is in pF]

   [T_W is in ns]

   $K \approx \text{Ln}2 = 0.70$
4. The multiplicative factor K is plotted as a function of C_X for design considerations: (See *Figure 2*).
5. For $C_X < 1000$ pF see *Figure 3* for T_W vs C_X family curves with R_X as a parameter.
6. To obtain variable pulse widths by remote trimming, the following circuit is recommended: (See *Figure 4*).
7. Output pulse width versus V_{CC} and temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}. *Figure 6* depicts pulse width variation versus temperatures.
8. Duty cycle is defined as T_W/T x 100 in percentage, if it goes above 50% the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes output pulse width to vary, or jitter (a function of the R_{EXT} only). To reduce jitter, R_{EXT} should be as large as possible, for example, with R_{EXT} = 100k jitter is not appreciable until the duty cycle approaches 90%.
9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. Although the 'LS221's pin-out is identical to the 'LS123 it should be remembered that they are not functionally identical. The 'LS123 is a retriggerable device such that the output is dependent upon the input transitions when its output "Q" is at the "High" state. Furthermore, it is recommended for the 'LS123 to externally ground the C_{EXT} pin for improved system performance. However, this pin on the 'LS221 is not an internal connection to the device ground. Hence, if substitution of an 'LS221 onto an 'LS123 design layout where the C_{EXT} pin is wired to the ground, the device will not function.
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

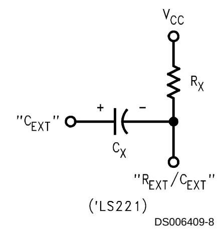


FIGURE 1.

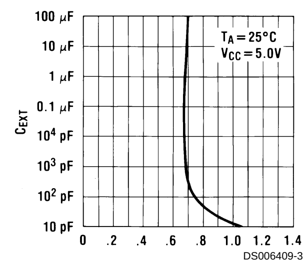


FIGURE 2.

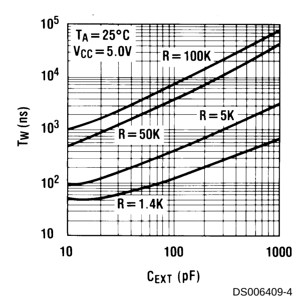
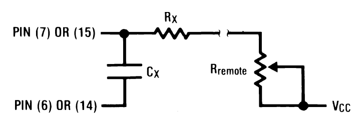


FIGURE 3.



Note: "R_{remote}" should be as close to the one-shot as possible.

FIGURE 4.

Operating Rules (Continued)

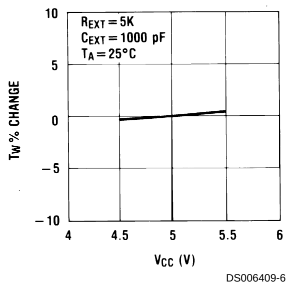


FIGURE 5.

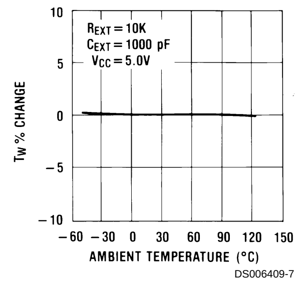
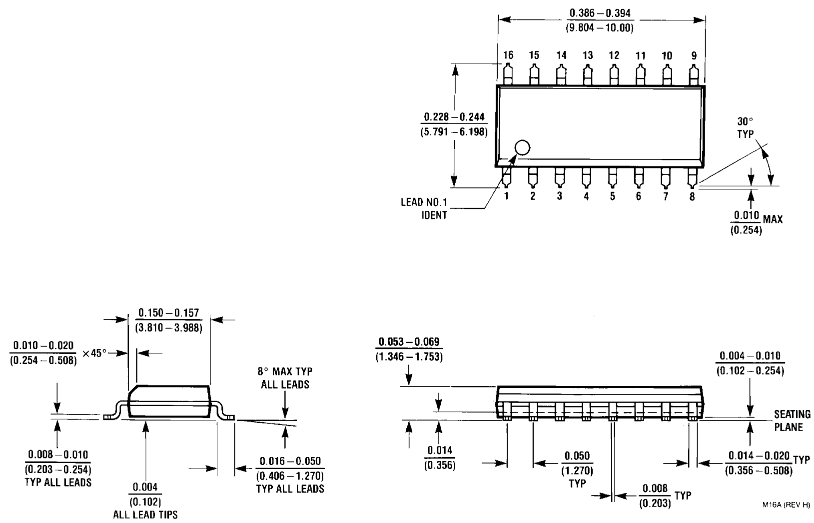


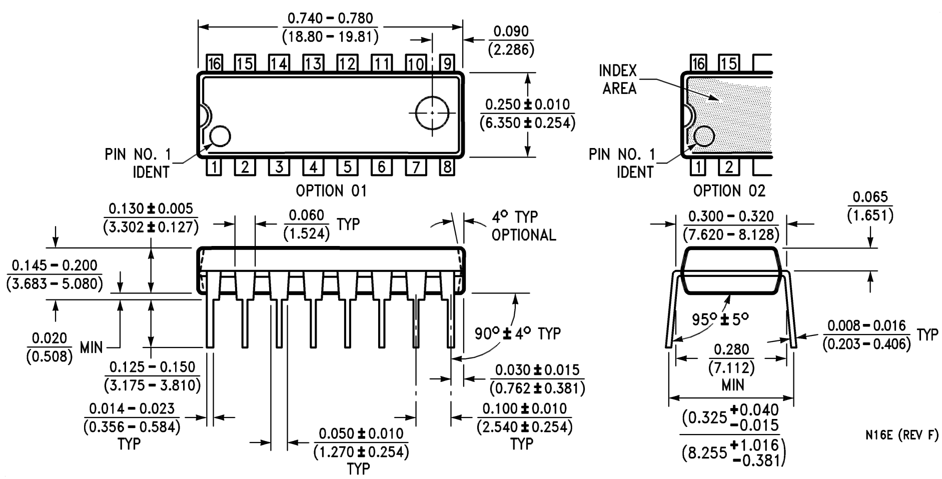
FIGURE 6.

Note: For further detailed device characteristics and output performance, please refer to the NSC one-shot application note AN-372.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Molded Package (M)
Order Number DM74LS221M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS221N
Package Number N16E

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March 1998

DM74LS240, DM74LS241 Octal 3-STATE Buffers/Line Drivers/Line Receivers

General Description

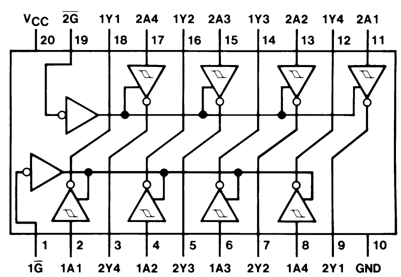
These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  54LS 12 mA
  74LS 24 mA
- Typical I_{OH} (source current)
  54LS −12 mA
  74LS −15 mA
- Typical propagation delay times
  Inverting 10.5 ns
  Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  Inverting 130 mW
  Noninverting 135 mW

Connection Diagrams

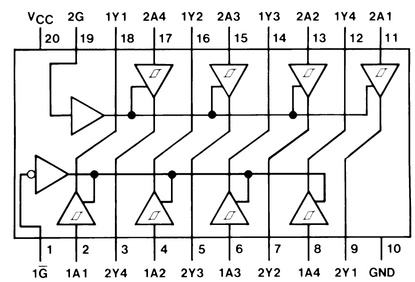
Dual-In-Line Package



DS006411-1

Order Number DM54LS240J, DM54LS240W, DM54LS240E, DM74LS240WM or DM74LS240N
See Package Number E20A, J20A, M20B, N20A or W20A

Dual-In-Line Package



DS006411-2

Order Number DM54LS241J, DM54LS241W, DM54LS241E, DM74LS241WM or DM74LS241N
See Package Number E20A, J20A, M20B, N20A or W20A

Function Tables

LS240

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

LS241

Inputs				Outputs	
G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS, 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS240, 241			DM74LS240, 241			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V (DM74), V_I = 10V (DM54)					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High	LS240, LS241		13	23	mA
			Outputs Low	LS240		26	44	
				LS241		27	46	
			Outputs Disabled	LS240		29	50	
				LS241		32	54	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

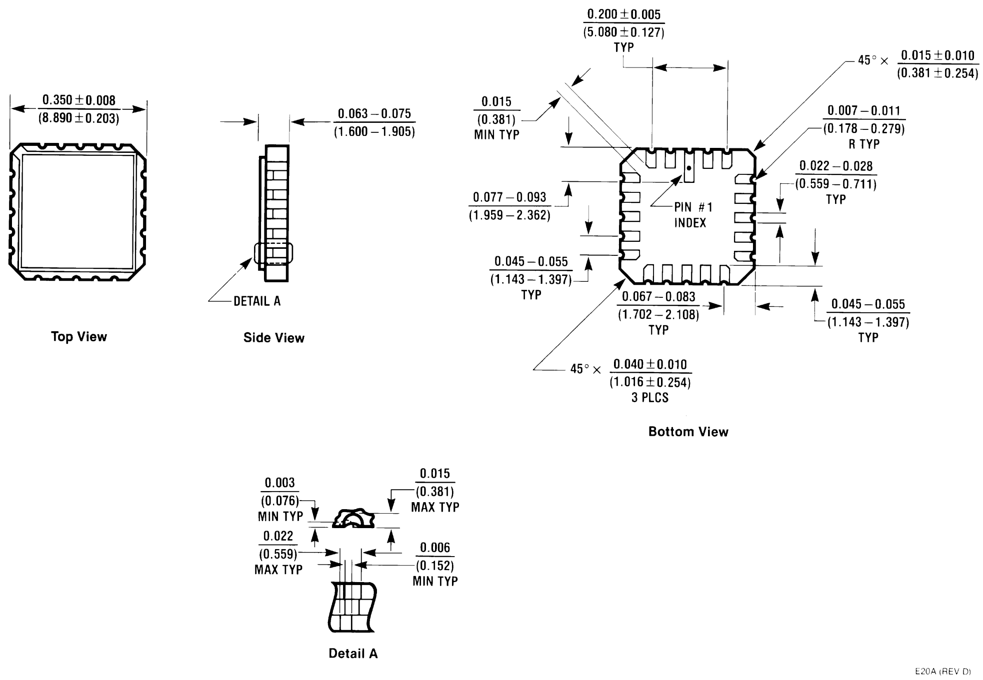
Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	Conditions		DM54LS Max	DM74LS Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF	LS240	18	14	ns
		R_L = 667Ω	LS241	18	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF	LS240	18	18	ns
		R_L = 667Ω	LS241	18	18	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF	LS240	30	30	ns
		R_L = 667Ω	LS241	30	30	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF	LS240	23	23	ns
		R_L = 667Ω	LS241	23	23	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF	LS240	25	25	ns
		R_L = 667Ω	LS241	25	25	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF	LS240	18	18	ns
		R_L = 667Ω	LS241	18	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF	LS240		18	ns
		R_L = 667Ω	LS241		21	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF	LS240		22	ns
		R_L = 667Ω	LS241		22	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF	LS240		33	ns
		R_L = 667Ω	LS241		33	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF	LS240		26	ns
		R_L = 667Ω	LS241		26	

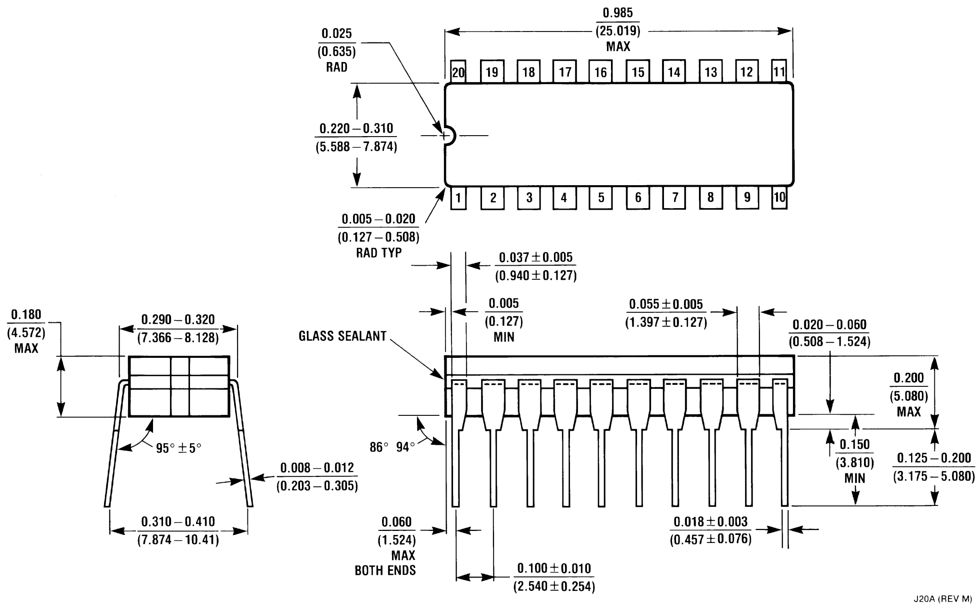
Note 4: 54LS Output load is C_L = 50 pF for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH}.

Physical Dimensions inches (millimeters) unless otherwise noted

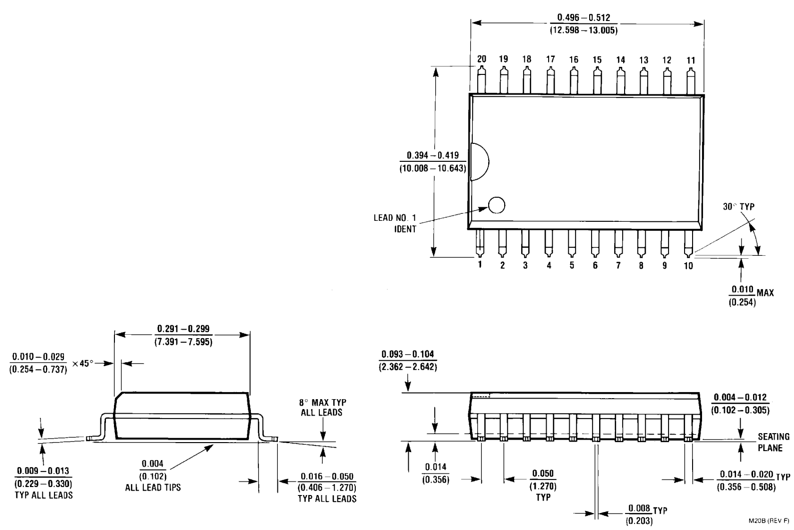


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS240E or DM54LS241E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

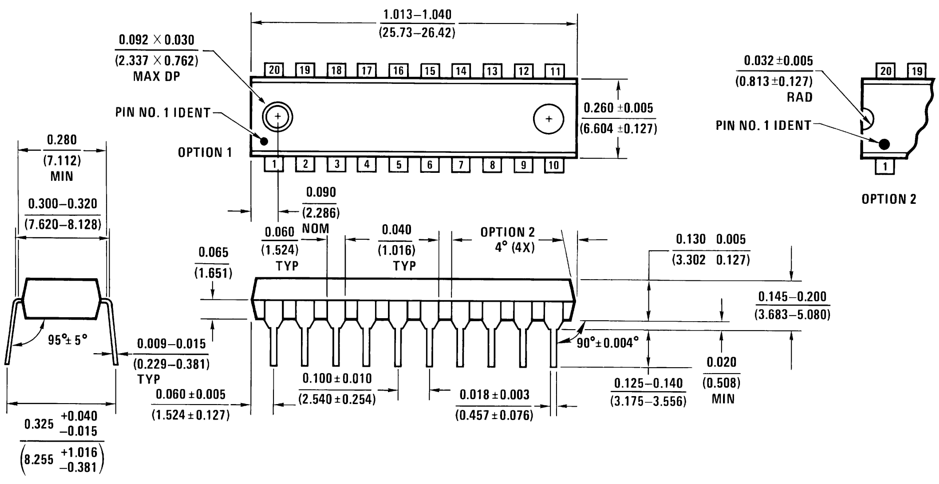


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS240J or DM54LS241J
Package Number J20A

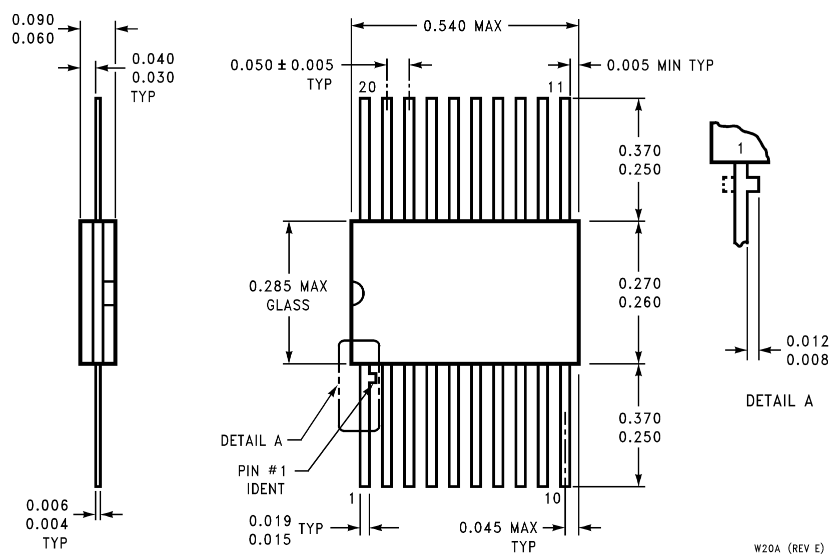


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS240WM or DM74LS241WM
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS240N or DM74LS241N
Package Number N20A



20-Lead Ceramic Flat Package (W)
Order Number DM54LS240W or DM54LS241W
Package Number W20A

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March 1998

DM74LS243
Quadruple Bus Transceiver

General Description

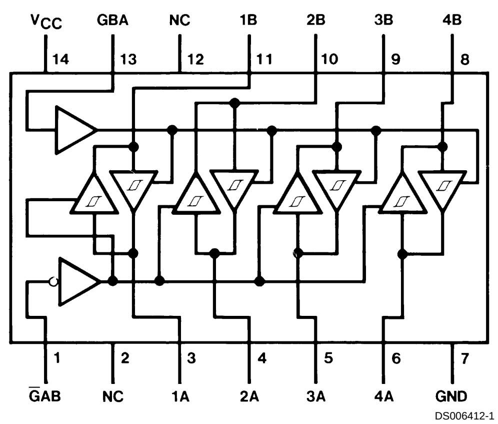
This four data line transceiver is designed for asynchronous two-way communications between data buses. It can be used to drive terminated lines down to 133Ω.

Features

- Two-way asynchronous communication between data buses
- PNP inputs reduce DC loading on bus line
- Hysteresis at data inputs improves noise margin

Connection Diagram

Dual-In-Line Package



Order Number DM74LS243WM or DM74LS243N
See Package Number M14B or N14A

Function Table

Control Inputs		Data Port Status	
$\overline{G}$ AB	**GBA**	**A**	**B**
H	H	O	I
L	H	(Note 1)	(Note 1)
H	L	ISOLATED	
L	L	I	O

I = Input, O = Output.

H = High Logic Level, L = Low Logic Level.

Note 1: Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

Absolute Maximum Ratings (Note 2)

Supply Voltage	7V
Input Voltage	
Any G	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM74LS243			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−15	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Note 2: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
HYS	Hysteresis (V_{T+} − V_{T-}) (Data Inputs Only)	V_{CC} = Min	0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min; I_{OL} = 12 mA			0.4	V
		I_{OL} = Max			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min; V_O = 2.7V			40	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_O = 0.4V			−200	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max; V_I = 5.5V; A or B			0.1	mA
		V_I = 7V; Any G			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max Outputs Open; Outputs High		22	38	mA
		Outputs Low		29	50	
		Outputs Disabled		32	54	

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

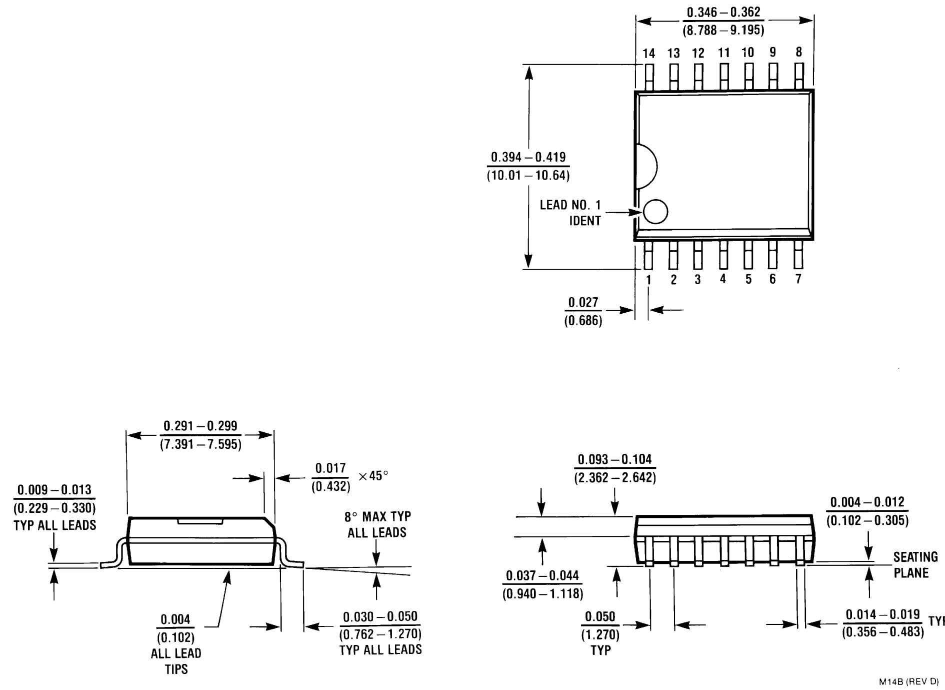
Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

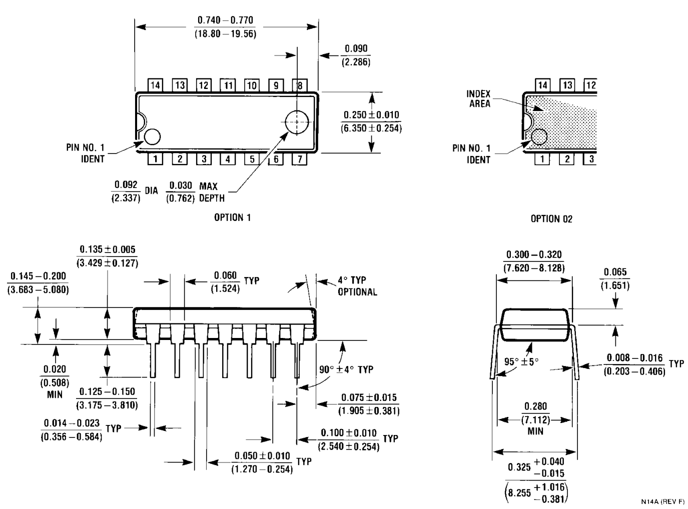
at V_{CC} = 5V, T_A = 25°C (for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 667Ω		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 667Ω		18	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 667Ω		30	ns
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 667Ω		23	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 667Ω		25	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 667Ω		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 667Ω		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 667Ω		22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 667Ω		33	ns
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 667Ω		26	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Wide Small Outline Package (M)
Order Number DM74LS243WM
Package Number M14B



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS243N
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS244
Octal 3-STATE Buffers/Line Drivers/Line Receivers

General Description

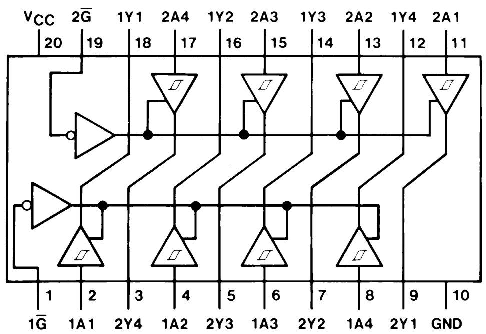
These buffers/line drivers are designed to improve both the performance and PC board density of 3-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at data inputs improves noise margins
- Typical I_{OL} (sink current)
  54LS 12 mA
  74LS 24 mA
- Typical I_{OH} (source current)
  54LS −12 mA
  74LS −15 mA
- Typical propagation delay times
  Inverting 10.5 ns
  Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  Inverting 130 mW
  Noninverting 135 mW

Connection Diagram

Dual-In-Line Package



DS008442-1

Order Number 54LS244DMQB, 54LS244FMQB, 54LS244LMQB, DM74LS244WM or DM74LS244N
See Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$) Data Inputs Only	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		54LS/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		54LS/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	54LS/DM74			0.4	V
			I_{OL} = Max	DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V (DM74) V_I = 10V (54LS)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V		−0.5		−200	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		54LS	−50		−225	mA
				DM74	−40			
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

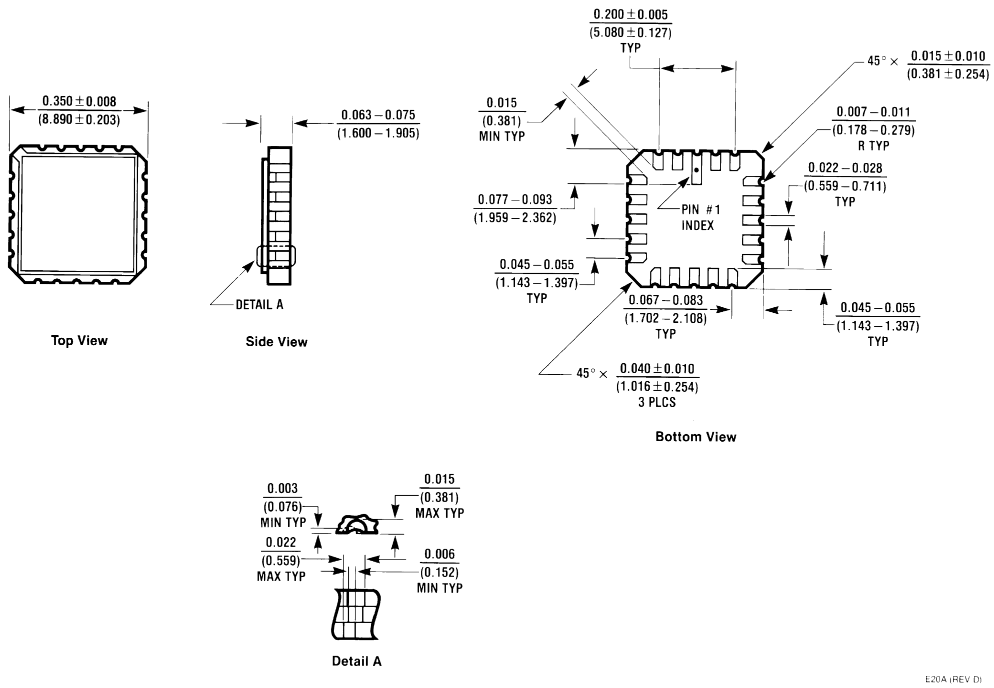
Switching Characteristics

at V_{CC} = 5V, T_A = 25˚C

Symbol	Parameter	Conditions	54LS Max	DM74LS Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 667Ω	18	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 667Ω	18	18	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 667Ω	30	30	ns
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 667Ω	23	23	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 667Ω	25	25	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 667Ω	18	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 667Ω		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 667Ω		22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 667Ω		33	ns
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 667Ω		26	ns

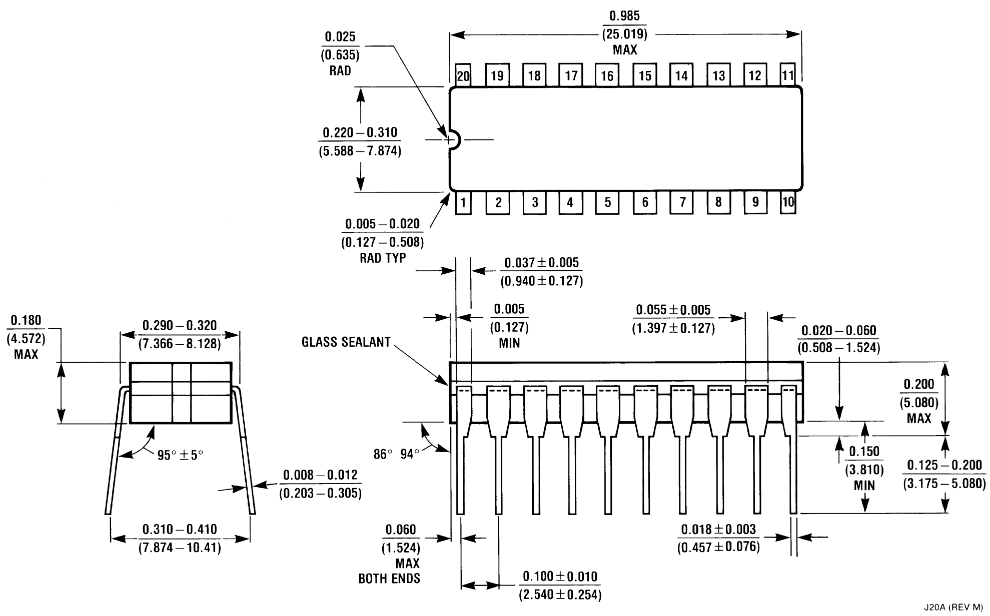
Note 4: 54LS Output Load is C_L = 50 pF for t_{PLH}, t_{PHL}, t_{PZL} and t_{PZH}.

Physical Dimensions inches (millimeters) unless otherwise noted



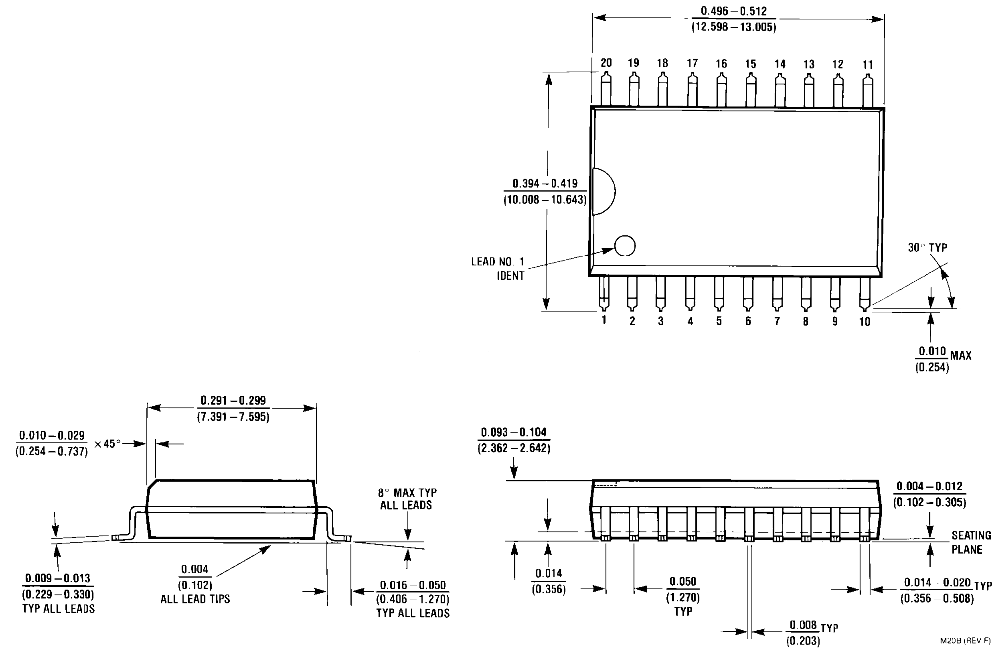
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS244LMQB
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

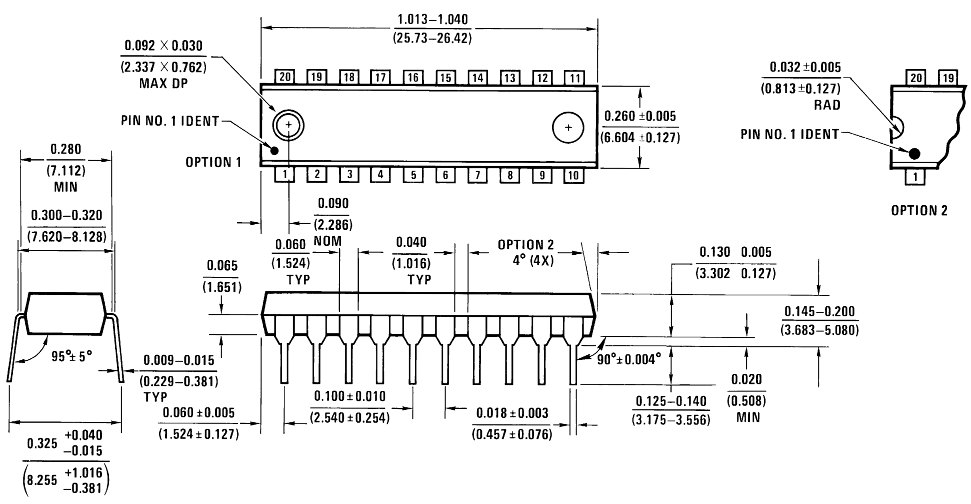


20-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS244DMQB
Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

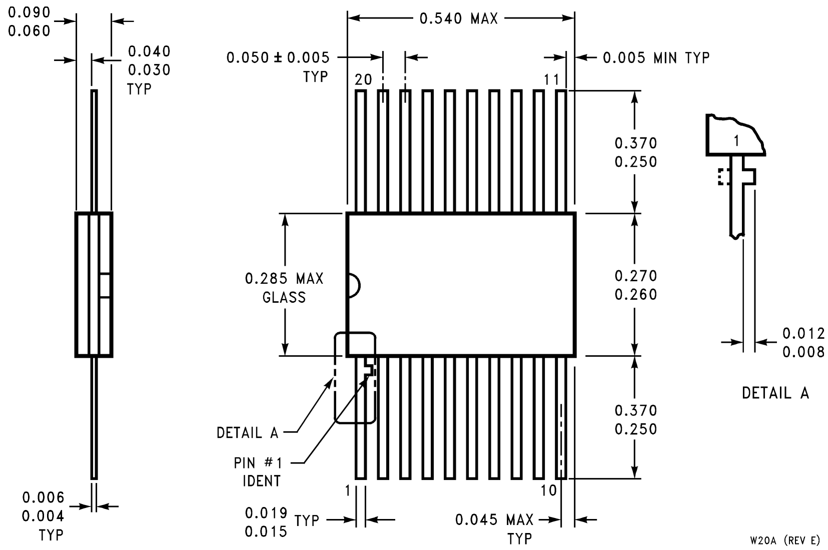


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS244WM
Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS244N
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flat Package (W)
Order Number 54LS244FMQB
Package Number W20A

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March 1998

DM74LS245
3-STATE Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

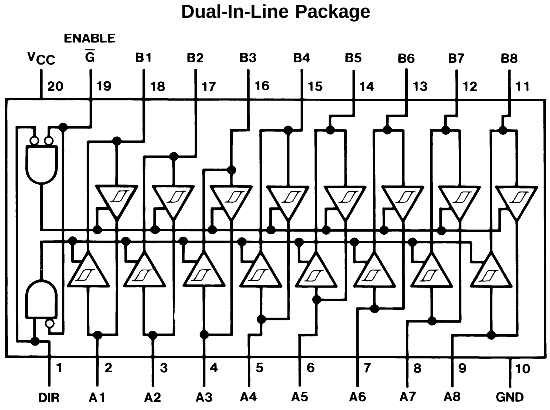
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$)can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-Directional bus transceiver in a high-density 20-pin package
- 3-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  54LS 12 mA
  74LS 24 mA
- I_{OH} (source current)
  54LS −12 mA
  74LS −15 mA
- Alternate Military/Aerospace device (54LS245) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS245DMQB, 54LS245FMQB, 54LS245LMQB, DM54LS245J, DM54LS245W, DM74LS245WM or DM74LS245N See Package Number E20A, J20A, M20B, N20A or W20A

Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS245			DM74LS245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IL} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	µA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	µA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)			−40		−225	mA
I_{CC}	Supply Current	Outputs High		V_{CC} = Max		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

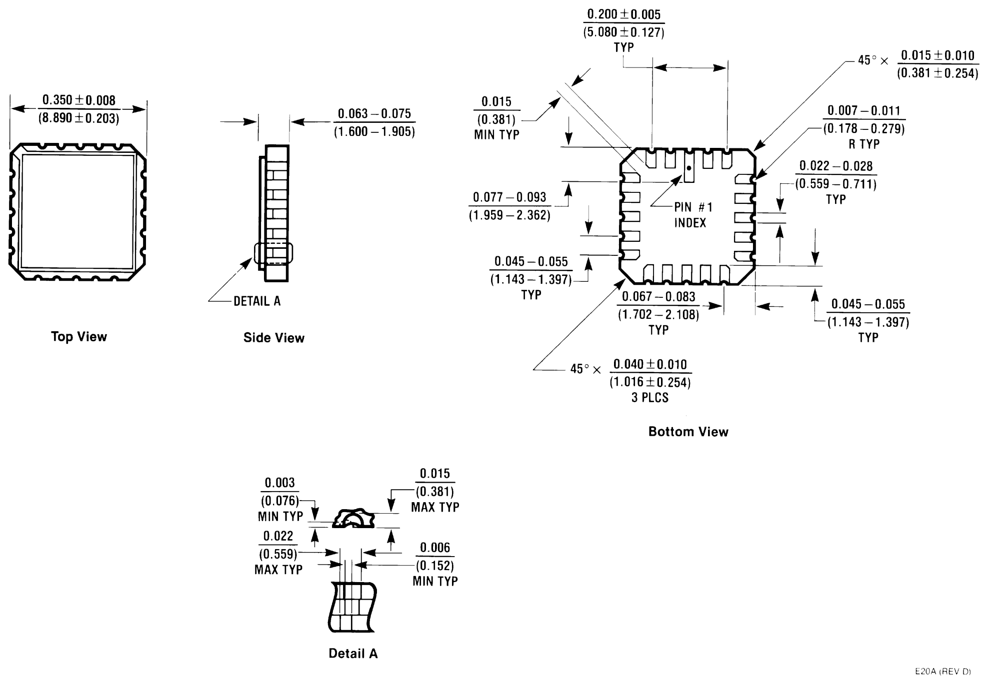
Note 3: Not more than one output should be shorted at a time, not to exceed one second duration

Switching Characteristics

$V_{CC} = 5V$, $T_A = 25°C$

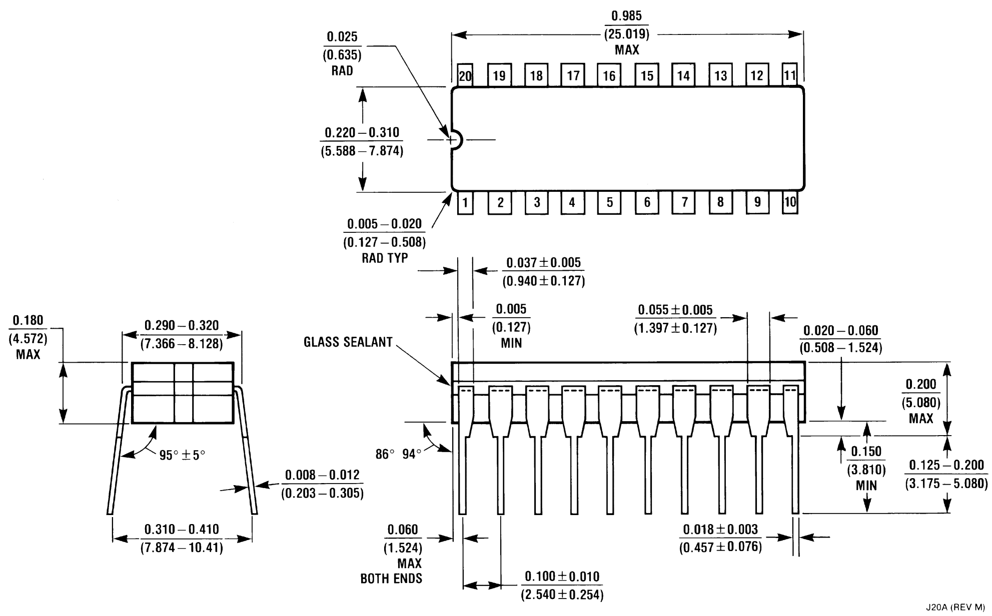
Symbol	Parameter	Conditions	DM54/74 LS245		Units
			Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$C_L = 45$ pF $R_L = 667\Omega$		12	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			12	ns
t_{PZL}	Output Enable Time to Low Level			40	ns
t_{PZH}	Output Enable Time to High Level			40	ns
t_{PLZ}	Output Disable Time from Low Level	$C_L = 5$ pF $R_L = 667\Omega$		25	ns
t_{PHZ}	Output Disable Time from High Level			25	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	$C_L = 150$ pF $R_L = 667\Omega$		16	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			17	ns
t_{PZL}	Output Enable Time to Low Level			45	ns
t_{PZH}	Output Enable Time to High Level			45	ns

Physical Dimensions inches (millimeters) unless otherwise noted



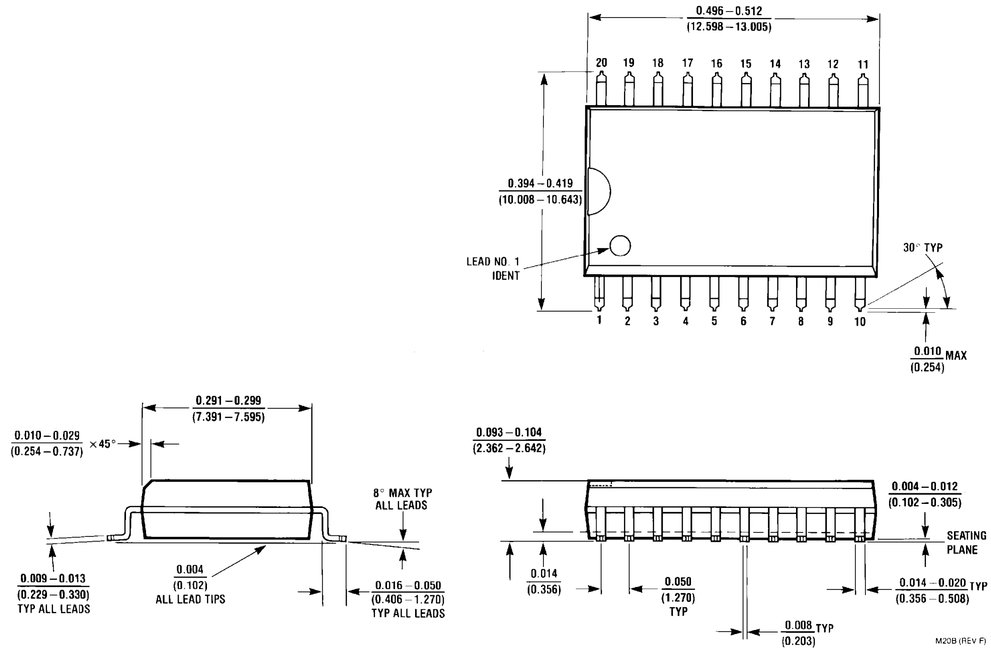
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS245LMQB
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

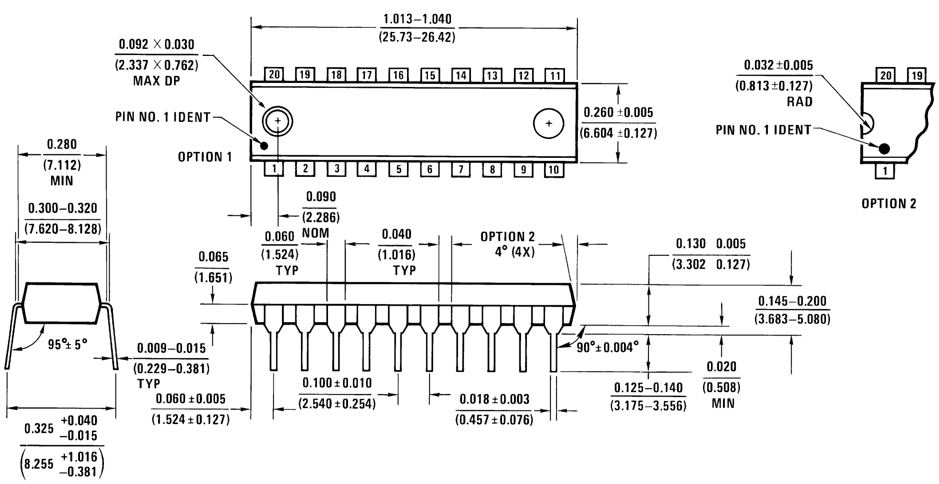


20-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS245DMQB or DM54LS245J
Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

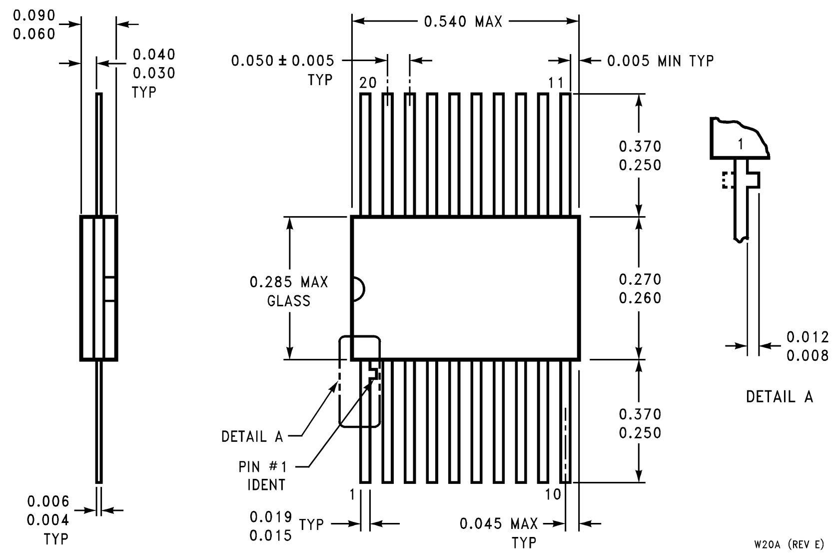


20-Lead Small Outline Molded Package (M)
Order Number DM74LS245WM
Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS245N
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flat Package (W)
Order Number 54LS245FMQB or DM54LS245W
Package Number W20A

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March 1998

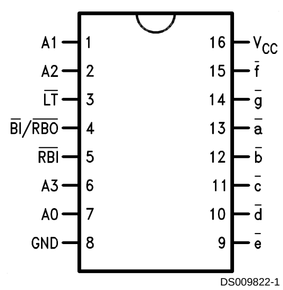
DM74LS247 BCD to 7-Segment Decoder/Driver with Open-Collector Outputs

General Description

The 'LS247 has active LOW open-collector outputs guaranteed to sink 24 mA. It has the same electrial characteristics and pin connections as the 'LS47. The only difference is that the 'LS247 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for number 9. For detailed description and specifications please refer to the 'LS47 data sheet.

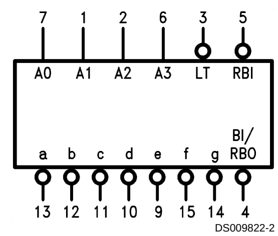
Connection Diagram

Dual-In-Line Package



Order Number DM74LS247M or DM74LS247N
See Package Number M16A or N16E

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	Segment Outputs (Active LOW)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current $\overline{BI}/\overline{RBO}$			−50	μA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4	3.4		V
I_{OFF}	Output High Current Segment Outputs	V_{CC} = 5.5V, V_O = 15V			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min; I_{OL} = Max, V_{IH} = Min		0.35	0.5	V
		V_{CC} = Min; I_{OL} = 3.2 mA; $\overline{BI}/\overline{RBO}$			0.5	
		V_{CC} = Min; I_{OL} = 12 mA; $\overline{a}$ –$\overline{g}$		0.25	0.4	
		V_{CC} = Min; I_{OL} = 1.6 mA; $\overline{BI}/\overline{RBO}$			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V; Other Inputs			−0.4	mA
		V_{CC} = Max, V_I = 0.4V; $\overline{BI}/\overline{RBO}$ Input			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−0.3		−2.0	mA
I_{CC}	Supply Current	V_{CC} = Max			13	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

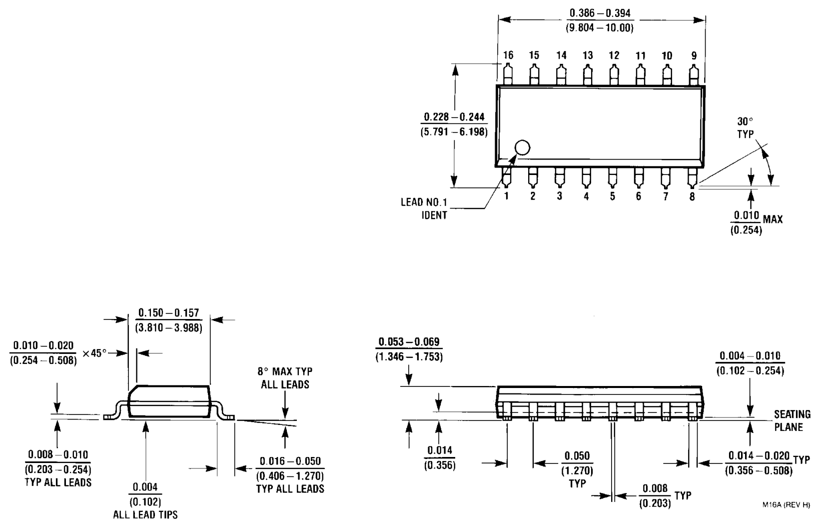
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

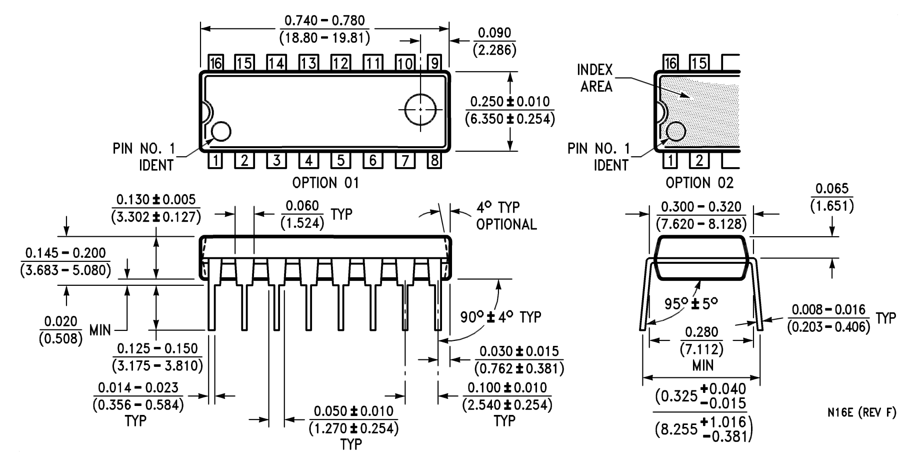
V_{CC} = +5V, T_A = +25˚C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF Min	R_L = 2 kΩ, C_L = 15 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		100	ns

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Molded Package (M)
Order Number DM74LS247M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS247N
Package Number N16E

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National Semiconductor

February 1992

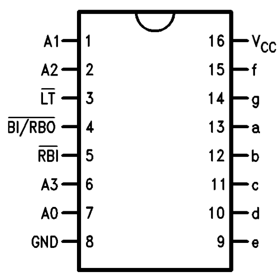
DM74LS248
BCD to 7-Segment Decoder with 2 kΩ Pull-Up Resistors

General Description

The ’LS248 has active HIGH outputs with internal 2 kΩ pull-up resistors. It has the same electrical characteristics and pin connections as the ’LS48. The only difference is that the ’LS248 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9. For detailed description and specifications please refer to the ’LS48 data sheet.

Connection Diagram

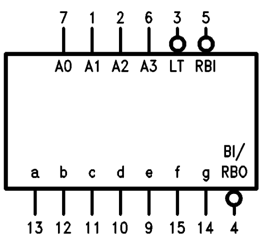
Dual-In-Line Package



TL/F/10181–1

Order Number DM74LS248M or DM74LS248N
See NS Package Number M16A or N16E

Logic Symbol



TL/F/10181–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI/RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a–g	Segment Outputs (Active HIGH)

 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Voltage			−0.1	mA
I_{OL}	Low Level Output Current			6	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 3.2 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−0.3		−2.0	mA
I_{CC}	Supply Current	V_{CC} = Max			38	mA
I_{OFF}	Output High Current	Segment Inputs, V_O = 0.85V	−1.3			μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

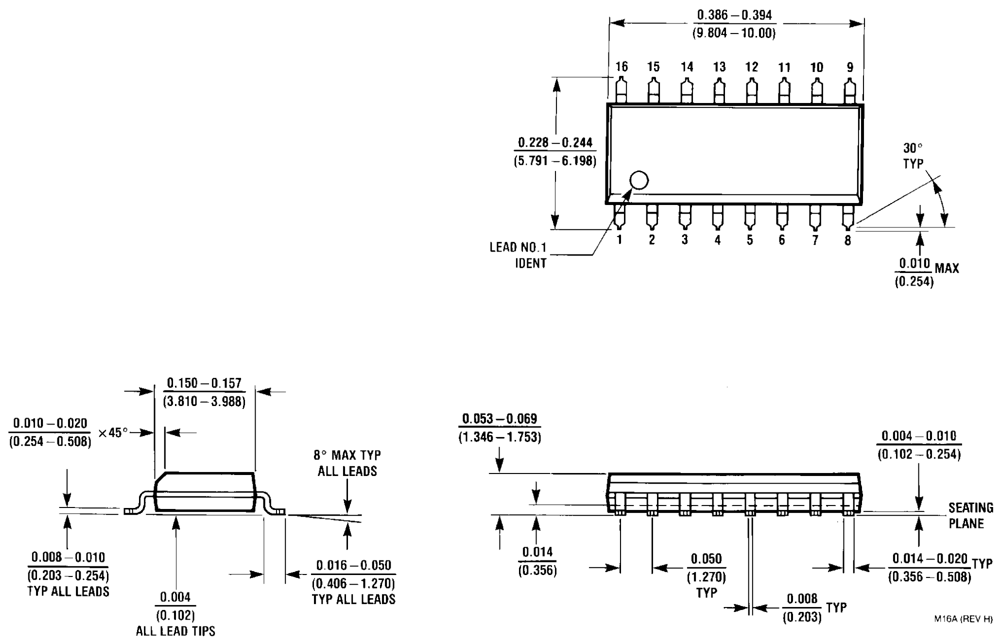
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C

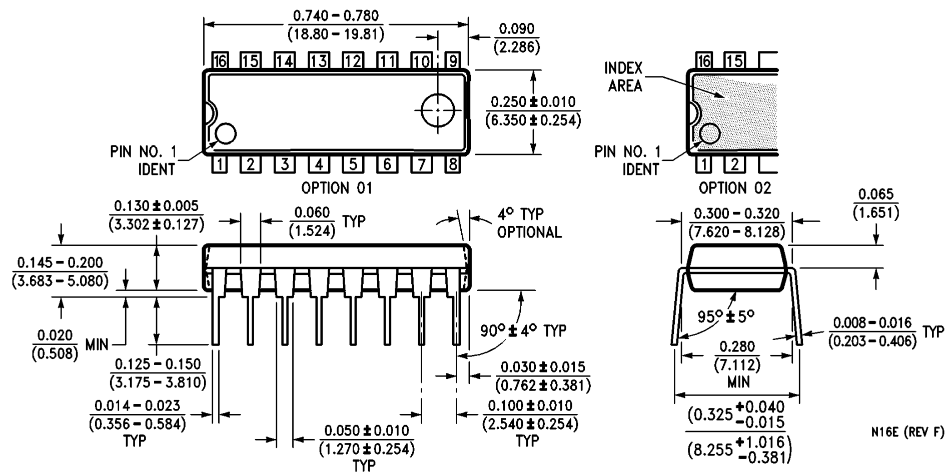
Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		100	ns

Physical Dimensions inches (millimeters)



16-Lead Small Outline Molded Package (M)
Order Number DM74LS248M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS248N
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

February 1992

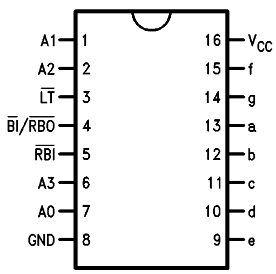
DM74LS249
BCD to 7-Segment Decoder with Open-Collector Outputs

General Description

The 'LS249 has active HIGH open-collector outputs and incorporates the Lamp Test and $\overline{BI}/\overline{RBO}$ inputs. Additionally, the 'LS249 will light the top bar (segment a) for numeral 6 and the bottom bar (segment d) for numeral 9.

Connection Diagram

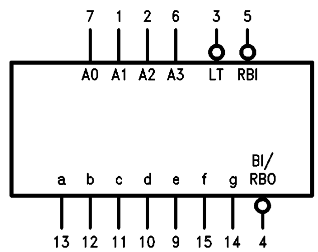
Dual-In-Line Package



TL/F/10213–1

Order Number DM74LS249N
See NS Package Number N16E

Logic Symbol



TL/F/10213–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A_0–A_3	BCD Inputs
$\overline{BI}$	Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
a–g	Segment Outputs (Active HIGH)

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current ($\overline{BI}/\overline{RBO}$)			−0.25	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage ($\overline{BI}/\overline{RBO}$)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.7	3.4		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Min, V_O = 5.5V				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs			−0.4	mA
			$\overline{BI}/\overline{RBO}$			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−0.3		−2.0	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{IN} = 4.5V				15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

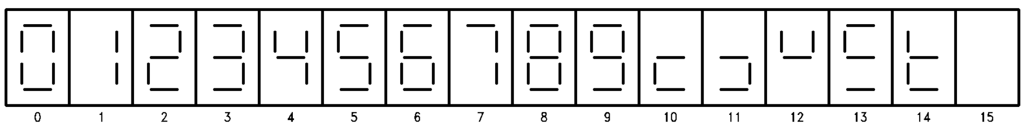
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$ / $C_L = 15\ pF$ Min	$R_L = 2\ k\Omega$ / $C_L = 15\ pF$ Max	Units
t_{PLH} t_{PHL}	Propagation Delay Time A_n to a–g (54LS $R_L = 2\ k\Omega$)		100 100	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{BI}$ to a–g (54LS $R_L = 6\ k\Omega$)		100 100	ns

Numerical Designations—Resultant Displays



TL/F/10213–3

Truth Table

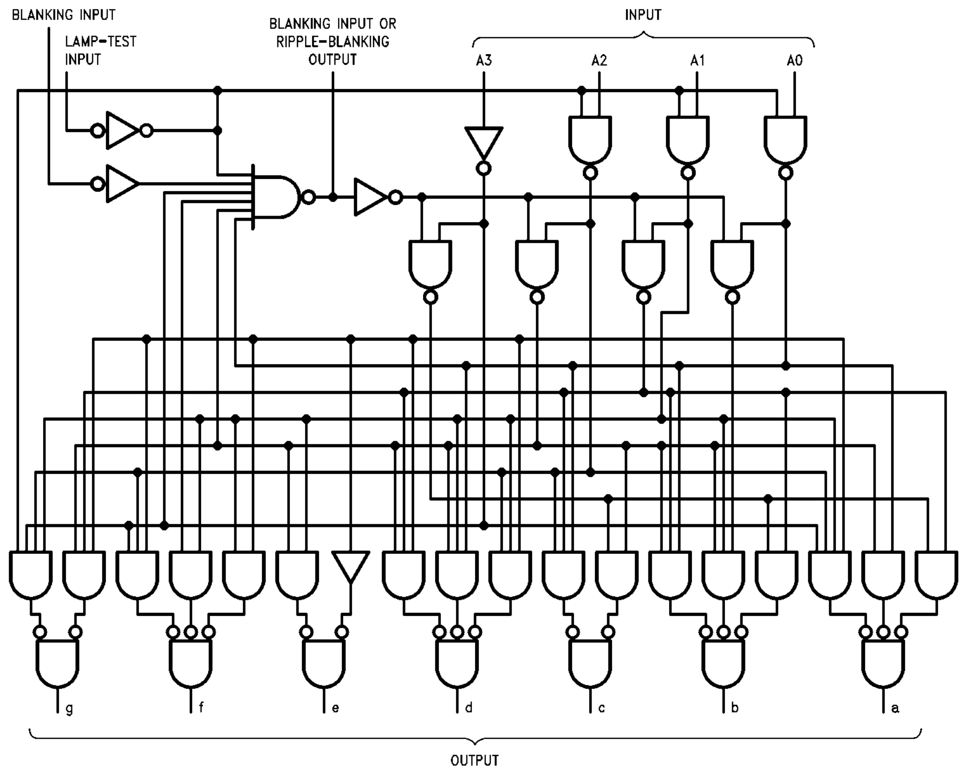
Decimal or Function	Inputs $\overline{LT}$	A_3	A_2	A_1	A_0	$\overline{BI/RBO}$	Outputs a	b	c	d	e	f	g	Note
0	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	H	L	L	L	L	L	L	L	
$\overline{BI}$	X	X	X	X	X	L	L	L	L	L	L	L	L	2
$\overline{LT}$	L	X	X	X	X	H	H	H	H	H	H	H	H	3

Note 1: $\overline{BI/RBO}$ is wired-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired. X = input may be HIGH or LOW.

Note 2: When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level, regardless of the state of any other input condition.

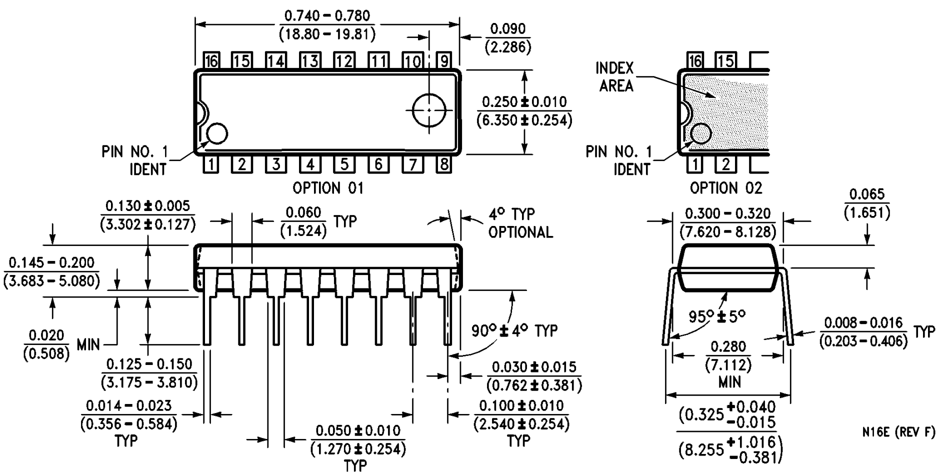
Note 3: When the blanking input/ripple-blanking output ($\overline{BI/RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a HIGH level.

Logic Diagram



TL/F/10213-4

Physical Dimensions inches (millimeters)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS249N
NS Package Number N16E

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS251
3-STATE Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled 3-STATE output. The strobe must be at a low logic level to enable these devices. The 3-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

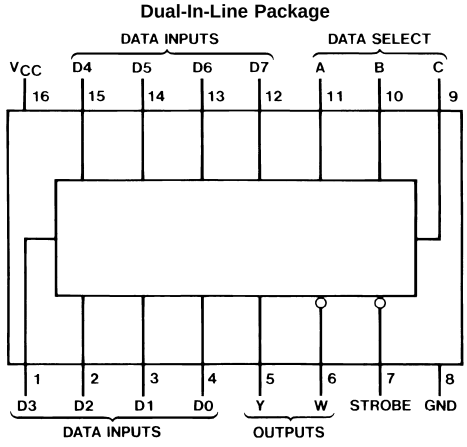
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- 3-STATE version of LS151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Maximum number of common outputs
  54LS 49
  74LS 129
- Typical propagation delay time (D to Y)
  54LS 17 ns
  74LS 17 ns
- Typical power dissipation
  54LS 35 mW
  74LS 35 mW

Connection Diagram

Dual-In-Line Package



Order Number DM54LS251J, DM54LS251W, DM74LS251M or DM74LS251N
See Package Number J16A, M16A, N16E or W16A

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level,
X = Don't Care, Z = High Impedance (Off)
D0, D1…D7 = The level of the respective D input

Absolute Maximum Ratings (Note 1)

Supply Voltage 7V

Input Voltage 7V

Operating Free Air Temperature Range

DM54LS −55°C to +125°C

DM74LS 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS251			DM74LS251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.4	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 4)			6.1	10	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 5)			7.1	12	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC1} is measured with the outputs open, STROBE grounded, and all other inputs at 4.5V.

Note 5: I_{CC2} is measured with the outputs open and all inputs at 4.5V.

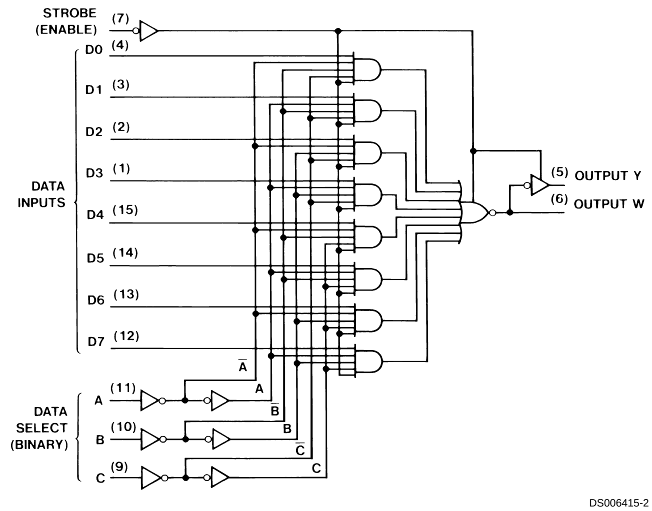
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

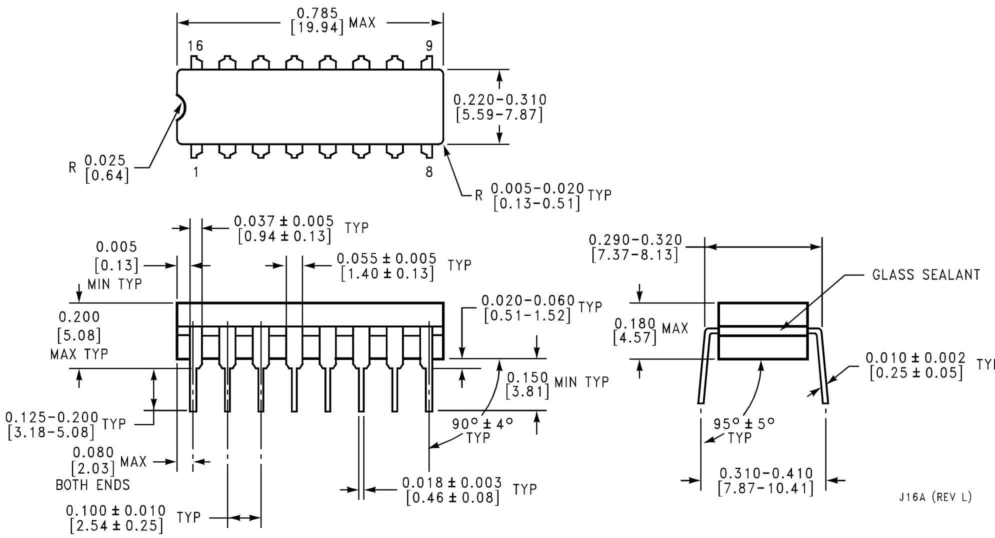
Symbol	Parameter	From (Input) to (Output)	R_L = 667Ω C_L = 45 pF Min	C_L = 45 pF Max	C_L = 150 pF Min	C_L = 150 pF Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W		33		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Y		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Y		28		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to W		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to W		15		25	ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to Y		45		60	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to Y		40		51	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)	Strobe to Y		45			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)	Strobe to Y		25			ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to W		27		40	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to W		40		47	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)	Strobe to W		55			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)	Strobe to W		25			ns

Note 6: C_L = 5 pF

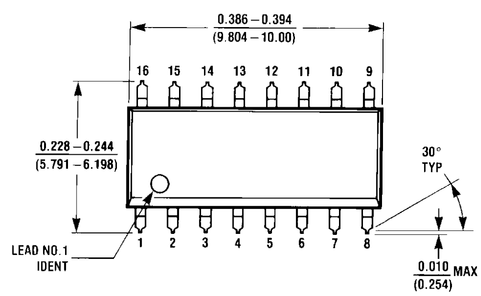
Logic Diagram

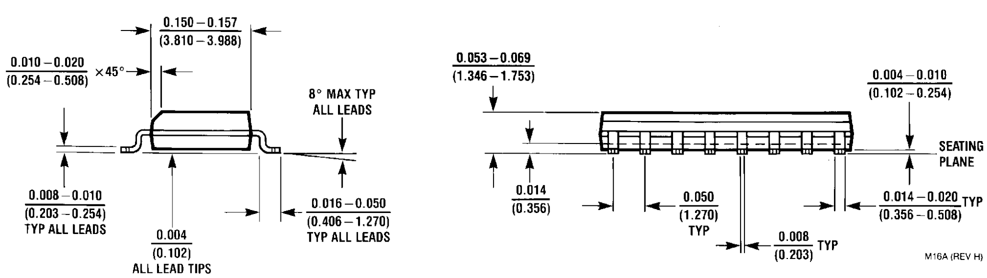


Physical Dimensions inches (millimeters) unless otherwise noted



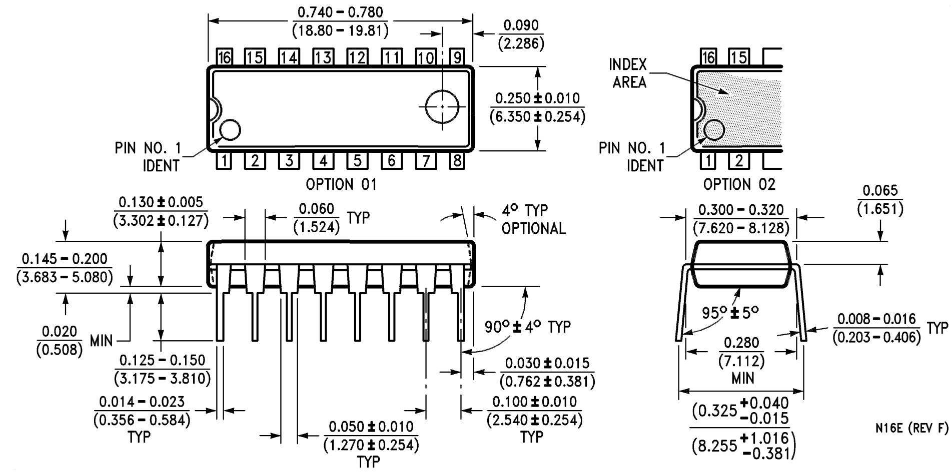
16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS251J
Package Number J16A



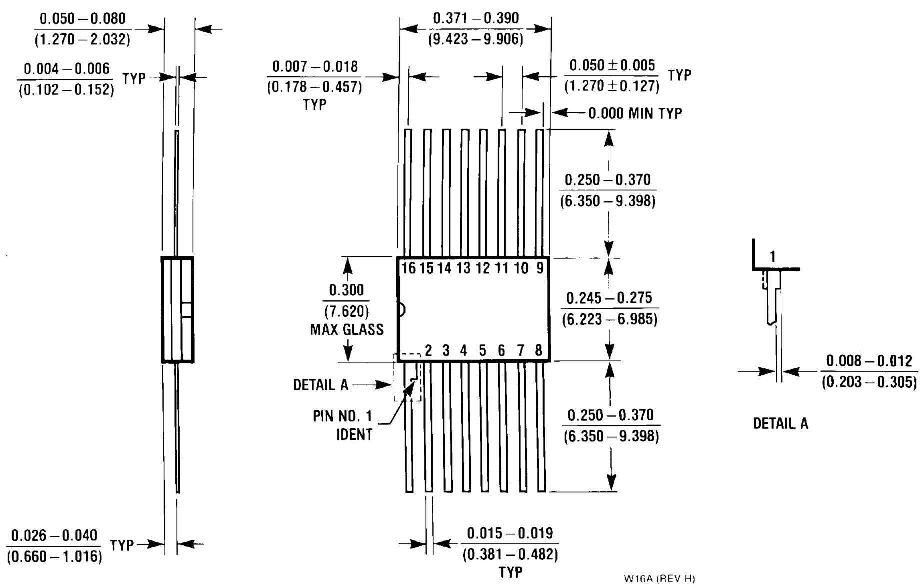


16-Lead Small Outline Molded Package (M)
Order Number DM74LS251M
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Molded Dual-In-Line Package (N)
Order Number DM74LS251N
Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS251W
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS253
3-STATE Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

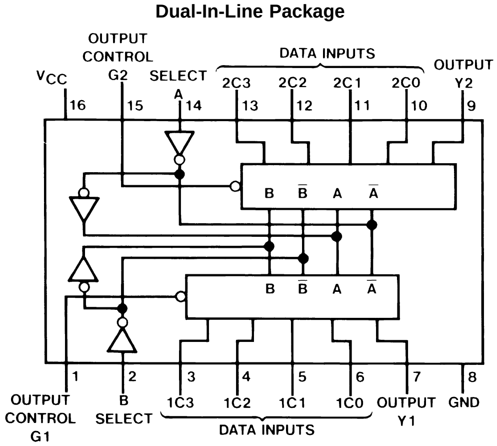
The 3-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- 3-STATE version of LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
  - Data to output 12 ns
  - Select to output 21 ns
- Typical power dissipation 35 mW
- Alternate Military/Aerospace device (54LS253) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006416-1

Order Number 54LS253DMQB, 54LS253FMQB, 54LS253LMQB, DM54LS253J, DM54LS253W, DM74LS253M or DM74LS253N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	**A**	**C0**	**C1**	**C2**	**C3**	**G**	**Y**
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (off).

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS253			DM74LS253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.4	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54			0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4 V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 4)			7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 5)			8.5	14	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC1} is measured with all outputs open, and all the inputs grounded.

Note 5: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

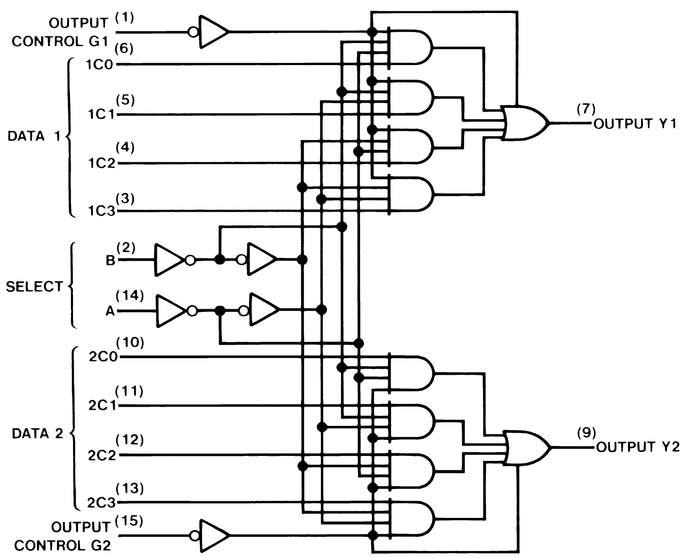
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		45		54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		32		44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		18		32	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		23		35	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)	Output Control to Y		41			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)	Output Control to Y		27			ns

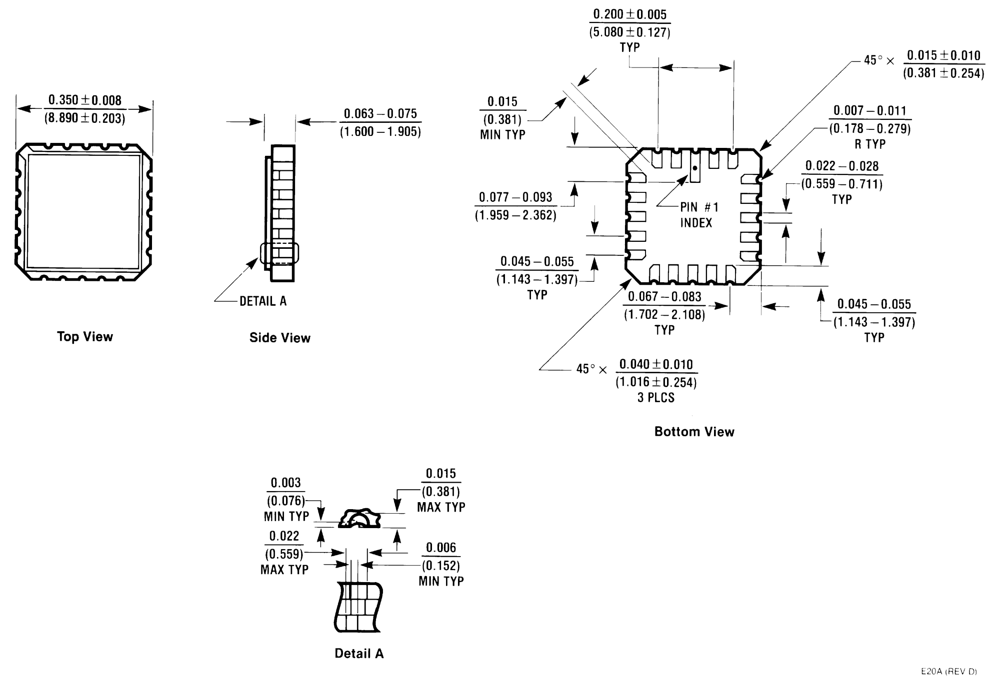
Note 6: C_L = 5 pF.

Logic Diagram

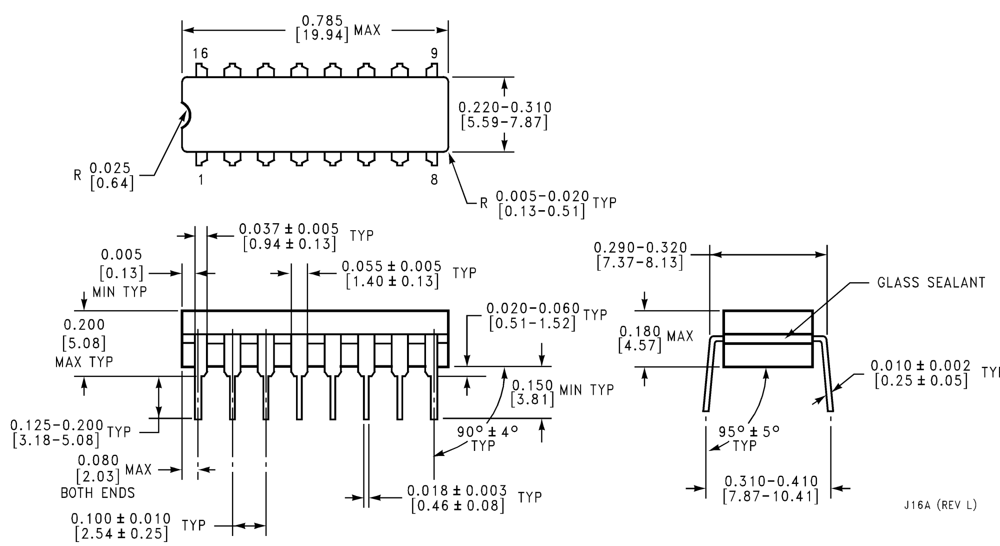


DS006416-2

Physical Dimensions inches (millimeters) unless otherwise noted

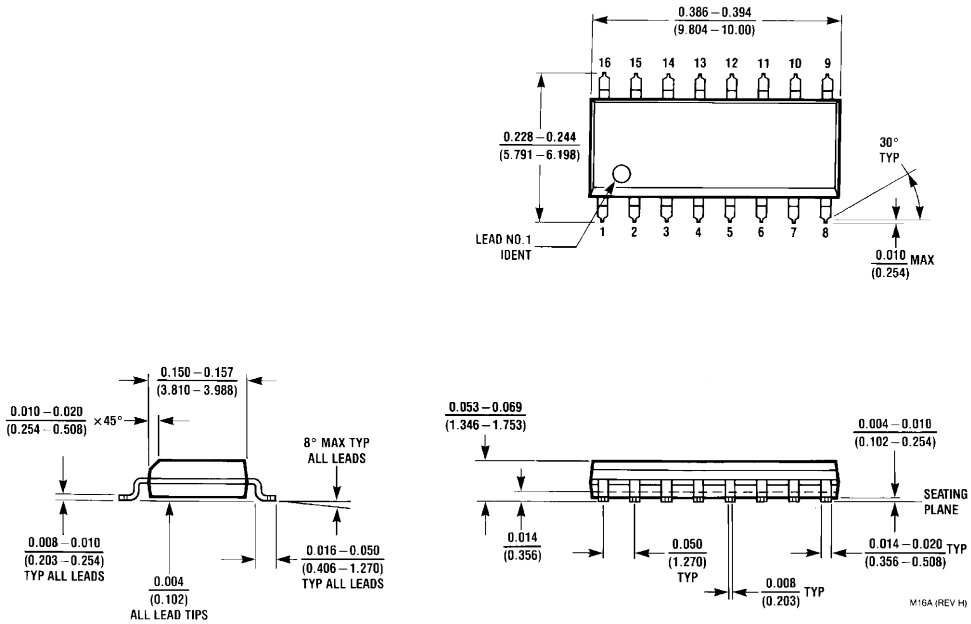


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS253LMQB
Package Number E20A

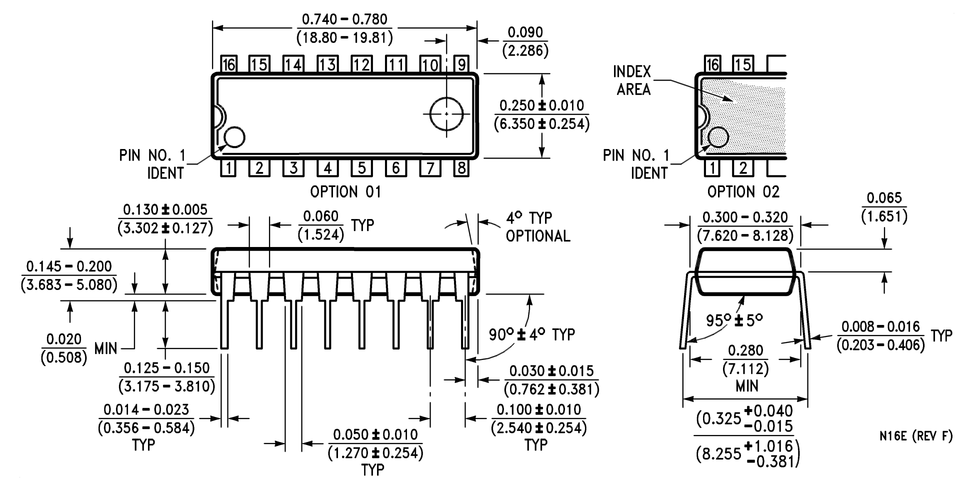


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS253DMQB or DM54LS253J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

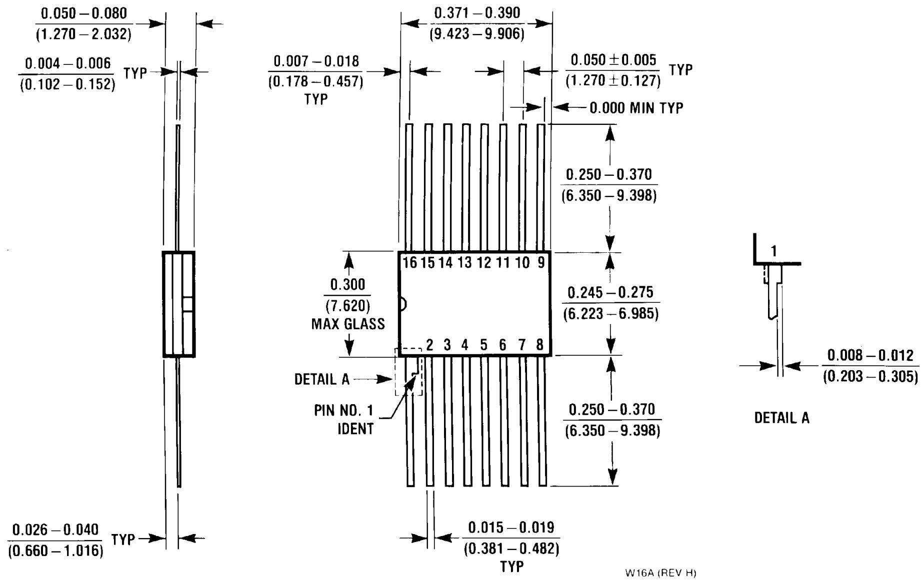


16-Lead Small Outline Molded Package (M)
Order Number DM74LS253M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS253N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS253FMQB or DM54LS253W
Package Number W16A

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National Semiconductor

June 1989

54LS256/DM74LS256 Dual 4-Bit Addressable Latch

General Description

The 'LS256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A0, A1), an active LOW enable input ($\overline{E}$) and an active LOW Clear input ($\overline{CL}$). Each latch has a Data input (D) and four outputs (Q0–Q3).

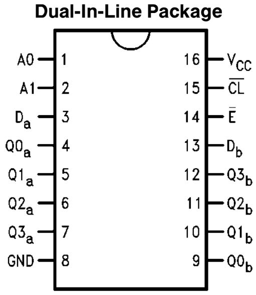
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q0–Q3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{CL}$ and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q0–Q3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{CL}$ = HIGH), changing more than one bit of the Address (A0, A1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{CL}$ = HIGH).

Features

- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Active low common clear

Connection Diagram

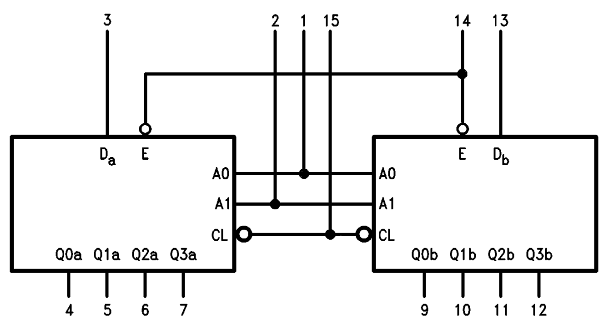
Dual-In-Line Package



TL/F/9823–1

Order Number 54LS256DMQB, 54LS256FMQB or DM74LS256N See NS Package Number J16A, N16E or W16A

Logic Symbol



TL/F/9823–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0, A1	Common Address Inputs
D_a, D_b	Data Inputs
$\overline{E}$	Common Enable Input (Active LOW)
$\overline{CL}$	Conditional Clear Input (Active LOW)
$Q0_a$–Q_3a	Side A Latch Outputs
$Q0_b$–Q_3b	Side B Latch Outputs

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Truth Table

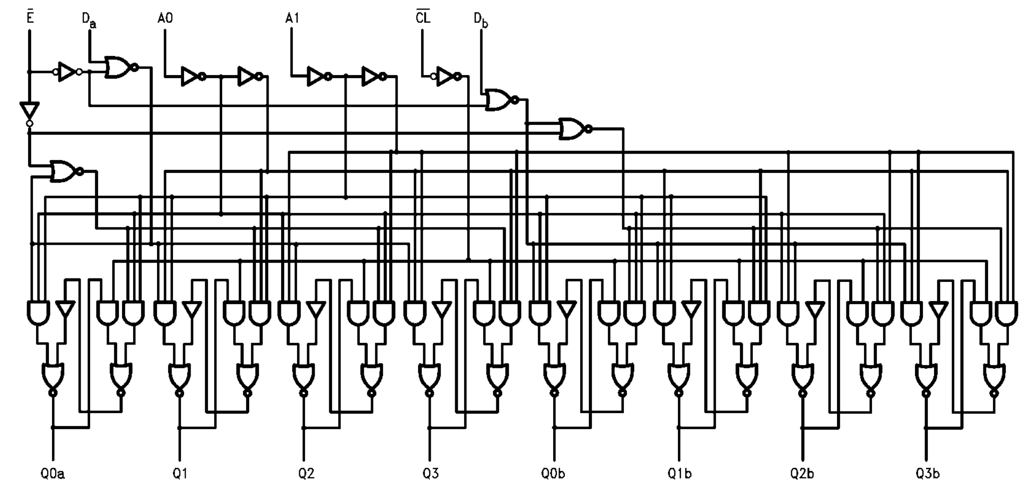
Inputs				Outputs				Mode
$\overline{CL}$	$\overline{E}$	A0	A1	Q0	Q1	Q2	Q3	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable Latch
H	L	H	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	
H	L	L	H	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	
H	L	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

$t-1$ = Bit time before address change or rising edge of E
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Mode Selection

$\overline{E}$	$\overline{CL}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

Logic Diagram



TL/F/9823-3

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS256			DM74LS256			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to $\overline{E}$	20			20			ns
t_h (H)	Hold Time HIGH, D_n to $\overline{E}$	0			0			ns
t_s (L)	Setup Time LOW, D_n to $\overline{E}$	15			15			ns
t_h (L)	Hold Time LOW, D_n to $\overline{E}$	0			0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW, A_n to $\overline{E}$	0			0			ns
t_w (L)	$\overline{E}$ Pulse Width LOW	17			17			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	Inputs			0.1	mA
			$\overline{E}$			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Inputs			20	μA
			$\overline{E}$			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Inputs			−0.4	mA
			$\overline{E}$			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

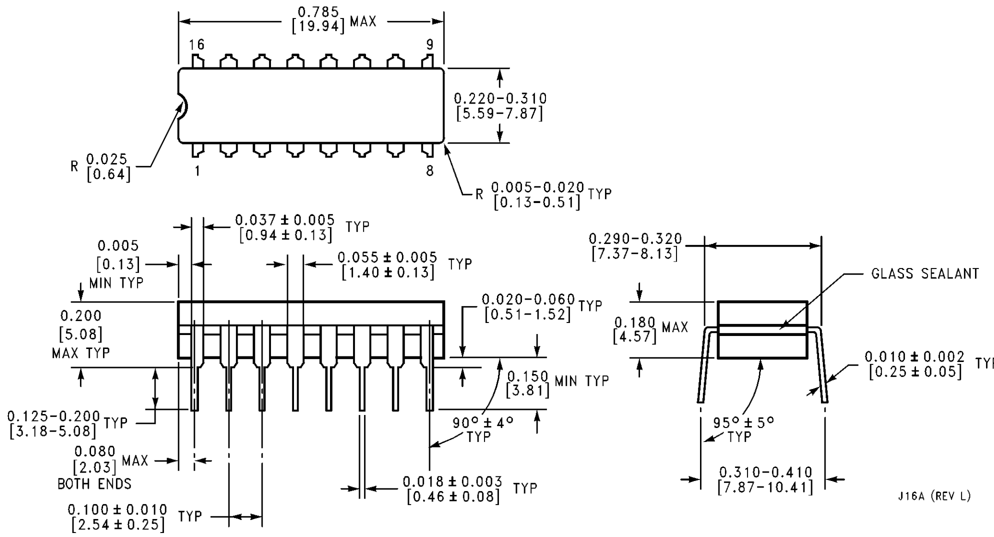
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

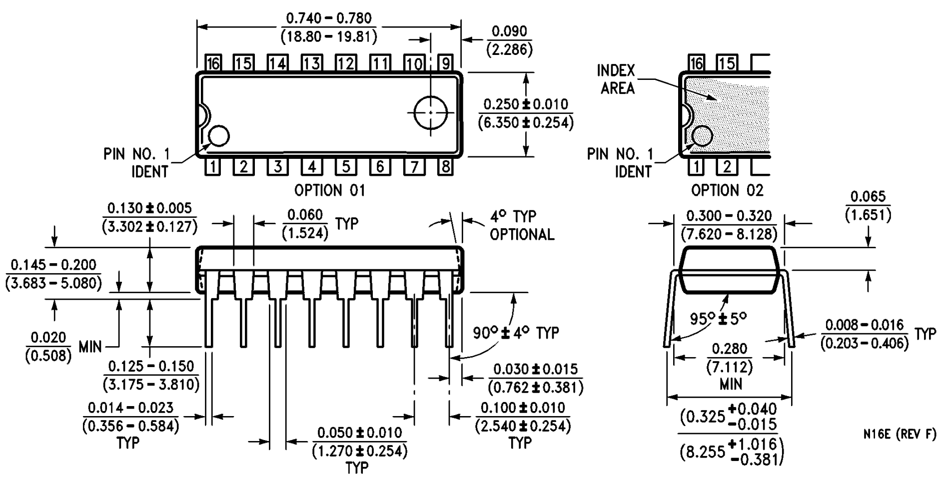
$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for waveforms and load configurations)

Symbol	Parameter	$R_L = 2\ k\Omega$ $C_L = 15\ pF$ Max	Units
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	27 24	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	30 20	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	30 29	ns
t_{PLH}	Propagation Delay $\overline{CL}$ to Q_n	18	ns

Physical Dimensions inches (millimeters)

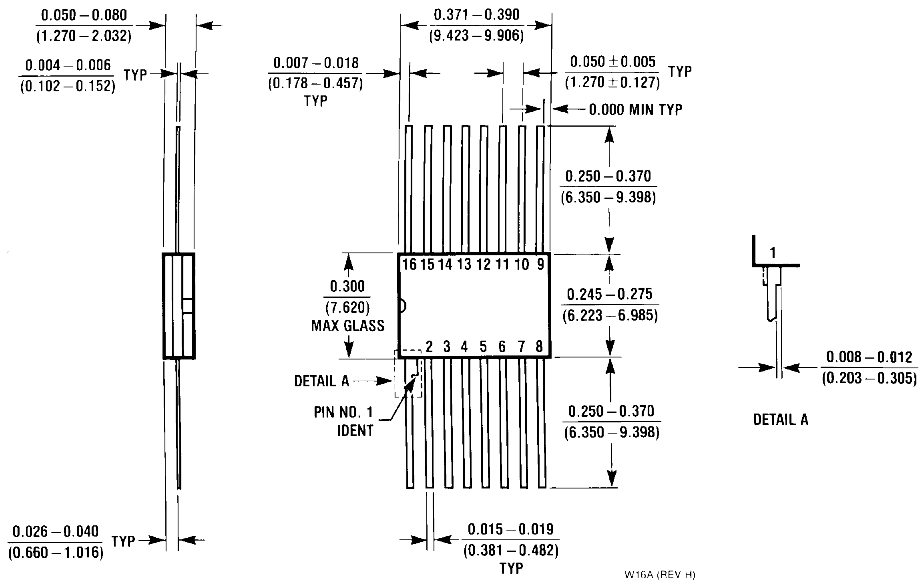


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS256DMQB
NS Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS256N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS256FMQB
NS Package Number W16A

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

June 1989

54LS257A/DM54LS257B/DM74LS257B, 54LS258A/DM54LS258B/DM74LS258B TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

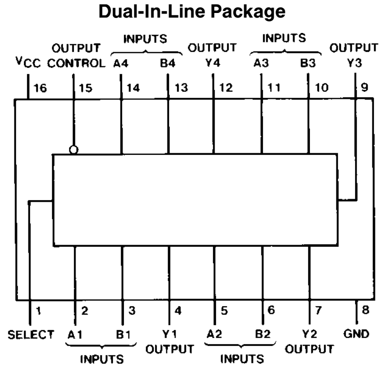
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions LS157 and LS158 with same pinouts
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input 12 ns
- Typical power dissipation
  LS257B 50 mW
  LS258B 35 mW
- Alternate military/aerospace devices (54LS257A/54LS258A) are available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagrams

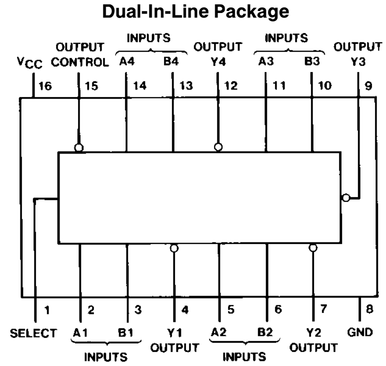
Dual-In-Line Package



TL/F/6417–1

Order Number 54LS257ADMQB, 54LS257AFMQB, 54LS257ALMQB, DM54LS257BJ, DM54LS257BW, DM74LS257BM or DM74LS257BN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Dual-In-Line Package



TL/F/6417–2

Order Number 54LS258ADMQB, 54LS258AFMQB, 54LS258ALMQB, DM54LS258BJ, DM54LS258BW, DM74LS258BM or DM74LS258BN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs				Output Y	
Output Control	Select	A	B	LS257	LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance (off)

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS257B			DM74LS257B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS257B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			5.9	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9.2	16	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS257B Switching Characteristics

at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 667\Omega$				Units
			$C_L = 45$ pF		$C_L = 150$ pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Y		25			ns

Note 1: $C_L = 5$ pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS258B			DM74LS258B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS258B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -18$ mA				−1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max $V_{IL} = $ Max, $V_{IH} = $ Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max $V_{IL} = $ Max, $V_{IH} = $ Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 12$ mA, $V_{CC} = $ Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 7V$	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.7V$	Select			40	μA
			Other			20	

'LS258B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			4.1	7	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9	14	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS258B Switching Characteristics

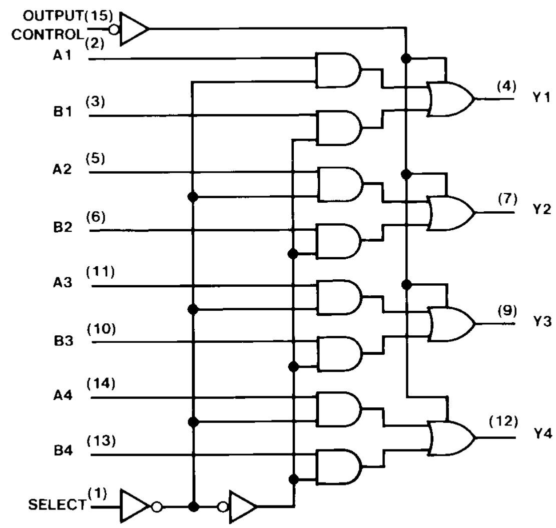
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)	Output Control to Y		25			ns

Note 4: C_L = 5 pF.

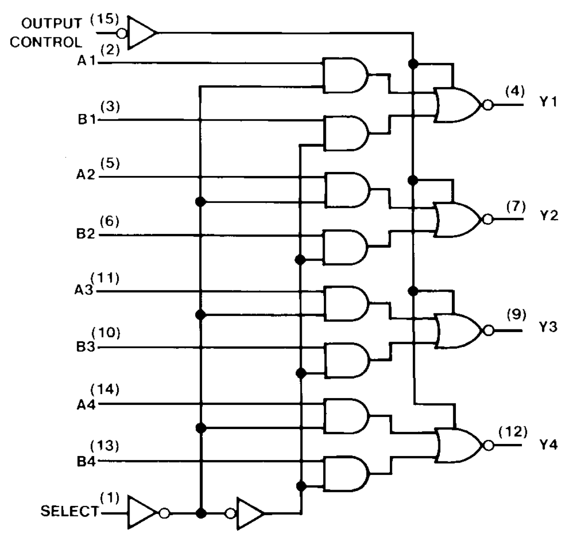
Logic Diagrams

LS257B



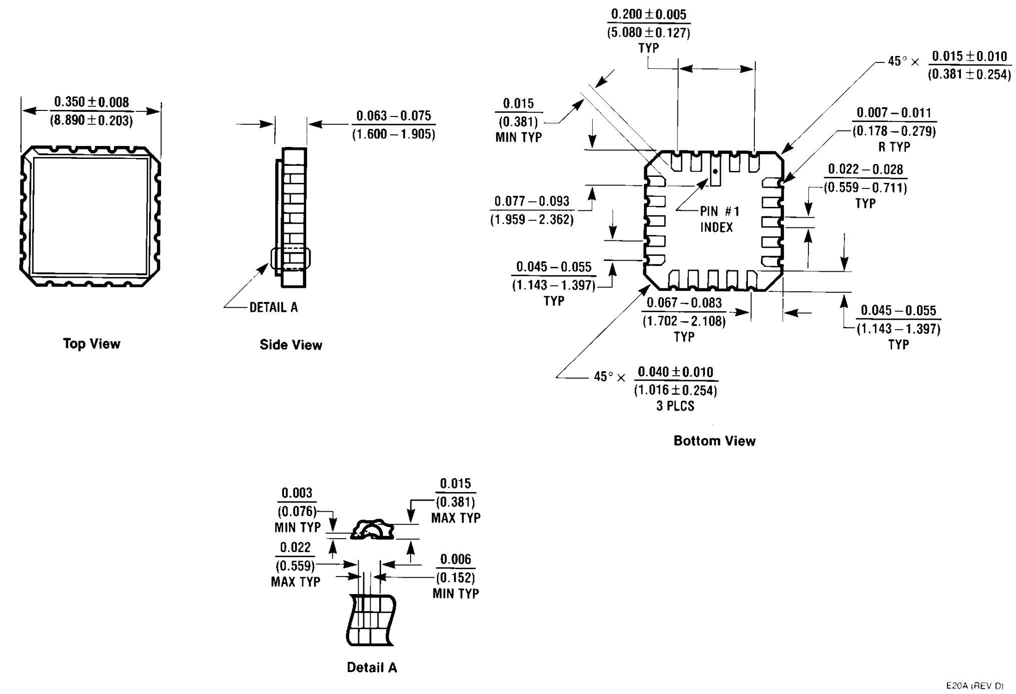
TL/F/6417–3

LS258B

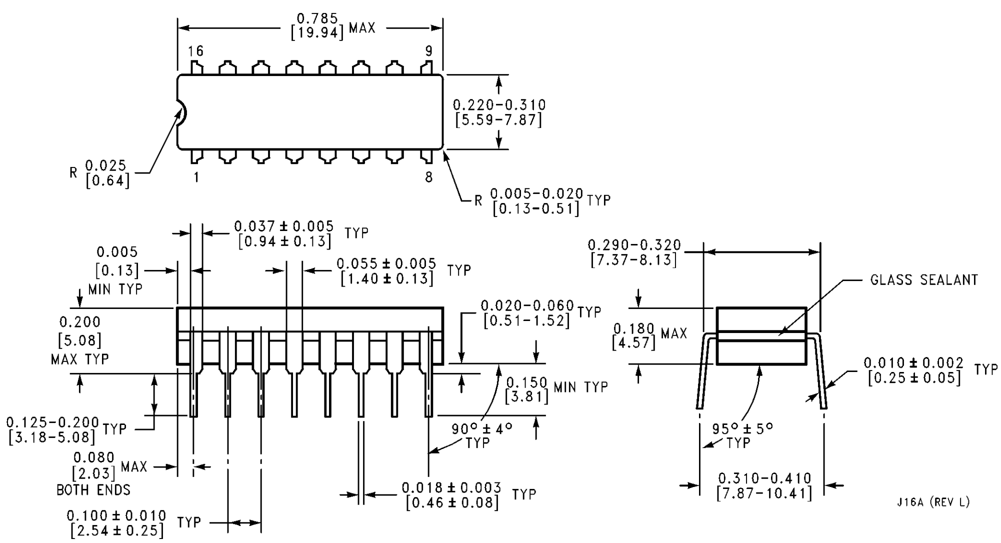


TL/F/6417–4

Physical Dimensions inches (millimeters)

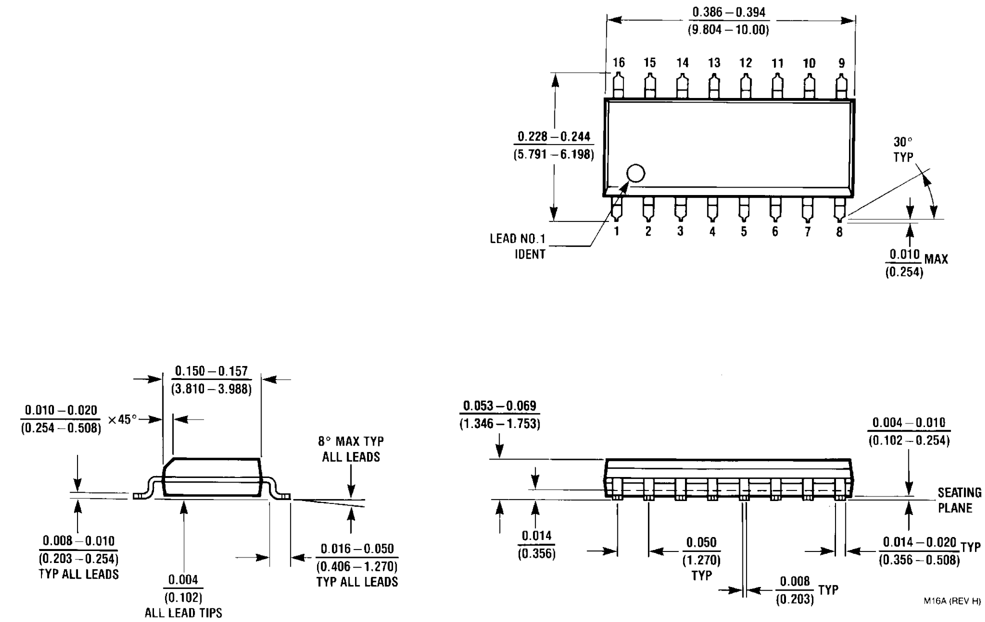


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS257ALMQB or 54LS258ALMQB
NS Package Number E20A

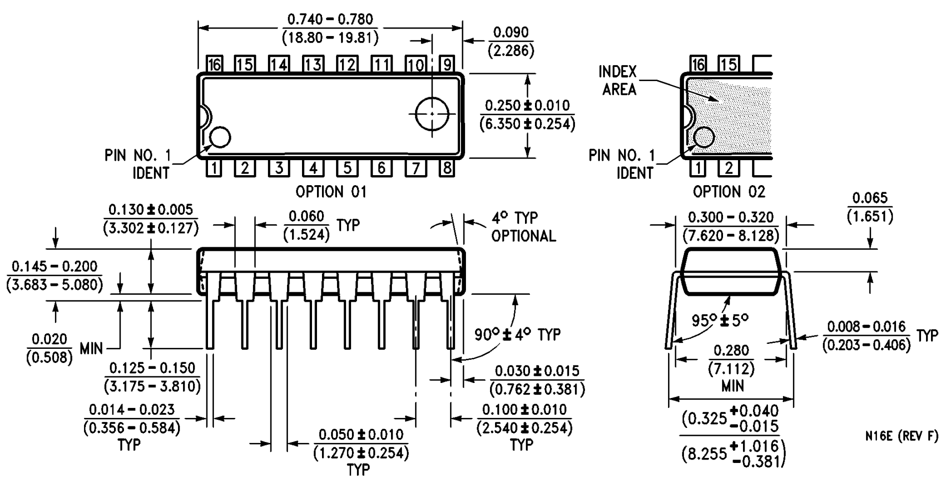


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS257ADMQB, 54LS258ADMQB, DM54LS257BJ or DM54LS258BJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

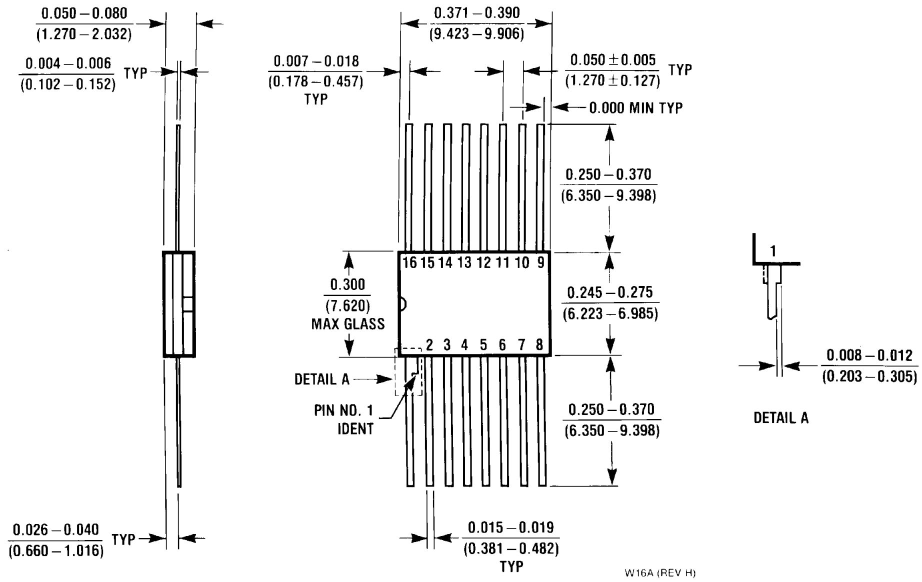


16-Lead Small Outline Molded Package (M)
Order Number DM74LS257BM or DM74LS258BM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS257BN or DM74LS258BN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS257AFMQB or 54LS258AFMQB
NS Package Number W16A

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FAIRCHILD SEMICONDUCTOR™

March 1998

DM74LS259
8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

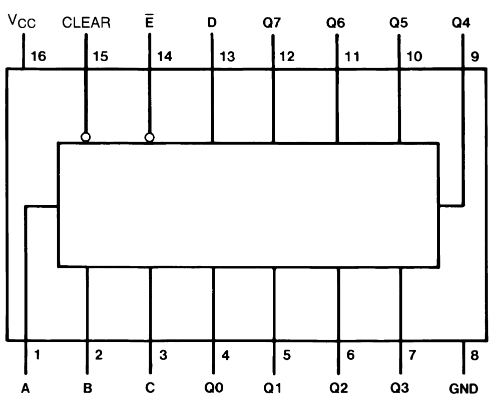
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
  - Enable-to-output 18 ns
  - Data-to-output 16 ns
  - Address-to-output 21 ns
  - Clear-to-output 17 ns
- Fan-out
  - I_{OL} (sink current)
    - 54LS259 4 mA
    - 74LS259 8 mA
  - I_{OH} (source current) −0.4 mA
- Typical I_{CC} 22 mA

Connection Diagram

Dual-In-Line Package



DS006418-1

Order Number DM54LS259E, DM54LS259J, DM54LS259W, DM74LS259M, DM74LS259WM or DM74LS259N
See Package Number E20A, J16A, M16A, M16B, N16E or W16A

Function Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level
D = the Level of the Data Input
Q_{i0} = the Level of Q_i (i = 0, 1,…7, as Appropriate) before the Indicated Steady-State Input Conditions Were Established.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter		DM54LS259			DM74LS259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width	Enable	17			15			ns
	(Note 8)	Clear	17			15			
t_{SU}	Setup Time	Data	20↑			15↑			ns
	(Notes 2, 3, 4, 8)	Select	15↓			15↓			
t_H	Hold Time	Data	5↑			2.5↑			ns
	(Notes 2, 3, 8)	Select	0↑			2.5↑			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5			V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54			0.4	V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
	Input Voltage	V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
	Enable	V_{CC} = Max, V_I = 0.4V				−0.8	
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current	(Note 6)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 7)			22	36	mA

Note 2: The symbols (↓, ↑) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 3: Setup and hold times are with reference to the enable input.

Note 4: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 7: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

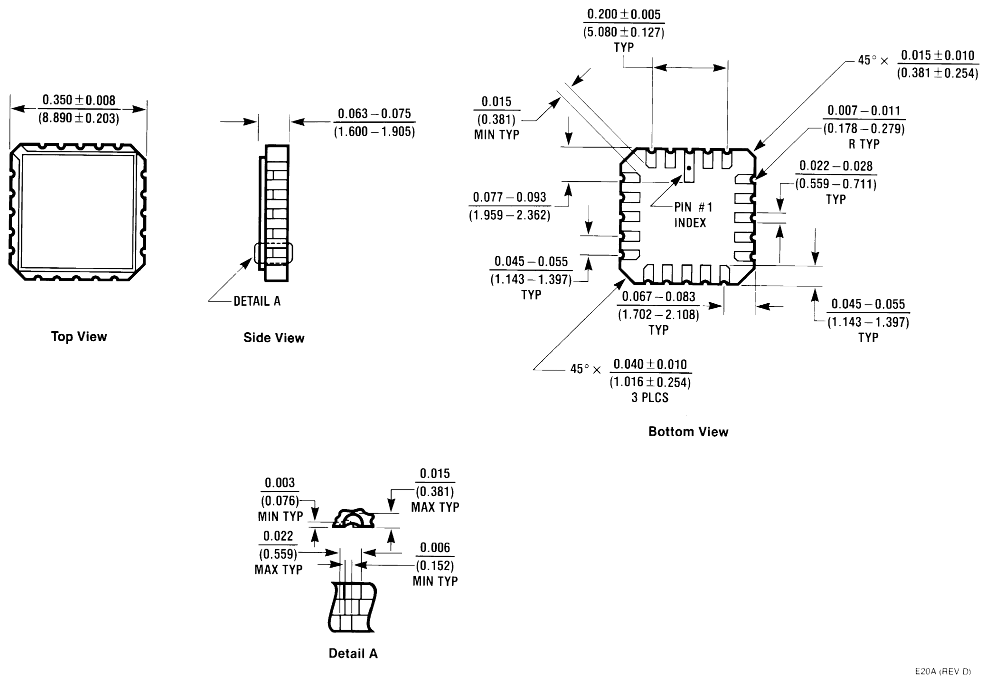
Note 8: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics

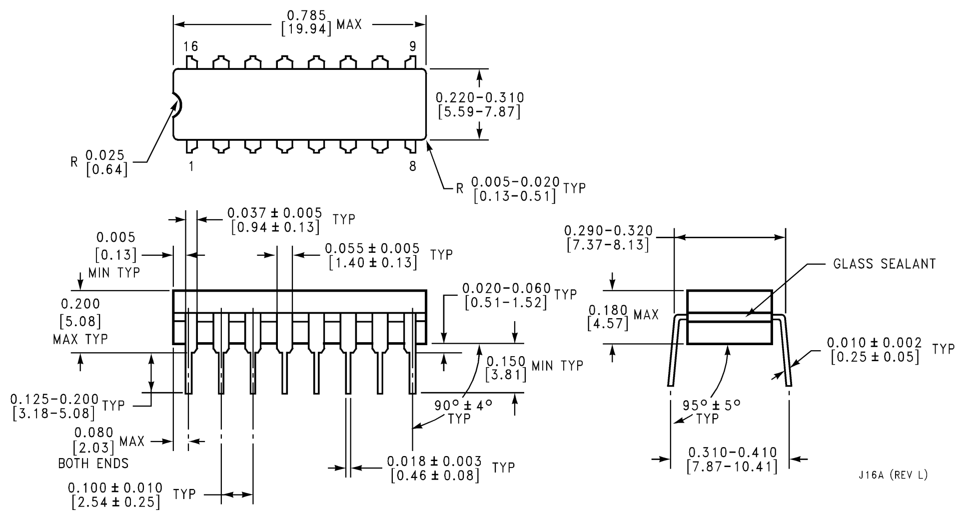
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	DM54LS C_L = 15 pF		DM74LS C_L = 50 pF R_L = 2 kΩ		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		27		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		30		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		29		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		18		36	ns

Physical Dimensions inches (millimeters) unless otherwise noted

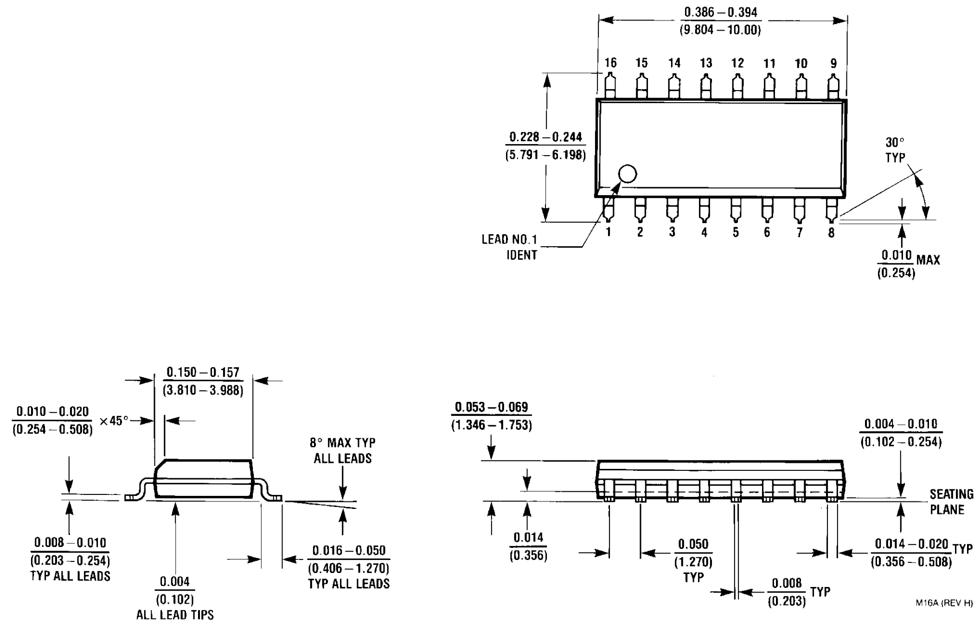


Ceramic Leadless Chip Carrier (E)
Order Number DM54LS259E
Package Number E20A



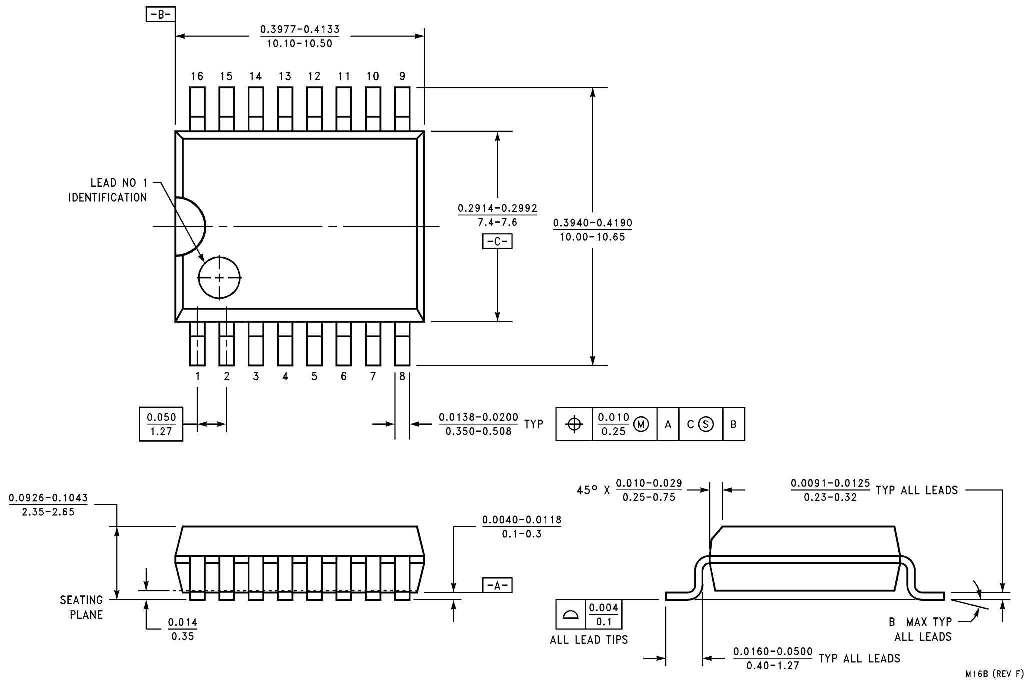
16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS259J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

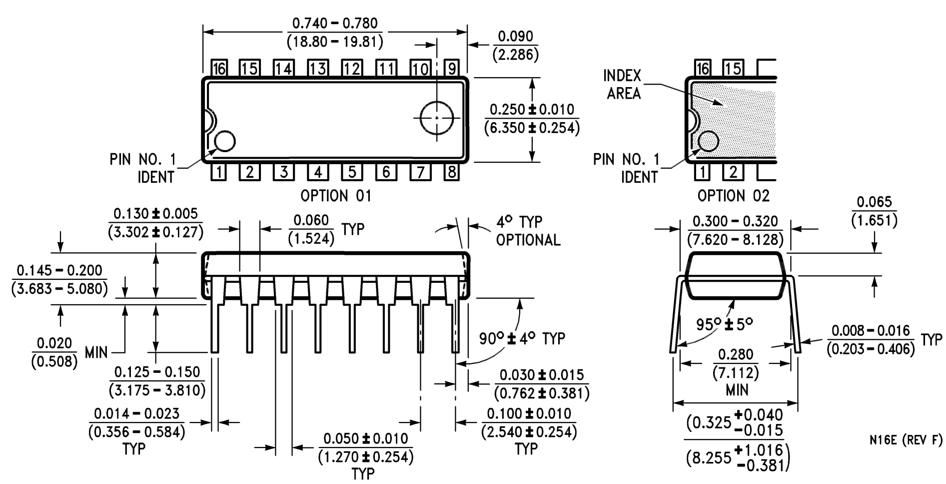


16-Lead Molded Package Small Outline (SO)
Order Number DM74LS259M
Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

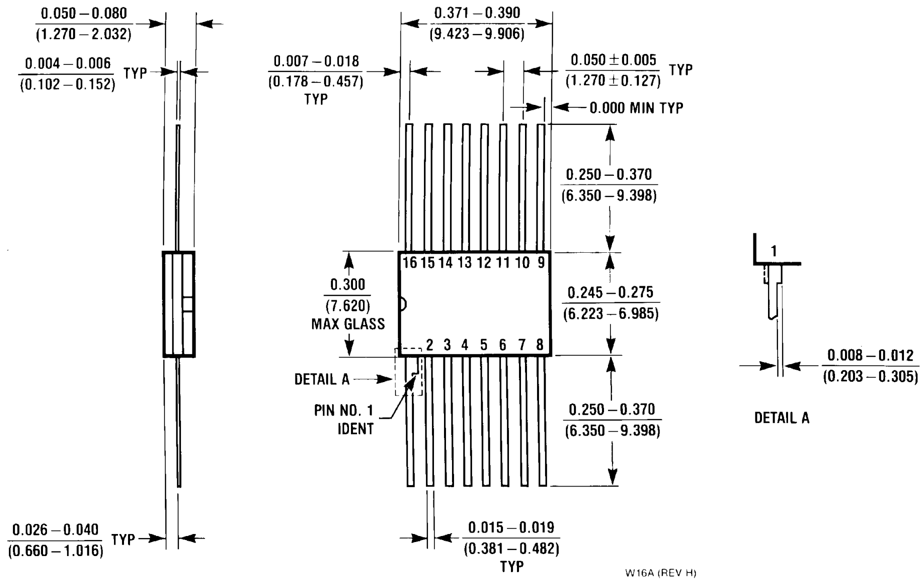


16-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS259WM
Package Number M16B



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS259N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS259W
Package Number W16A

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March 1998

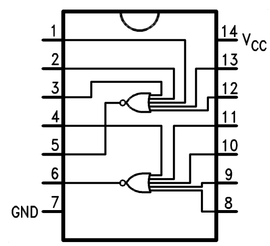
DM74LS260
Dual 5-Input NOR Gate

General Description

This device contains two individual five input gates, each of which perform the logic NOR function.

Connection Diagram

Dual-In-Line Package



DS009824-1

Order Number DM54LS260J, DM54LS260W, DN54LS260E, DM74LS260M or DM74LS260N
See Package Number E20A, J14A, M14A, N14A or W14B

Truth Table

$$\overline{A + B + C + D + E} = Y$$

Inputs					Outputs
A	**B**	**C**	**D**	**E**	**Y**
L	L	L	L	L	H
X	X	X	X	H	L
X	X	X	H	X	L
X	X	H	X	X	L
X	H	X	X	X	L
H	X	X	X	X	L

 DS009824

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS260			DM74LS260			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5			V
		V_{IL} = Max	DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54			0.4	V
		V_{IH} = Min	DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	DM54			−0.40	mA
			DM74			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 2)	DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max, V_{IN} = GND				4.0	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max, V_{IN} = Open				5.5	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

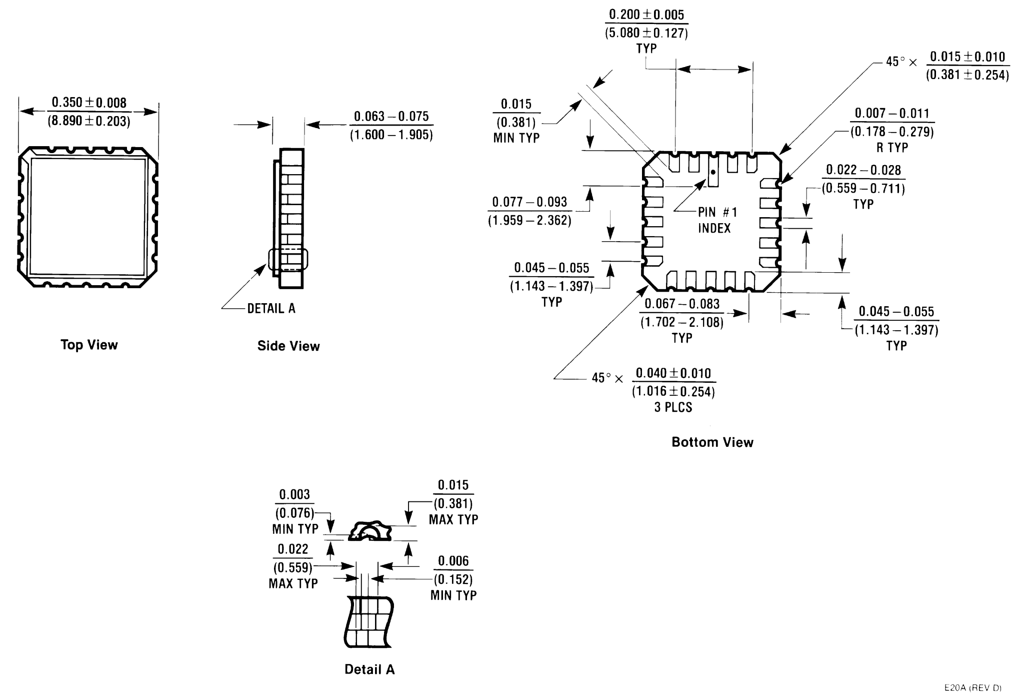
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5V, T_A = +25˚C

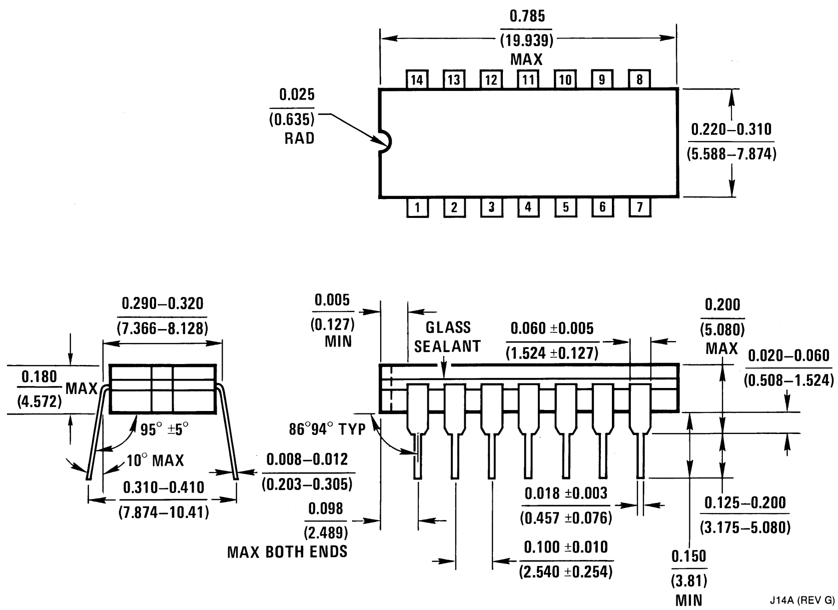
Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		12	ns

Physical Dimensions inches (millimeters) unless otherwise noted

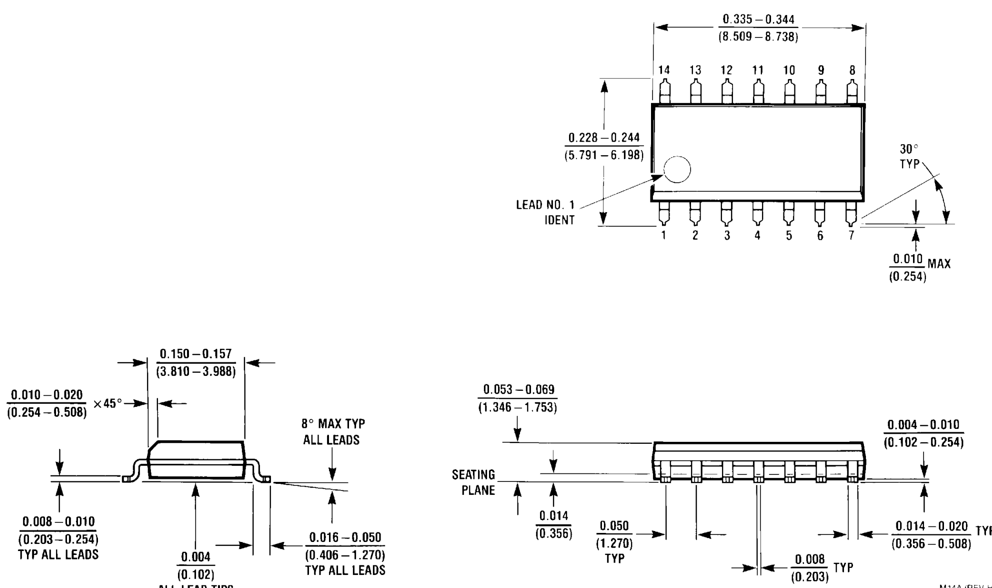


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS260E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

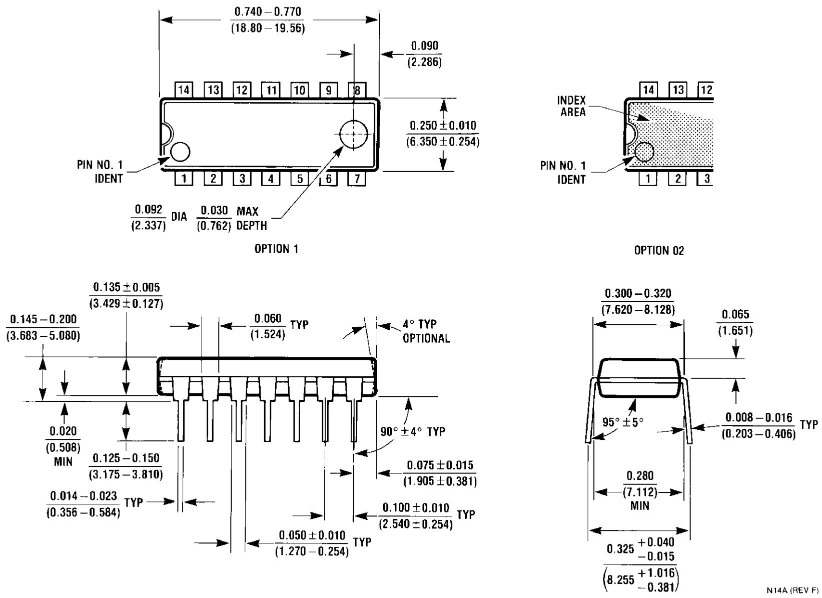


14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS260J
Package Number J14A

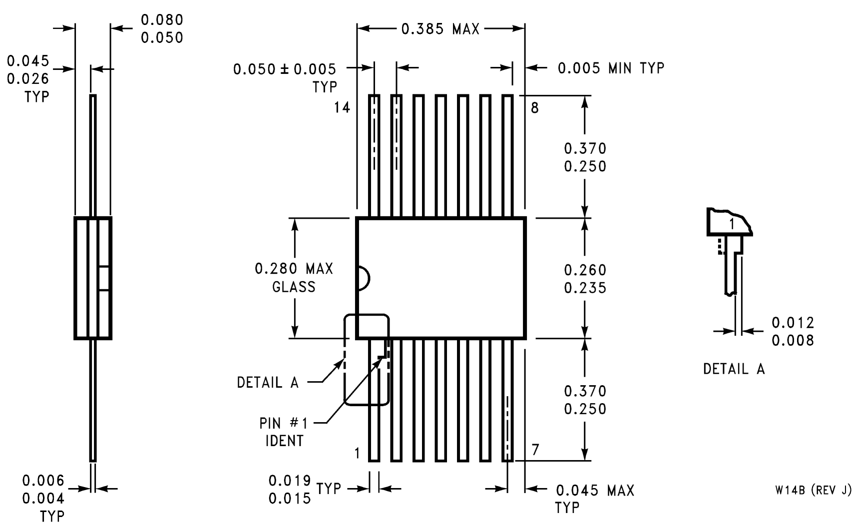


14-Lead Small Outline Molded Package (M)
Order Number DM74LS260M
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS260N
Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS260W
Package Number W14B

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April 1998

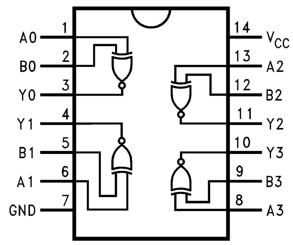
DM74LS266 Quad 2-Input Exclusive-NOR Gate with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic exclusive-NOR function. Outputs are open collector.

Connection Diagram

Dual-In-Line Package



Order Number DM74LS266M or DM74LS266N
See Package Number M14A or N14A

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
V_{OH}	High Level Output Voltage			5.5	V
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	˚C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max			13	mA

Switching Characteristics

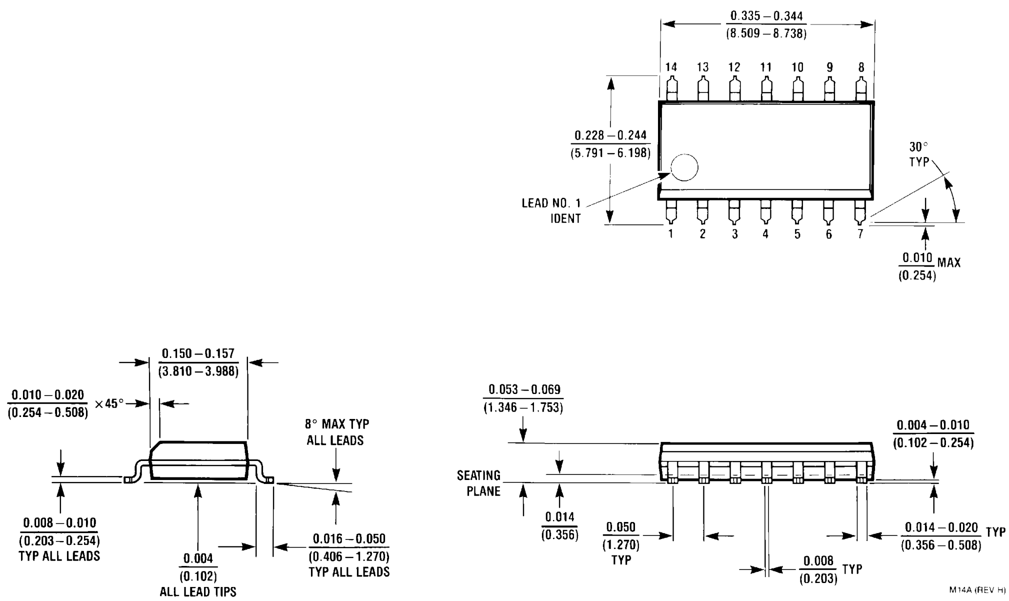
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		23	ns

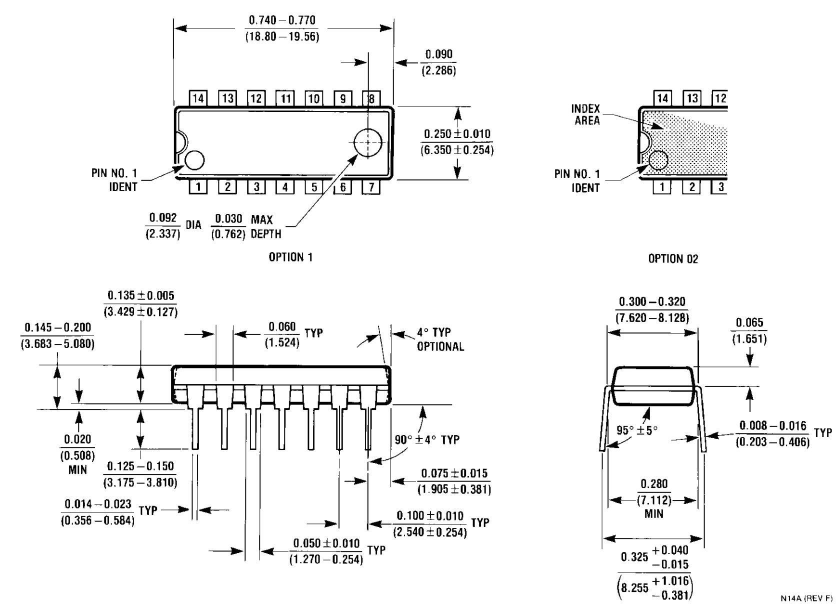
Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Molded Package (M)
Order Number DM74LS266M
Package Number M14A



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS266N
Package Number N14A

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March 1998

DM74LS273
8-Bit Register with Clear

General Description

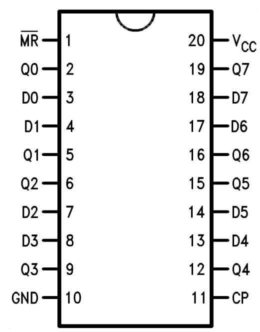
The 'LS273 is a high speed 8-bit register, consisting of eight D-type flip-flops with a common Clock and an asynchronous active LOW Master Reset. This device is supplied in a 20-pin package featuring 0.3 inch row spacing.

Features

- Edge-triggered
- 8-bit high speed register
- Parallel in and out
- Common clock and master reset

Connection Diagram

Dual-In-Line Package



DS009825-1

Order Number DM54LS273E, DM54LS273J, DM54LS273W, DM74LS273M or DM74LS273N
See Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D0–D7	Data Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
Q0–Q7	Flip-Flop Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS273			DM74LS273			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW D_n to CP	15 15			15 15			ns
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW D_n to CP	5 5			5 5			ns
$t_w(H)$ $t_w(L)$	CP Pulse Width HIGH or LOW	20 20			20 20			ns
$t_w(L)$	$\overline{MR}$ Pulse Width LOW	20			20			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			15			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max,	DM54	2.5			V
		V_{IL} = Max	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max,	DM54			0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (DM54)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				27	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A =+25˚C

Symbol	Parameter	C_L = 15 pF				Units
		DM54LS		DM74LS		
				R_L = 2 kΩ		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	30		30		MHz
t_{PLH}	Propagation Delay		24		24	ns
t_{PHL}	CP to Q_n		24		24	
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n		27		27	ns

Functional Description

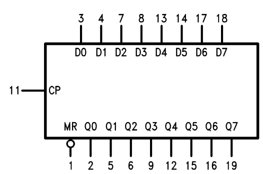
The 'LS273 is an 8-bit parallel register with a common Clock and common Master Reset. When the $\overline{MR}$ input is LOW, the Q outputs are LOW, independent of the other inputs. Information meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

Truth Table

Inputs			Outputs
MR	CP	D_n	Q_n
L	X	X	L
H	↑	H	H
H	↑	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

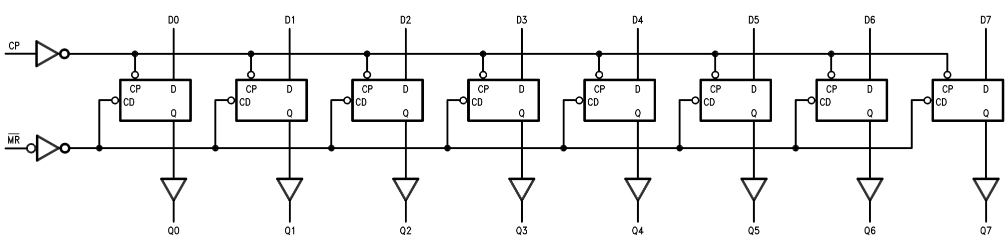
Logic Symbol



DS009825-2

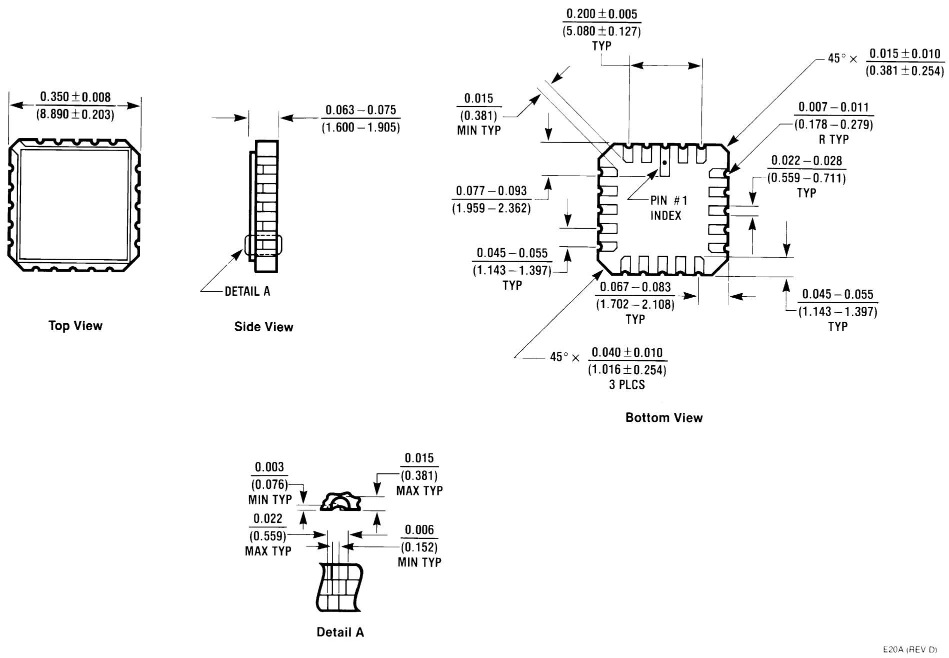
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram

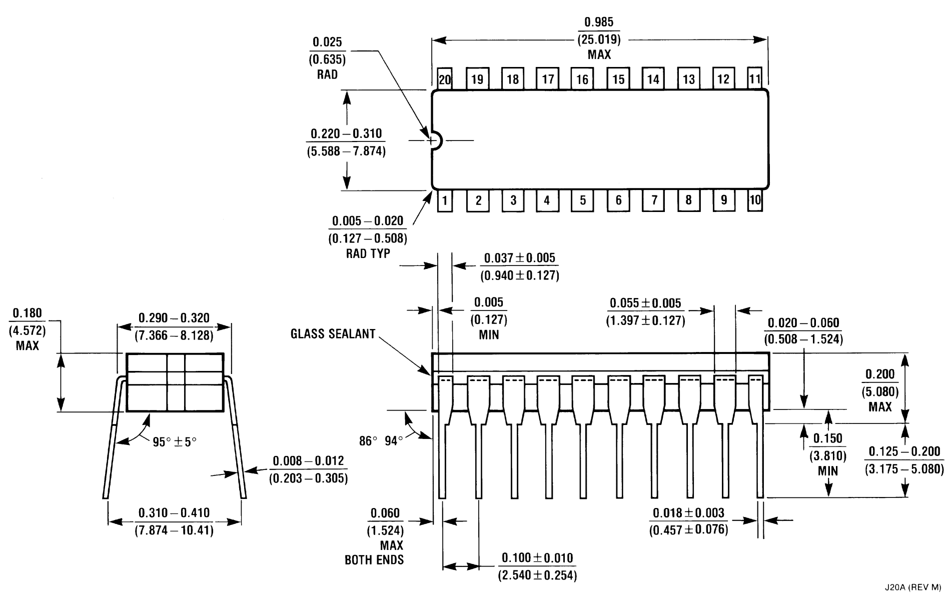


DS009825-3

Physical Dimensions inches (millimeters) unless otherwise noted

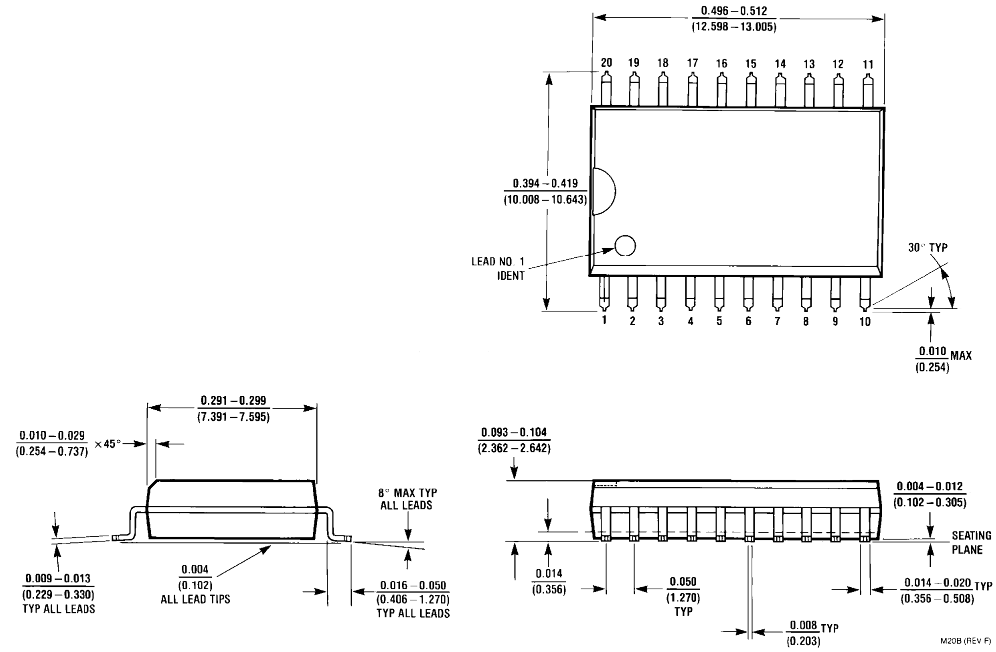


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS273E
Package Number E20A

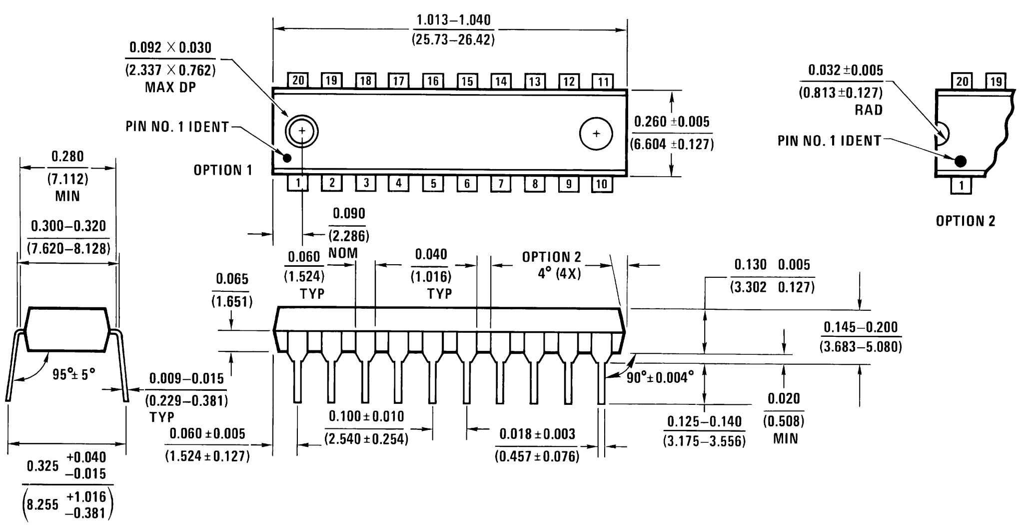


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS273J
Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

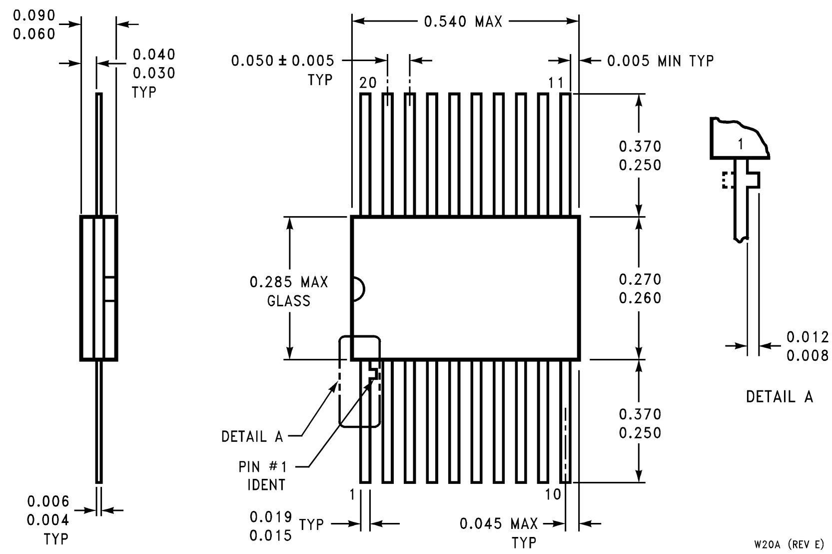


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS273M
Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS273N
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS273W
Package Number W20A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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March 1998

DM74LS279 Quad $\overline{S}$ -$\overline{R}$ Latches

General Description

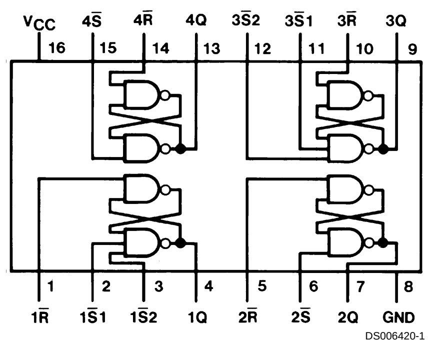
The 'LS279 consists of four individual and independent Set-Reset Latches with active low inputs. Two of the four latches have an additonal $\overline{S}$ input ANDed with the primary $\overline{S}$ input. A low on any $\overline{S}$ input while the $\overline{R}$ input is high will be stored in the latch and appear on the corresponding Q output as a high. A low on the $\overline{R}$ input while the $\overline{S}$ input is high will clear the Q output to a low. Simultaneous transistion of the $\overline{R}$ and $\overline{S}$ inputs from low to high will cause the Q output to be indeterminate. Both inputs are voltage level triggered and are not affected by transition time of the input data.

Features

- Alternate military/aerospace device (54LS279) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS279DMQB, 54LS279FMQB, 54LS279LMQB, DM54LS279J, DM74LS279M or DM74LS279N
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Inputs		Output
$\overline{S}$ (Note 2)	$\overline{R}$	Q
L	L	H (Note 1)
L	H	H
H	L	L
H	H	Q_0

H = High Level
L = Low Level
Q_0 = The Level of Q before the indicated input conditions were established.

Note 1: This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.

Note 2: For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

Absolute Maximum Ratings (Note 3)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS279			DM74LS279			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 3: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.5		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			3.8	7	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V and all outputs open.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

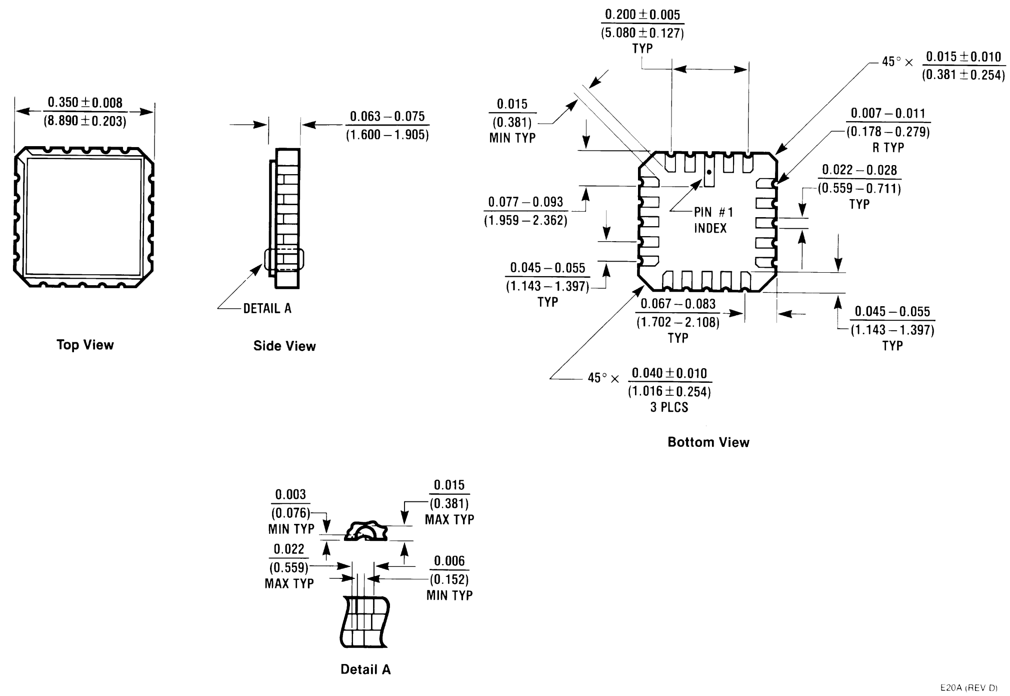
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{S}$ to Q		22		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{S}$ to Q		15		23	ns

Switching Characteristics (Continued)

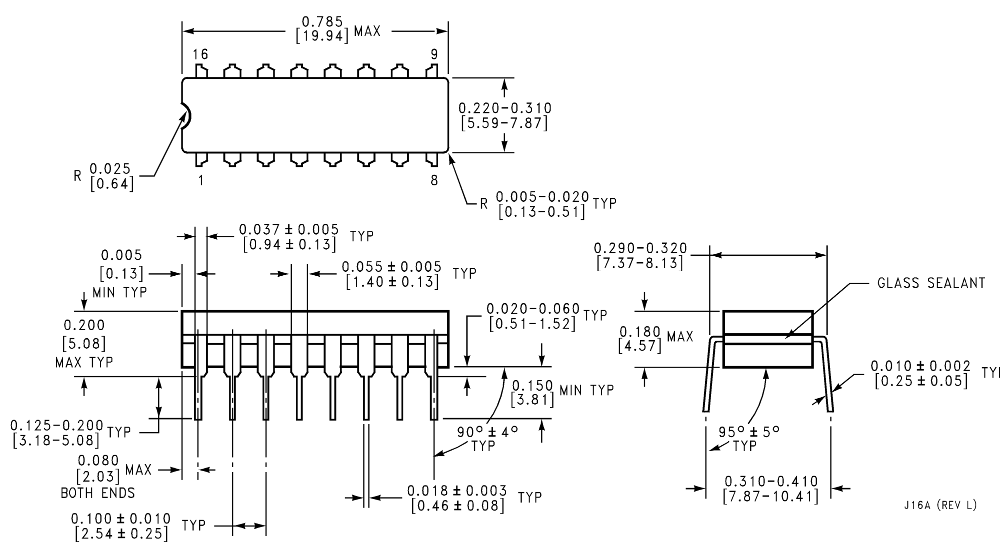
at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{R}$ to Q		27		33	ns

Physical Dimensions inches (millimeters) unless otherwise noted

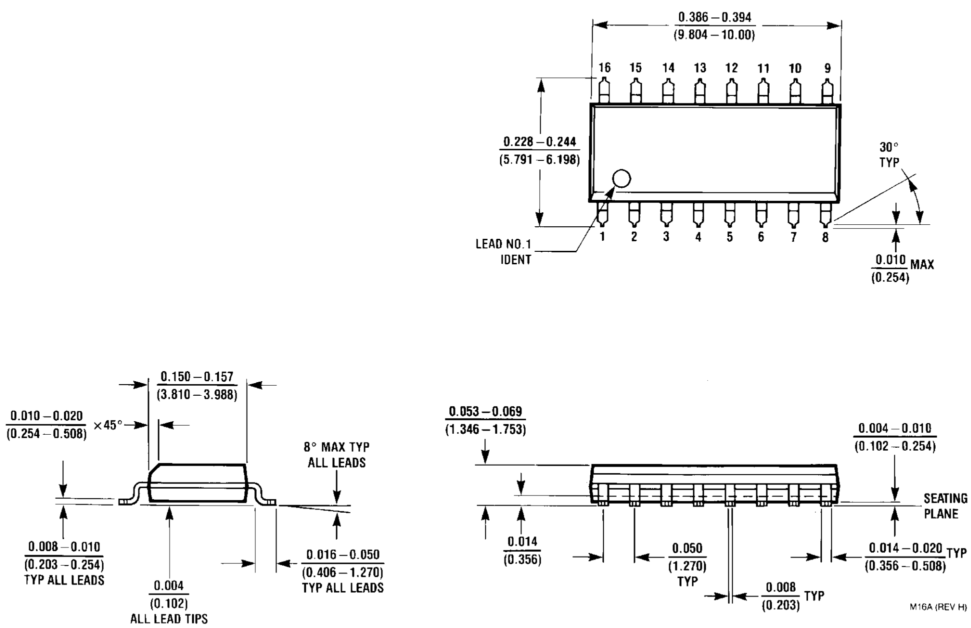


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS279LMQB
Package Number E20A

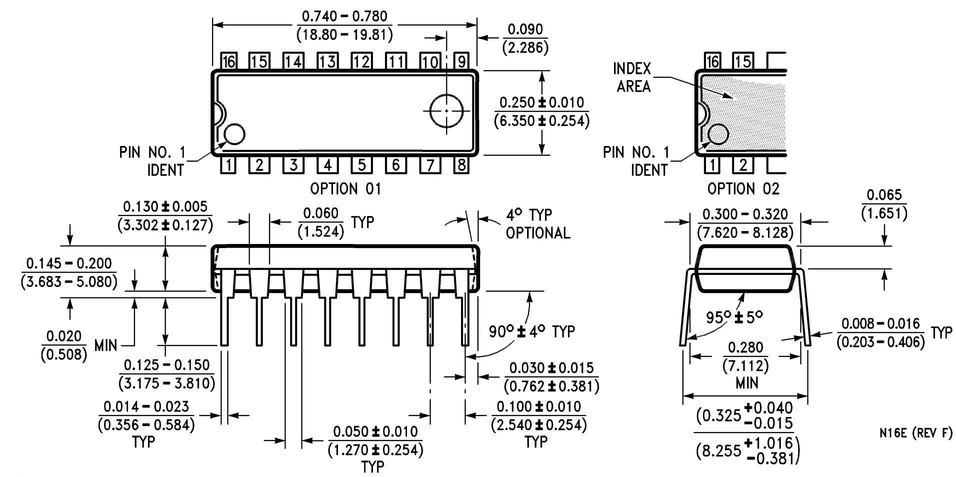


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS279DMQB or DM54LS279J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

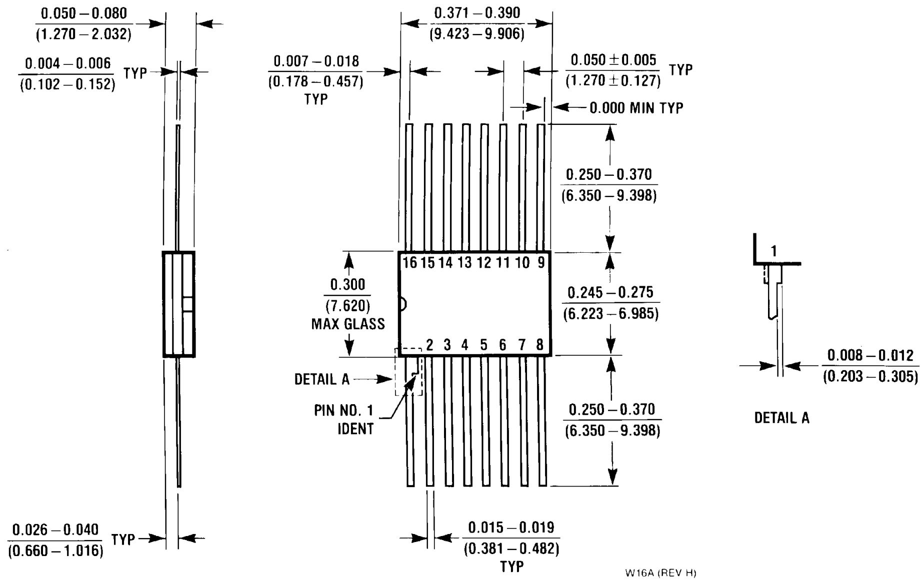


16-Lead Small Outline Molded Package (M)
Order Number DM74LS279M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS279N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS279FMQB or DM54LS279W
Package Number W16A

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March 1998

DM74LS283
4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

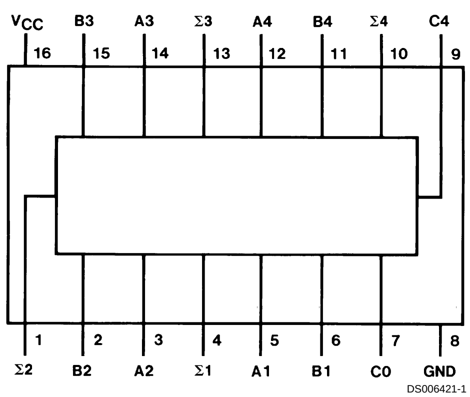
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW
- Alternate Military/Aerospace device (54LS283) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



Order Number 54LS283DMQB, 54LS283FMQB, 54LS283LMQB, DM54LS283J, DM54LS283W, DM74LS283M or DM74LS283N
See Package Number E20A, J16A, M16A, N16E or W16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS283			DM74LS283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
	Voltage	V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max	V_{CC} = Max	A, B			0.2	mA
	Input Voltage	V_I = 7V	C0			0.1	
I_{IH}	High Level Input	V_{CC} = Max	A, B			40	µA
	Current	V_I = 2.7V	C0			20	
I_{IL}	Low Level Input	V_{CC} = Max	A, B			−0.8	mA
	Current	V_I = 0.4V	C0			−0.4	
I_{OS}	Short Circuit	V_{CC} = Max	DM54	−20		−100	mA
	Output Current		DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 4)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 5)			22	39	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 5: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 1$, $\Sigma 2$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 1$, $\Sigma 2$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 3$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 3$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to $\Sigma 4$		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to $\Sigma 4$		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to C4		17		26	ns

Function Table

Input				Outputs					
				When C0 = L / When C2 = L			When C0 = H / When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

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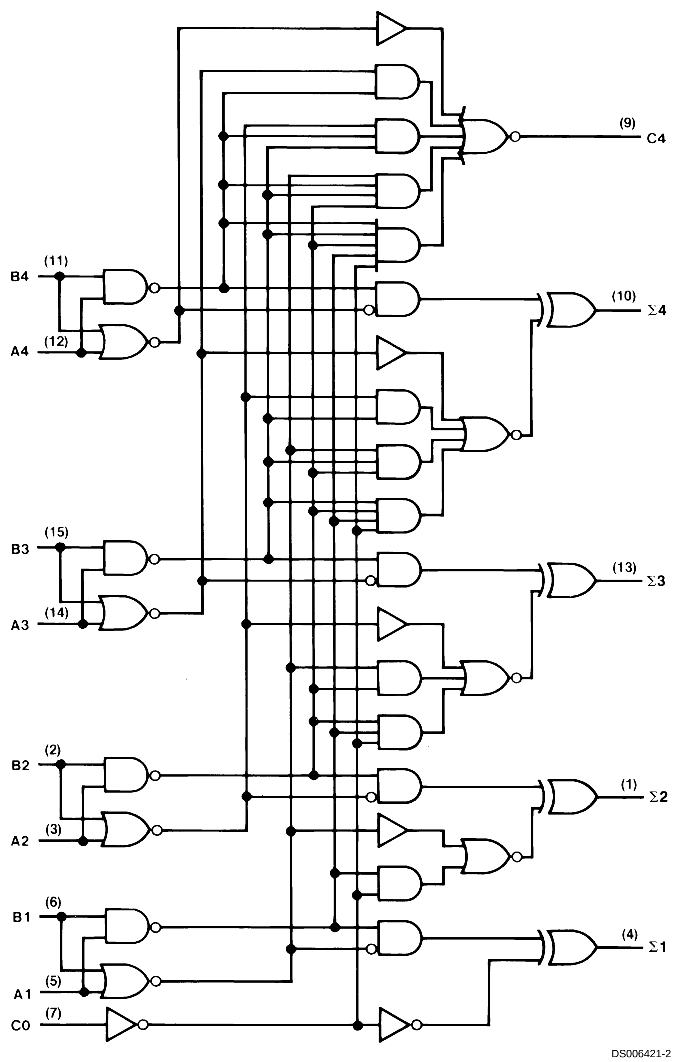
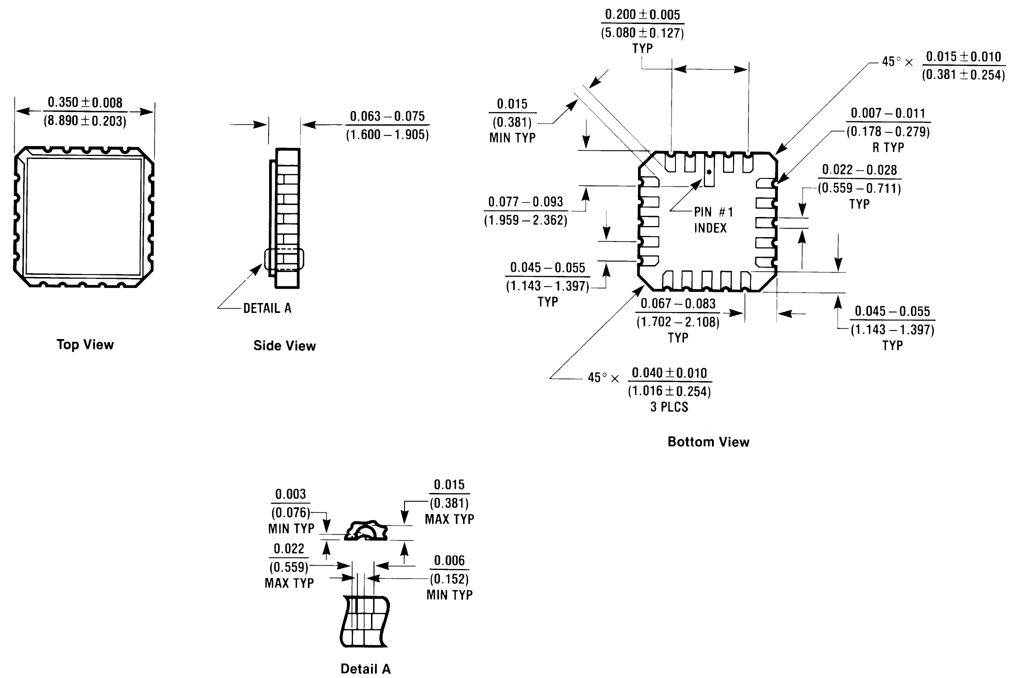
H = High Level, L = Low Level

Note 6: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

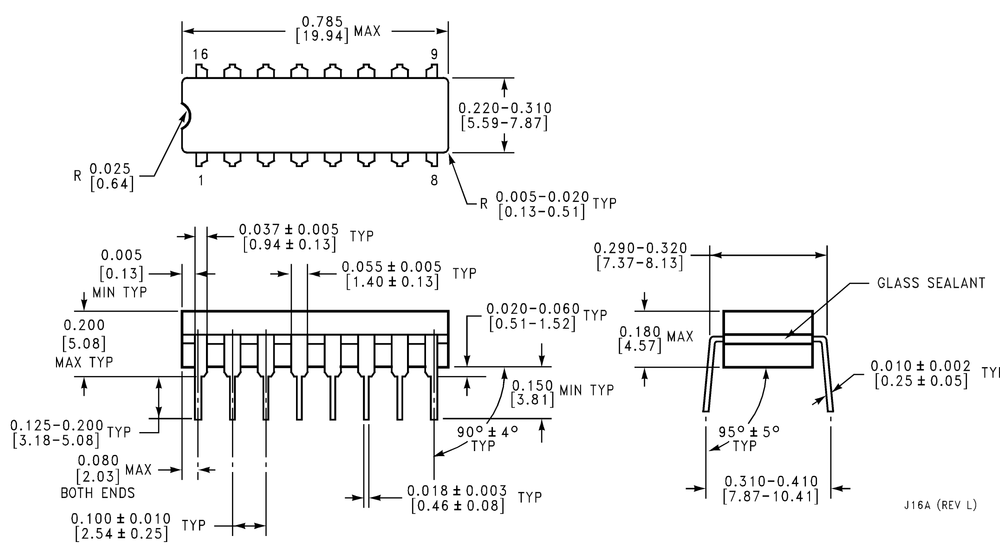
Logic Diagram



Physical Dimensions inches (millimeters) unless otherwise noted

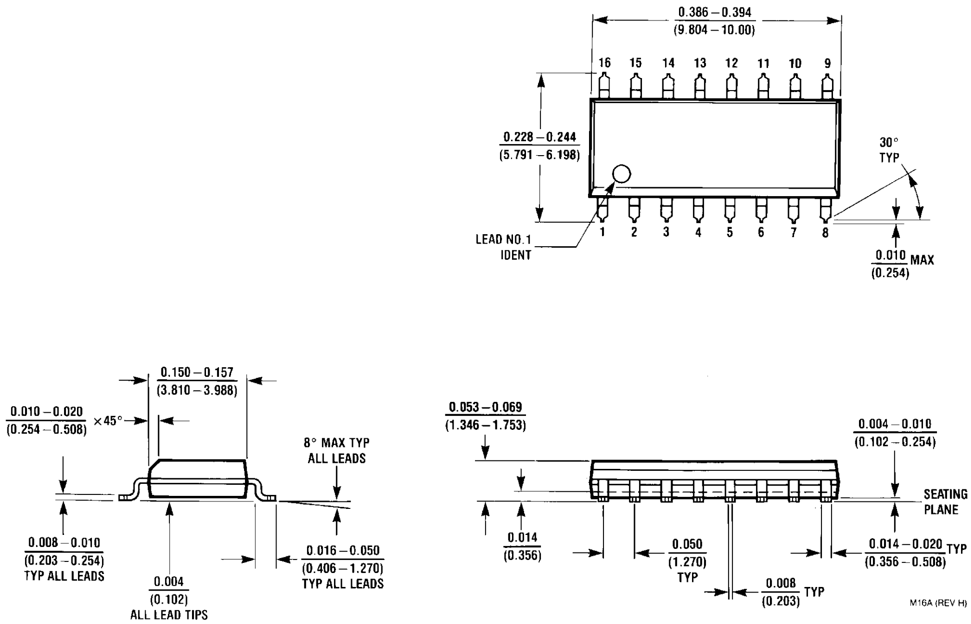


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS283LMQB
Package Number E20A

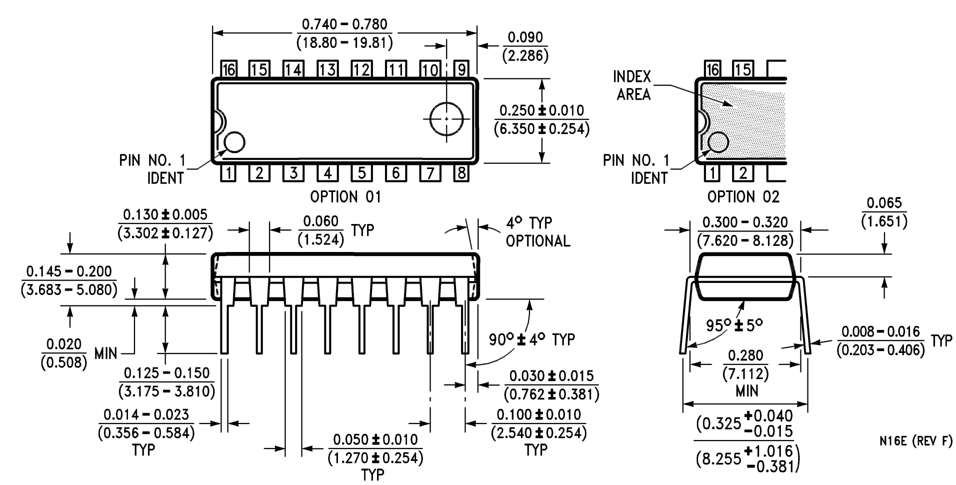


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS283DMQB or DM54LS283J
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

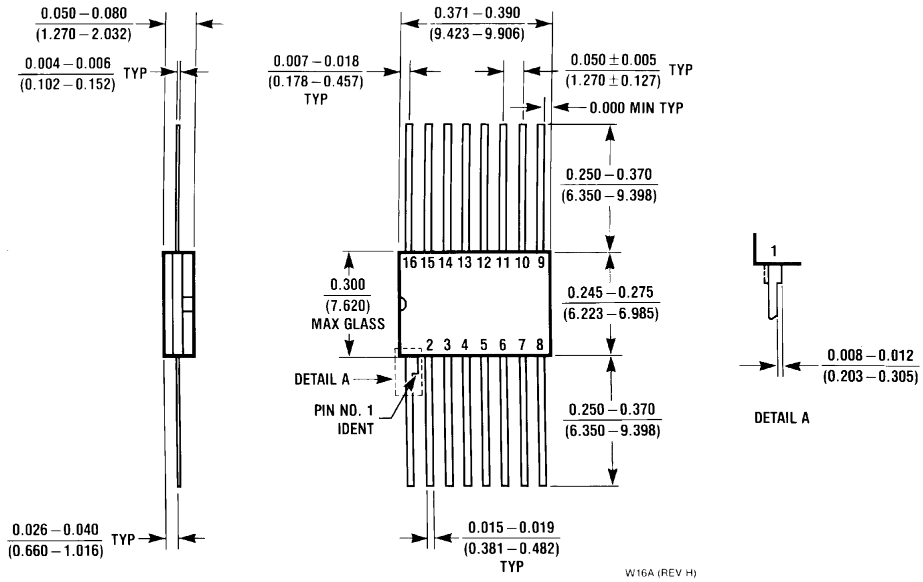


16-Lead Small Outline Molded Package (M)
Order Number DM74LS283M
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS283N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS283FMQB or DM54LS283W
Package Number W16A

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

May 1989

DM74LS290 4-Bit Decade Counter

General Description

The 'LS290 counter is electrically and functionally identical to the 'LS90. Only the arrangement of the terminals has been changed for the 'LS290.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

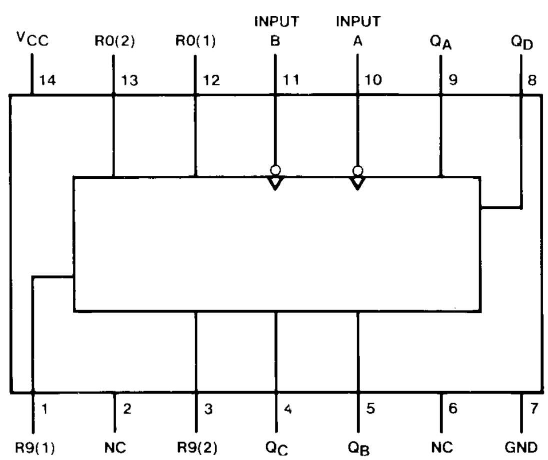
To use the maximum count length (decade) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS290 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6422–1

Order Number DM74LS290M or DM74LS290N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS290 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 6)	A	15			ns
		B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 6)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: $C_L = 15$ pF, $R_L = 2\ k\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2\ k\Omega$, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: $T_A = 25°C$ and V_{CC} 5V.

Function Tables

BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Note A: Output Q_A is connected to input B for BCD count

H = High Logic Level

L = Low Logic Level

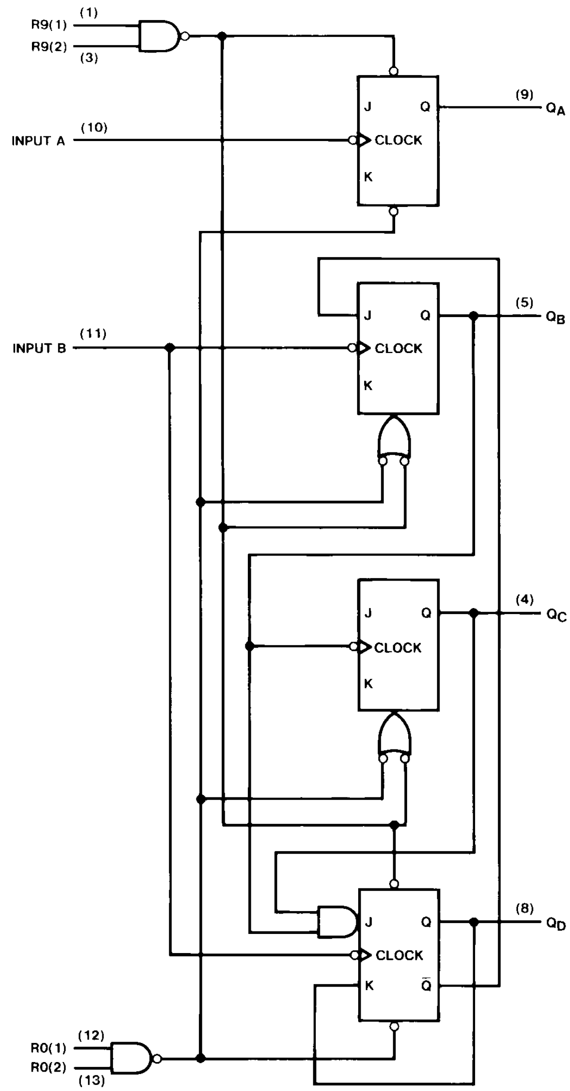
X = Either Low or High Logic Level

Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note B: Output Q_D is connected to input A for bi-quinary count.

Logic Diagram

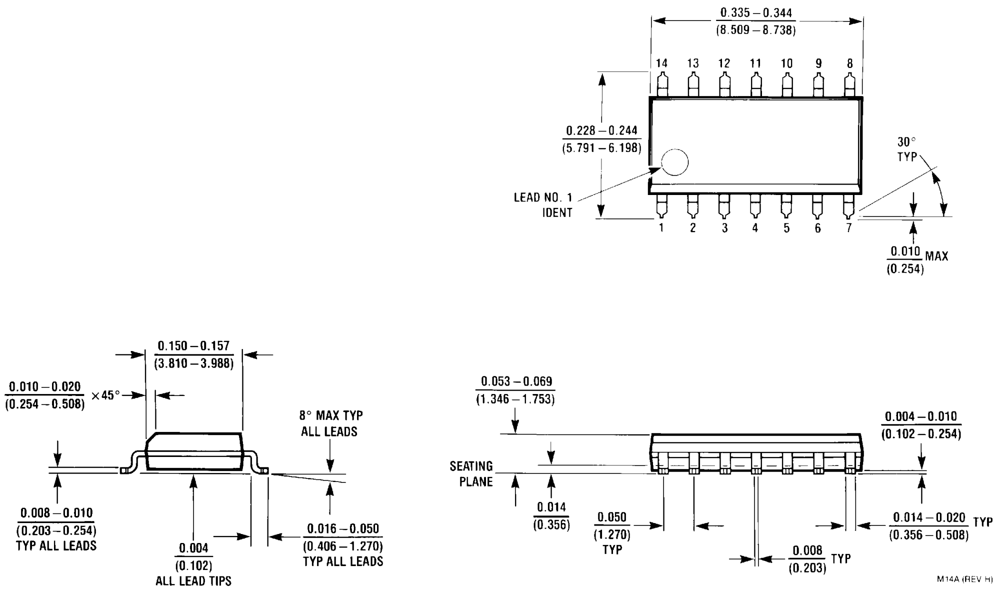


TL/F/6422–2

Reset/Count Truth Table

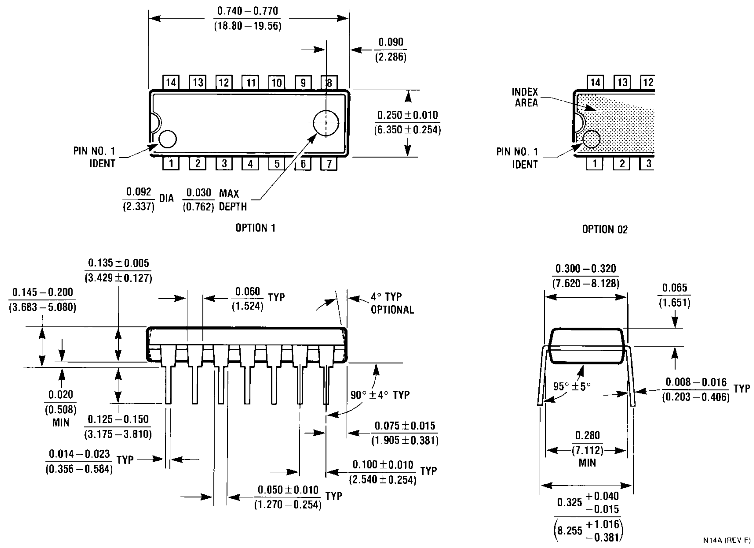
Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS290M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS290N
NS Package Number N14A

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National Semiconductor

June 1989

DM74LS293 4-Bit Binary Counter

General Description

The 'LS293 counter is electrically and functionally identical to the 'LS93. Only the arrangement of the terminals has been changed for the 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

All of these counters have a gated zero reset.

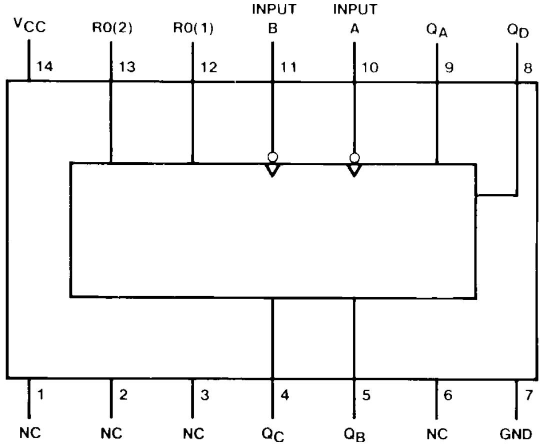
To use the maximum count length (four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6423–1

Order Number DM74LS293M or DM74LS293N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74LS293 Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	MHz
		B to Q_B	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	MHz
		B to Q_B	0		10	
t_W	Pulse Width (Note 6)	A	15			ns
		B	30			
		Reset	15			
t_{REL}	Reset Release Time (Note 6)		25			ns
T_A	Free Air Operating Temperature		0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Reset			20	μA
			A			40	
			B			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 2\ k\Omega$				Units
			$C_L = 15\ pF$		$C_L = 50\ pF$		
			Min	Max	Min	Max	
t_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		93	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: $C_L = 15$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 2: $C_L = 50$ pF, $R_L = 2$ kΩ, $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: $T_A = 25°C$ and $V_{CC} = 5V$.

Function Tables

Count Sequence (See Note C)

Count	Outputs Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Note C: Output Q_A is connected to input B.

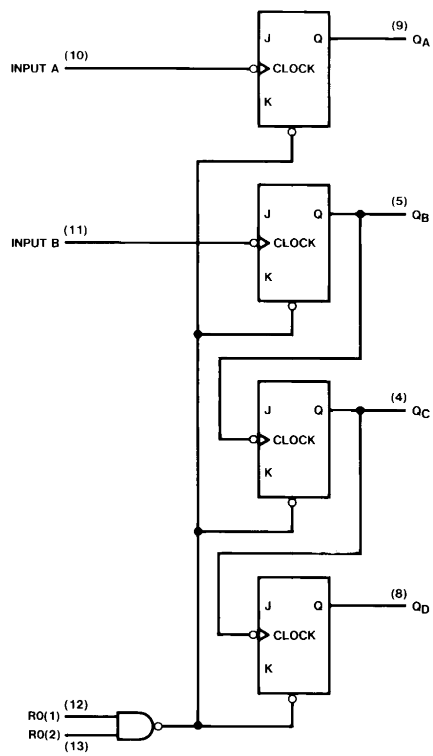
Reset/Count Truth Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram

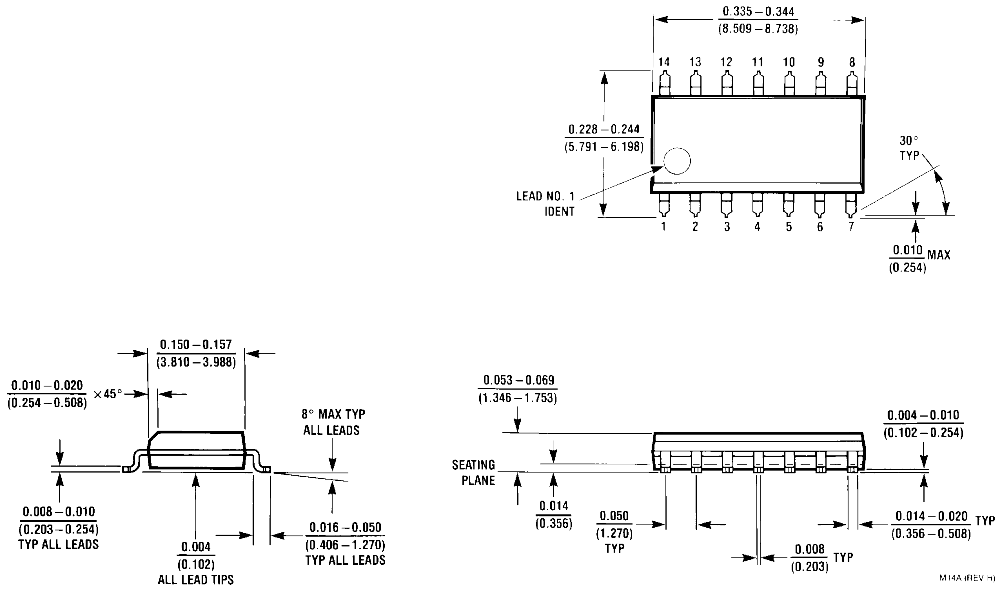
LS293



TL/F/6423–2

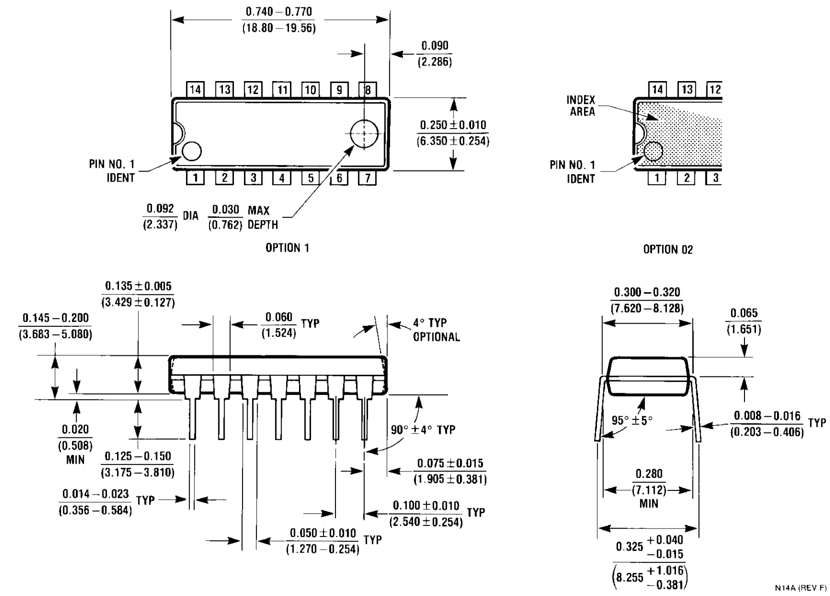
Note: The J and K inputs shown without connection are for reference only and are functionally at a high level.

Physical Dimensions inches (millimeters)



14-Lead Small Outline Molded Package (M)
Order Number DM74LS293M
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS293N
NS Package Number N14A

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National Semiconductor

April 1992

DM54LS295A/DM74LS295A 4-Bit Shift Register with TRI-STATE® Outputs

General Description

The 'LS295A is a 4-bit shift register with serial and parallel synchronous operating modes, and independent TRI-STATE output buffers. The Parallel Enable input (PE) controls the shift-right or parallel load operation. All data transfers and shifting occur synchronous with the HIGH-to-LOW clock transition.

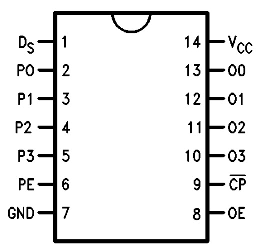
The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). Disabling the output buffers does not affect the shifting or loading of input data, but it does inhibit serial expansion. The device is fabricated with the Schottky barrier diode process for high speed.

Features

- Fully synchronous serial or parallel data transfers
- Negative edge-triggered clock input
- Parallel enable mode control input
- TRI-STATE bussable output buffers

Connection Diagram

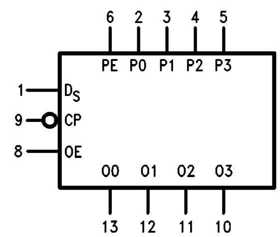
Dual-In-Line Package



TL/F/10183–1

Order Number DM54LS295AJ, DM54LS295AW, DM74LS295AM or DM74LS295AN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



TL/F/10183–2

V_{CC} = Pin 14
GND = Pin 7

Pin Names	Description
PE	Parallel Enable Input (Active HIGH)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
OE	TRI-STATE Output Enable Input (Active HIGH)
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
O0–O3	TRI-STATE Outputs

 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS295A			DM74LS295A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.0			−2.6	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S, P_n to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S, P_n to $\overline{CP}$	10 10			10 10			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW PE to $\overline{CP}$	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW PE to $\overline{CP}$	0 0			0 0			ns
t_w (L)	$\overline{CP}$ Pulse Width LOW	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.4			V
			DM74	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (DM54)				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current Outputs ON	V_{CC} = Max, P_n = GND PE, DS, OE = 4.5V, $\overline{CP}$ = ⎺_				23	mA
	Outputs OFF	V_{CC} = Max, PE, DS = 4.5V P_n, OE, $\overline{CP}$ = GND				25	mA

Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max			20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Shift Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay $\overline{CP}$ to Q_n		30 26	ns
t_{PZH} t_{PZL}	Output Enable Time		18 20	ns
t_{PHZ} t_{PLZ}	Output Disable Time		24 20	ns

Functional Description

This device is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial Data (D_S) and four Parallel Data (P0–P3) inputs and four parallel TRI-STATE output buffers (O0–O3). When the Parallel Enable (PE) input is HIGH, data is transferred from the Parallel Data inputs (P0–P3) into the register synchronous with the HIGH-to-LOW transition of the Clock ($\overline{CP}$). When the PE is LOW, a HIGH-to-LOW transition on the clock transfers the serial data on the D_S input to the register Q0, and shifts data from Q0 to Q1, Q1 to Q2 and Q2 to Q3. The input data and parallel enable are fully edge-triggered and must be stable only one setup time before the HIGH-to-LOW clock transition.

The TRI-STATE output buffers are controlled by an active HIGH Output Enable input (OE). When the OE is HIGH, the four register outputs appear at the O0–O3 outputs. When OE is LOW, the outputs are forced to a high impedance OFF state. The TRI-STATE output buffers are completely independent of the register operation, i.e., the input transitions on the OE input do not affect the serial or parallel data transfers of the register. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Mode Select Table

Operating Mode	Inputs				Outputs			
	PE	$\overline{CP}$	D_S	P_n	Q0	Q1	Q2	Q3
Shift Right	l	↘	l	X	L	q_0	q_1	q_2
	l	↘	h	X	H	q_0	q_1	q_2
Parallel Load	h	↘	X	p_n	p0	p1	p2	p3

*The indicated data appears at the Q outputs when OE is HIGH. When OE is LOW, the indicated data is loaded into the register, but the outputs are all forced to the high impedance OFF state.

p_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

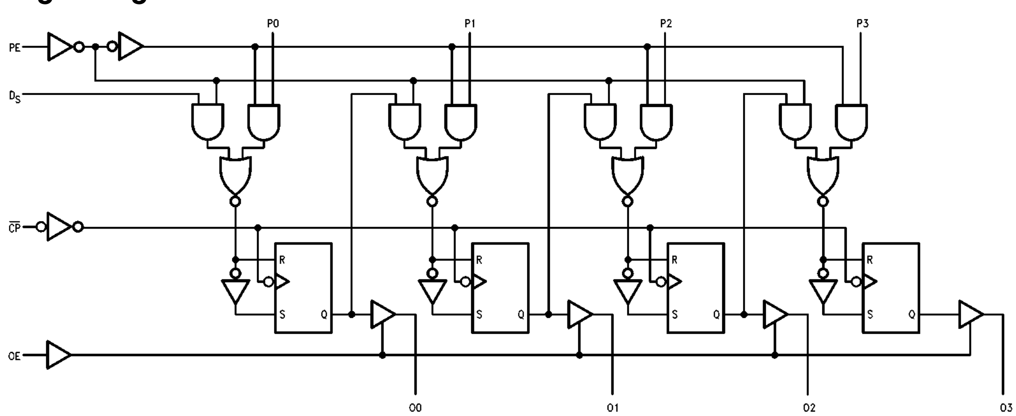
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level

L = LOW Voltage Level

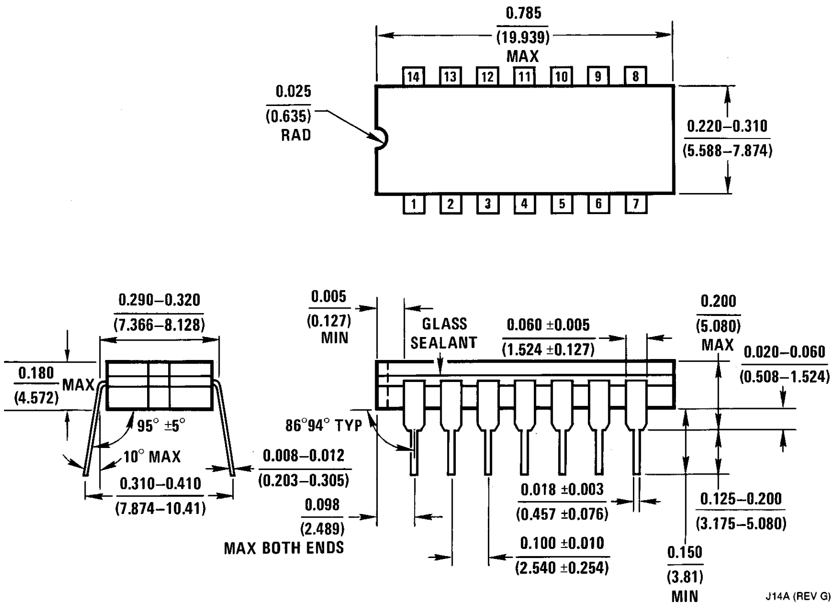
X = Immaterial

Logic Diagram

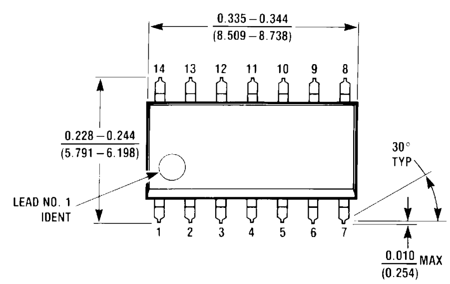


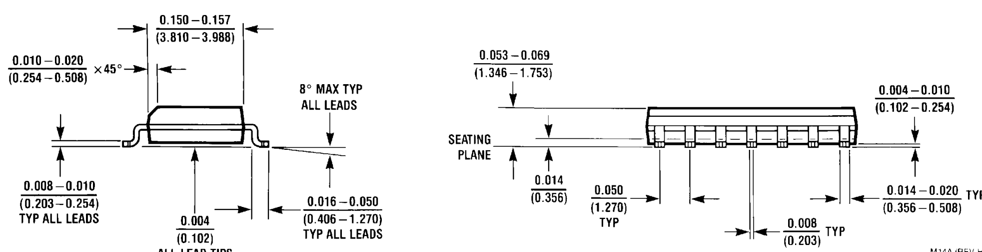
TL/F/10183–3

Physical Dimensions inches (millimeters)



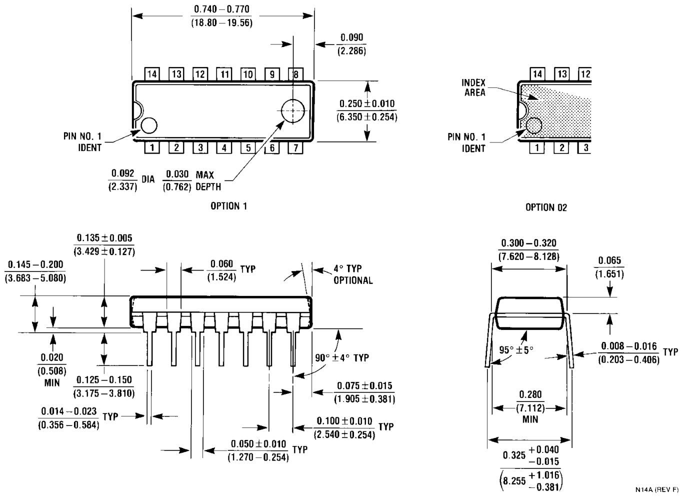
14-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS295AJ
NS Package Number J14A



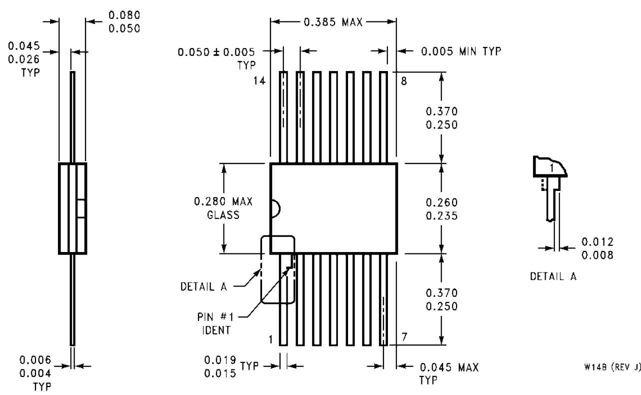


14-Lead Small Outline Molded Package (M)
Order Number DM74LS295AM
NS Package Number M14A

Physical Dimensions inches (millimeters) (Continued)



14-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS295AN
NS Package Number N14A



14-Lead Ceramic Flat Package (W)
Order Number DM54LS295AW
NS Package Number W14B

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March 1998

DM74LS298
Quad 2-Port Register Multiplexer with Storage

General Description

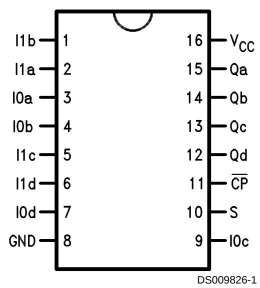
The 'LS298 is a quad 2-port register. It is the logical equivalent of a quad 2-input multiplexer followed by a quad 4-bit edge-triggered register. A Common Select input selects between two 4-bit input ports (data sources). The selected data is transferred to the output register synchronous with the HIGH-to-LOW transition of the Clock input.

Features

- Select from two data sources
- Fully edge-triggered operation
- Typical power dissipation of 65 mW

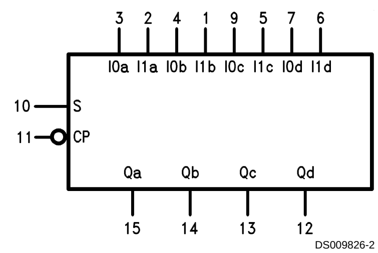
Connection Diagram

Dual-In-Line Package



Order Number DM54LS298J, DM54LS298W, DM74LS298M or DM74LS298N
See Package Number J16A, N16E or W16A

Logic Symbol



V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
S	Common Select Inputs
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
$I0_a$, $I0_d$	Source 0 Data Inputs
$I1_a$, $I1_d$	Source 1 Data Inputs
Q_a, Q_d	Flip-Flip Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS298			DM74LS298			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S to $\overline{CP}$	25 25			25 25			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S to $\overline{CP}$	0 0			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $I0_x$ or $I1_x$ to $\overline{CP}$	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $I0_x$ or $I1_x$ to $\overline{CP}$	5.0 5.0			5.0 5.0			ns
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width HIGH or LOW	20 20			20 20			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, $I0_n$, $I1_n$, S = GND, $\overline{CP}$ = ⌐_				21	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

at V_{CC} = +5V and T_A = +25˚C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output $\overline{CP}$ to Q_n		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output $\overline{CP}$ to Q_n		25	ns

Functional Description

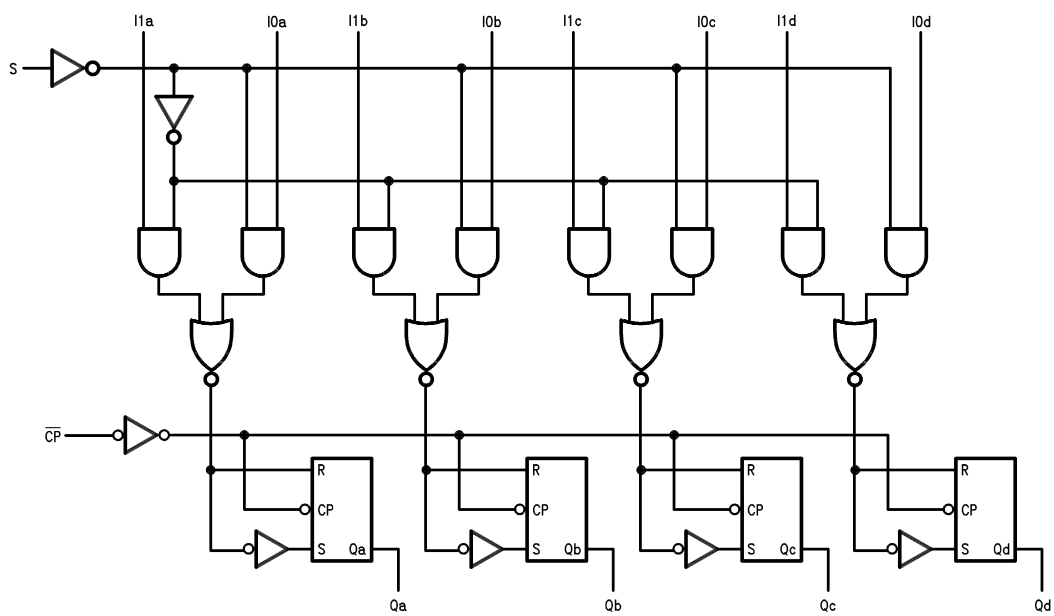
This device is a high speed quad 2-port register. It selects four bits of data from two sources (ports) under the control of a Common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit output register is fully edge-triggered. The Data inputs (I_{nx}) and Select input (S) need be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

Truth Table

Inputs			Output
S	$I0_x$	$I1_x$	Q_x
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

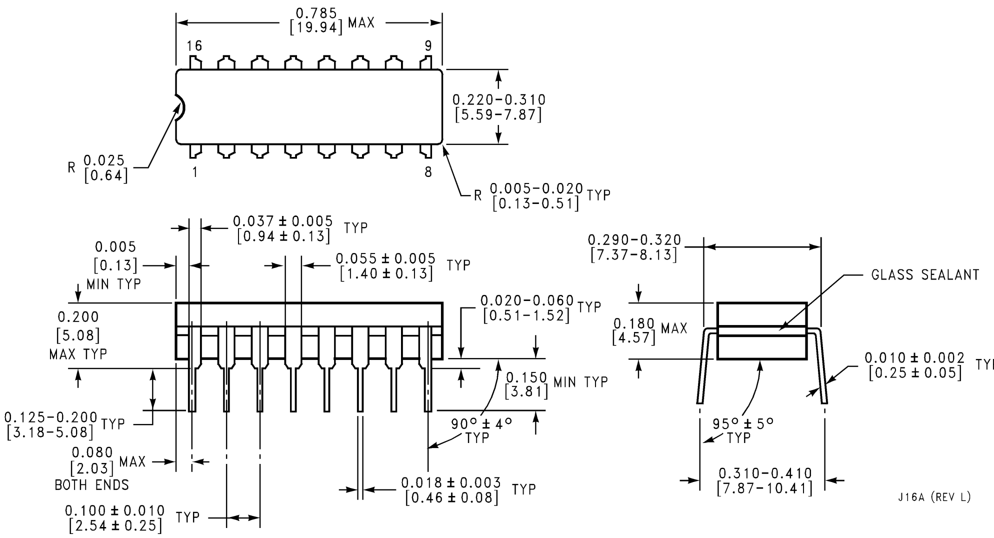
l = LOW Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one setup time prior to the HIGH-to-LOW clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

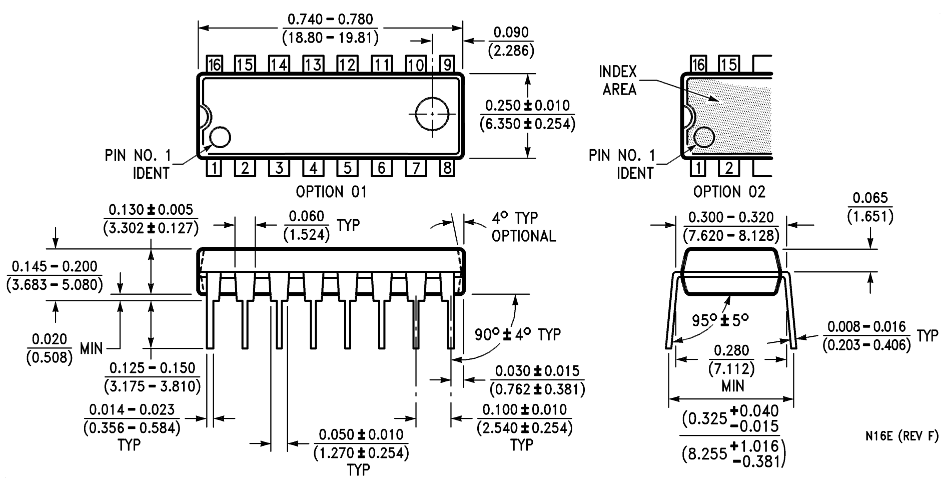


DS009826-3

Physical Dimensions inches (millimeters) unless otherwise noted

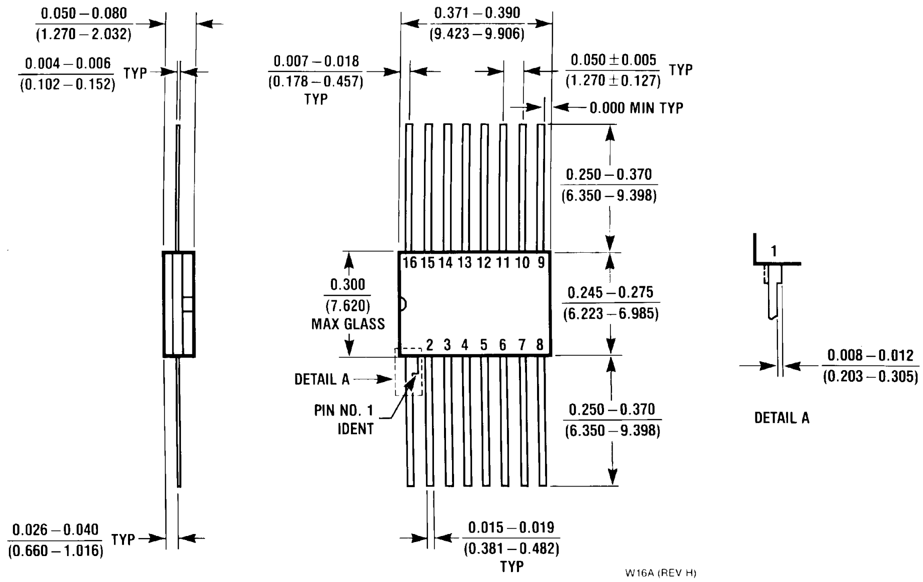


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS298J
Package Number J16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS298N
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS298W
NS Package Number W16A

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March 1998

DM74LS299
8-Input Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

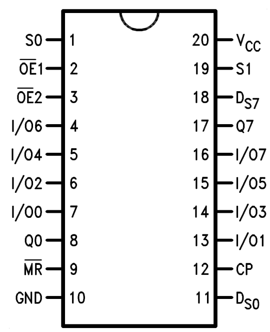
The 'LS299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Separate outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, load and store
- Separate shift right serial input and shift left serial input for easy cascading
- 3-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



DS009827-1

Order Number DM54LS299E, DM54LS299J, DM54LS299W, DM74LS299WM or DM74LS299N
See Package Number E20A, J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_{S0}	Serial Data Input for Right Shift
D_{S7}	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}1$, $\overline{OE}2$	3-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or 3-STATE Parallel Outputs
Q0–Q7	Serial Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS299			DM74LS299			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current	Q0, Q7			−0.4			−0.4	mA
		I/O0–I/O7			−2.6			−2.6	mA
I_{OL}	Low Level Output Current	Q0, Q7			4			8	mA
		I/O0–I/O7			12			24	mA
T_A	Free Air Operating Temperature		−55		125	0		70	˚C
t_s(H) t_s(L)	Setup Time HIGH or LOW S0 or S1 to CP		24 24			24 24			ns
t_h(H) t_h(L)	Hold Time HIGH or LOW S0 or S1 to CP		5 5			0 0			ns
t_s(H) t_s(L)	Setup Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP		15 15			10 10			ns
t_h(H) t_h(L)	Hold Time HIGH or LOW I/O_n, D_{S0}, D_{S7} to CP		5 5			0 0			ns
t_w(H) t_w(L)	CP Pulse Width HIGH or LOW		15 15			15 15			ns
t_w(L)	$\overline{MR}$ Pulse Width LOW		15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP		10			10			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max		DM54	2.5			V
		V_{IL} = Max	Q0, Q7	DM74	2.7	3.4		
			I/O0–I/O7		2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max		DM54			0.4	V
		V_{IH} = Min		DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min		DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V (DM54)		Inputs			0.1	mA
		V_I = 7V (DM74)		Sn			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V		Sn			40	µA
				Inputs			20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V		Sn			−0.8	mA
				Inputs			−0.4	mA

Electrical Characteristics (Continued)

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	Q_0, Q_7	−20		−100	mA
			I/O_0–I/O_7	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max, $\overline{OE}$ = 4.5V				60	mA
I_{OZH}	3-STATE Output Off Current High	V_{CC} = Max, V_O = 2.7V				40	µA
I_{OZL}	3-STATE Output Off Current Low	V_{CC} = Max, V_O = 0.4V				−400	µA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

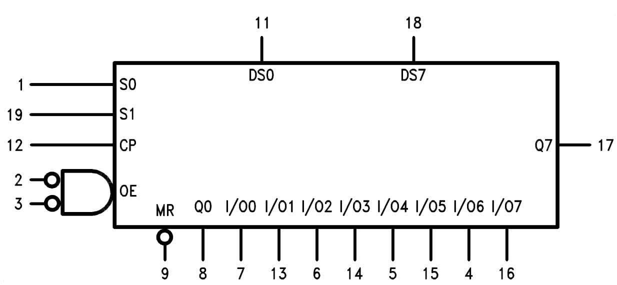
Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C (See Section 1 for waveforms and load configurations)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF Min	Max	Units
f_{max}	Maximum Input Frequency	35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q0 or Q7		26 28	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 35	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0 or Q7		28	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n		35	ns
t_{PZH} t_{PZL}	Output Enable Time		18 25	ns
t_{PHZ} t_{PLZ}	Output Disable Time		15 20	ns

Logic Symbol



V_{CC} = Pin 20
GND = Pin 10

Functional Description

The ’LS299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by the S0 and S1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

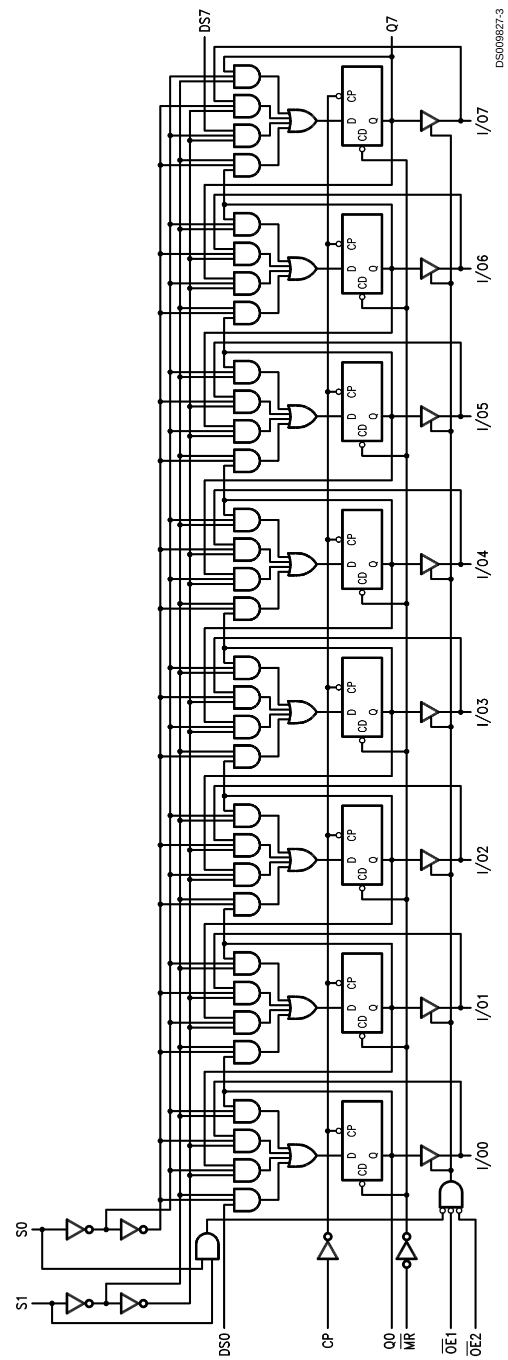
A HIGH signal on either $\overline{OE}1$ or $\overline{OE}2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

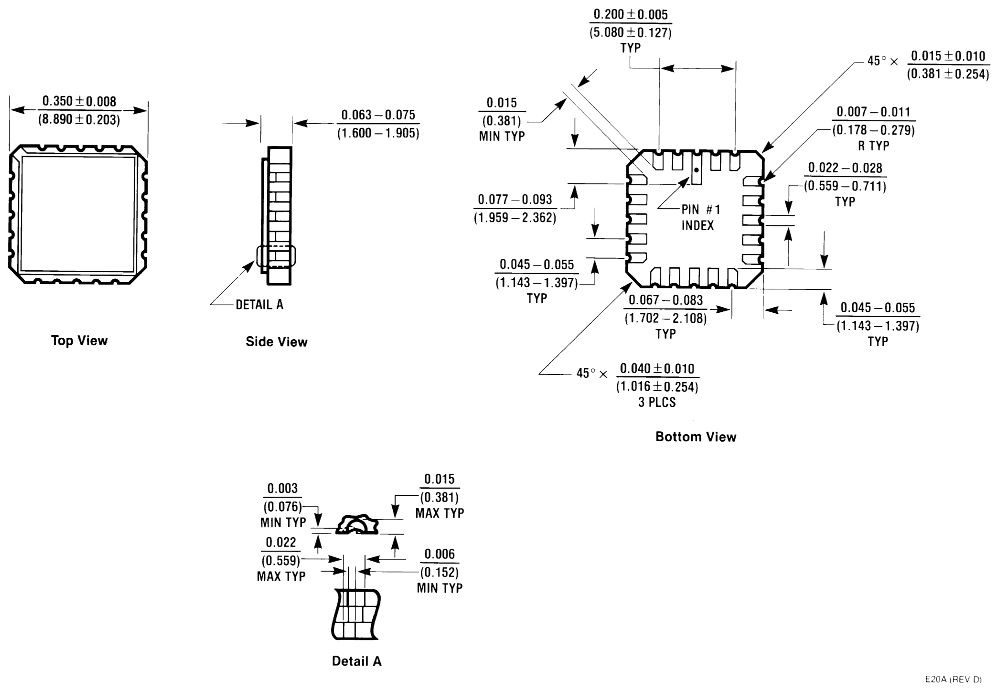
Inputs				Response
$\overline{MR}$	S1	S0	CP	
L	X	X	X	Asynchronous Reset; Q0–Q7 = LOW
H	H	H	$\uparrow$	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	$\uparrow$	Shift Right; $D_{S0} \rightarrow Q0$, $Q0 \rightarrow Q1$, etc.
H	H	L	$\uparrow$	Shift Left; $D_{S7} \rightarrow Q7$, $Q7 \rightarrow Q6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

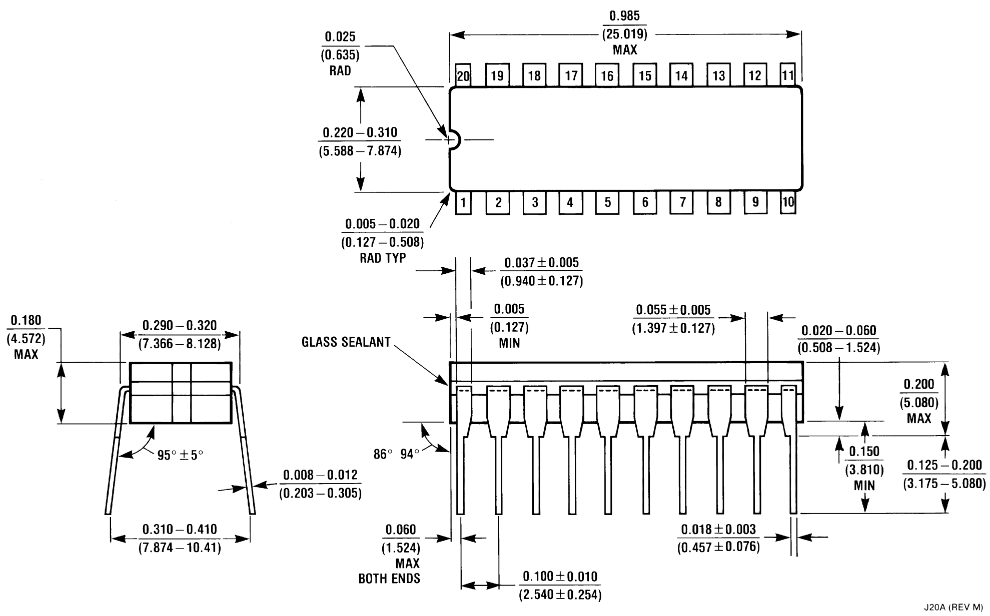


Physical Dimensions inches (millimeters) unless otherwise noted



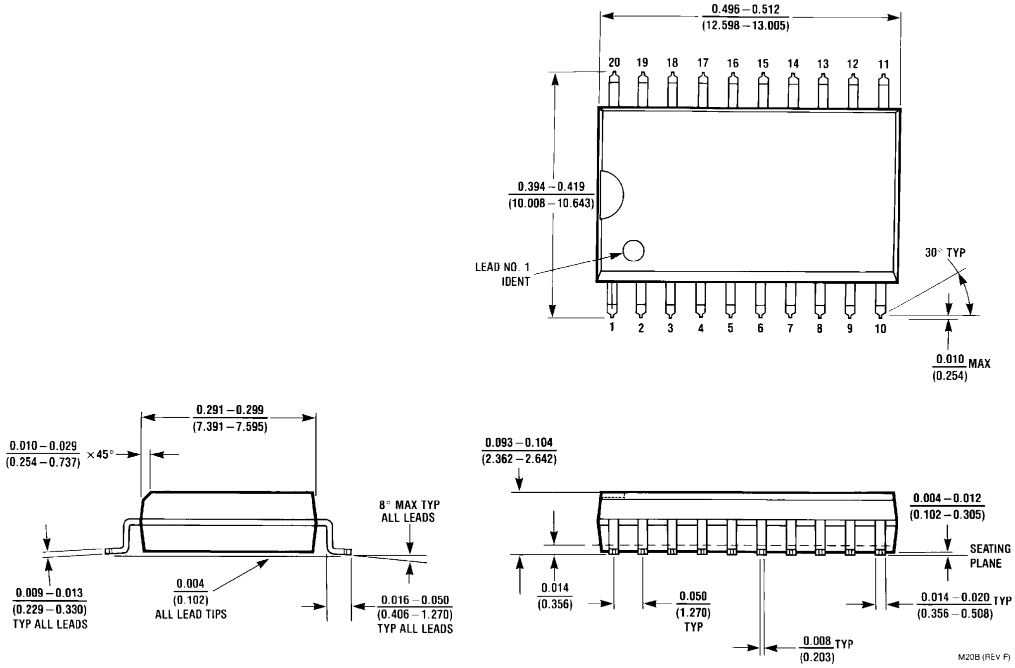
Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS299E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

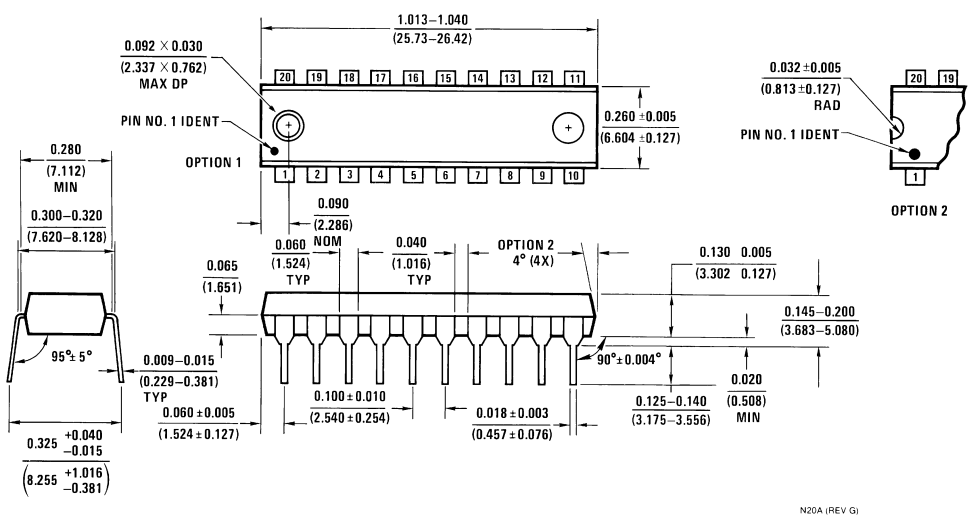


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS299J
Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

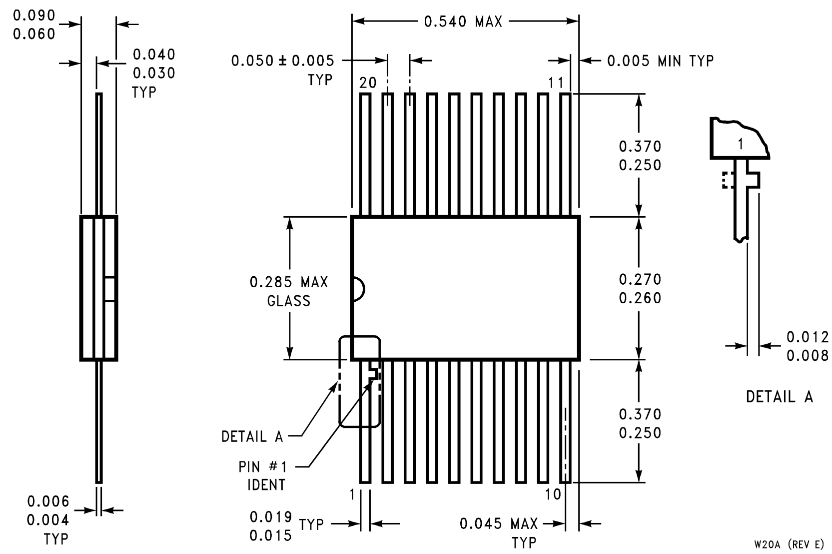


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS299WM
Package Number M20B



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS299N
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS299W
Package Number W20A

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National Semiconductor

April 1992

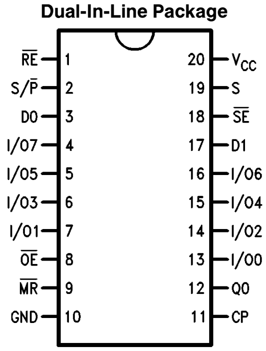
DM54LS322/DM74LS322
8-Bit Serial/Parallel Register with Sign Extend

General Description

The 'LS322 is an 8-bit shift register with provision for either serial or parallel loading and with TRI-STATE® parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and parallel load. An asynchronous Master Reset ($\overline{MR}$) input overrides clocked operation and clears the register. The '322 is specifically designed for operation with the '384 Multiplier and provides the sign extend function required for the '384.

Connection Diagram

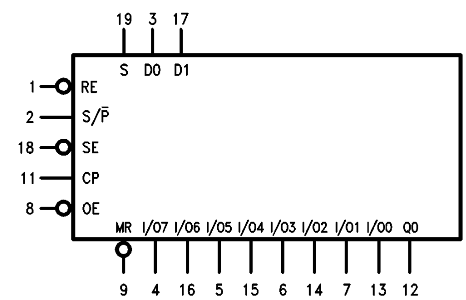
Dual-In-Line Package



TL/F/9828–1

Order Number DM54LS322J, DM54LS322W
DM74LS322WM or DM74LS322N
See NS Package Number J20A, M20B, N20A or W20A

Logic Symbol



TL/F/9828–2

V_{CC} = Pin 20
GND = Pin 10

Pin Names	Description
$\overline{RE}$	Register Enable Input (Active LOW)
S/$\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input
$\overline{SE}$	Sign Extend Input (Active LOW)
S	Serial Data Select Input
D0, D1	Serial Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
Q0	Bi-State Serial Output
I/O0–I/O7	Multiplexed Parallel Inputs or TRI-STATE Parallel Outputs

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RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS322			DM74LS322			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{RE}$ to CP	24 24			24 24			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{RE}$ to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW D0, D1 or I/O_n to CP	15 15			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D0, D1 or I/O_n to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SE}$ to CP	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SE}$ to CP	0 0			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW S$\overline{P}$ to CP	24 24			24 24			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW S to CP	15 15			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S or S$\overline{P}$ to CP	0 0			0 0			ns
t_w (H)	CP Pulse Width HIGH	15			15			ns
t_w (L)	$\overline{MR}$ Pulse Width LOW	15			15			ns
t_{rec}	Recovery Time $\overline{MR}$ to CP	15			15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	$V_{CC} = $ Min, $I_I = -18$ mA				-1.5	V
V_{OH}	High Level Output Voltage	$V_{CC} = $ Min, $I_{OH} = $ Max $V_{IL} = $ Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	$V_{CC} = $ Min, $I_{OL} = $ Max $V_{IH} = $ Min	DM54			0.4	V
			DM74		0.35	0.5	
		$I_{OL} = 4$ mA, $V_{CC} = $ Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	$V_{CC} = $ Max, $V_I = 7V$ $V_I = 10V$ (DM54)	Others			0.1	mA
			S Input			0.2	
			SE Input			0.3	
I_{IH}	High Level Input Current	$V_{CC} = $ Max, $V_I = 2.7V$	Others			20	μA
			S Input			40	
			SE Input			60	
I_{IL}	Low Level Input Current	$V_{CC} = $ Max, $V_I = 0.4V$	Others			-0.4	mA
			S Input			-0.8	
			SE Input			-1.2	
I_{OS}	Short Circuit Output Current	$V_{CC} = $ Max (Note 2)	DM54 I/On	-30		-130	mA
			DM54 Qn	-20		-100	
			DM74	-20		-100	
I_{CC}	Supply Current	$V_{CC} = $ Max				60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	$V_{CC} = $ Max $V_O = 2.7V$				40	μA
I_{OZL}	TRI-STATE Output Off Current LOW	$V_{CC} = $ Max $V_O = 0.4V$				-0.4	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2$ kΩ, $C_L = 15$ pF				Units
		DM54LS		DM74LS		
		Min	Max	Min	Max	
f_{max}	Maximum Clock Frequency	35		35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n**		25 35		25 34	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q0		26 28		26 29	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n**		35		34	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q0		28		28	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n**		18 25		21 23	ns

**$C_L = 50$ pF

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$C_L = 15$ pF				Units
		DM54LS		DM74LS		
		Min	Max	Min	Max	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n*		15 20		15 15	ns
t_{PZH} t_{PZL}	Output Enable Time $S/\overline{P}$ to I/O_n**		22 30		25 25	ns
t_{PHZ} t_{PLZ}	Output Disable Time $S\overline{P}$ to I/O_n*		23 23		40 26	ns

*$C_L = 5$ pF

**$C_L = 50$ pF

Functional Description

The 'LS322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on $\overline{RE}$ enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on $S/\overline{P}$ enables shift right, while a LOW signal disables the TRI-STATE output buffers and enables parallel loading. In the shift right mode a HIGH signal on $\overline{SE}$ enables serial entry from either D0 or D1, as determined by the S input. A LOW signal on $\overline{SE}$ enables shift right but Q7 reloads its contents, thus performing the sign extend function required for the '384 Twos Complement Multiplier. A HIGH signal on $\overline{OE}$ disables the TRI-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

Mode Table

Mode	Inputs							Outputs								
	$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}$*	CP	I/O7	I/O6	I/05	I/O4	I/O3	I/O2	I/O1	I/O0	Q0
Clear	L L	X X	X X	X X	X X	L H	X X	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L Z	L L
Parallel Load	H	L	L	X	X	X	↑	I7	I6	I5	I4	I3	I2	I1	I0	I0
Shift Right	H H	L L	H H	H H	L H	L L	↑ ↑	D0 D1	O7 O7	O6 O6	O5 O5	O4 O4	O3 O3	O2 O2	O1 O1	O1 O1
Sign Extend	H	L	H	L	X	L	↑	O7	O7	O6	O5	O4	O3	O2	O1	O1
Hold	H	H	X	X	X	L	↑	NC	NC	NC	NC	NC	NC	NC	NC	NC

*When the $\overline{OE}$ input is HIGH, all I/O_n terminals are at the high-impedance state; sequential operation or clearing of the register is not affected.

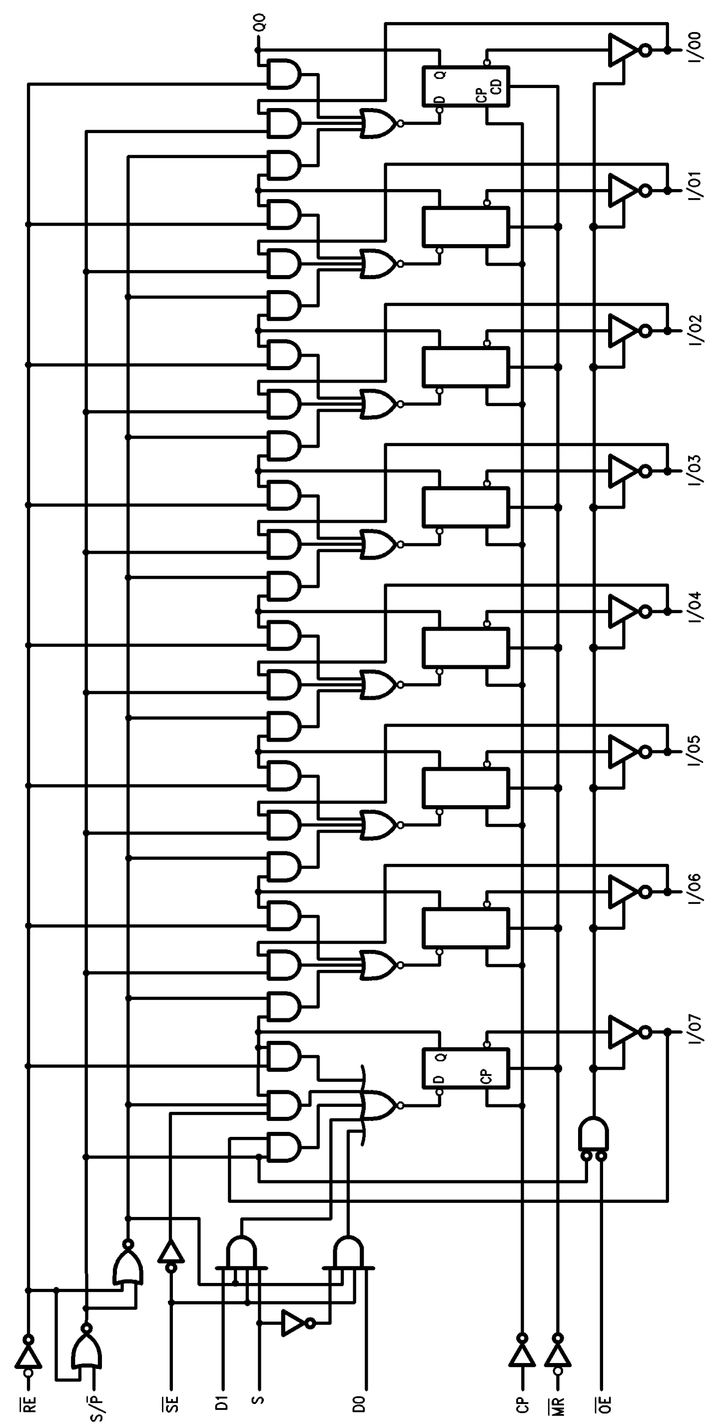
I7–I0 = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except Q0) are isolated from the I/O terminal.

D0, D1 = The level of the steady-state inputs to the serial multiplexer input.

O7–O0 = The level of the respective Q_n flip-flop prior to the last Clock LOW-to-HIGH transition.

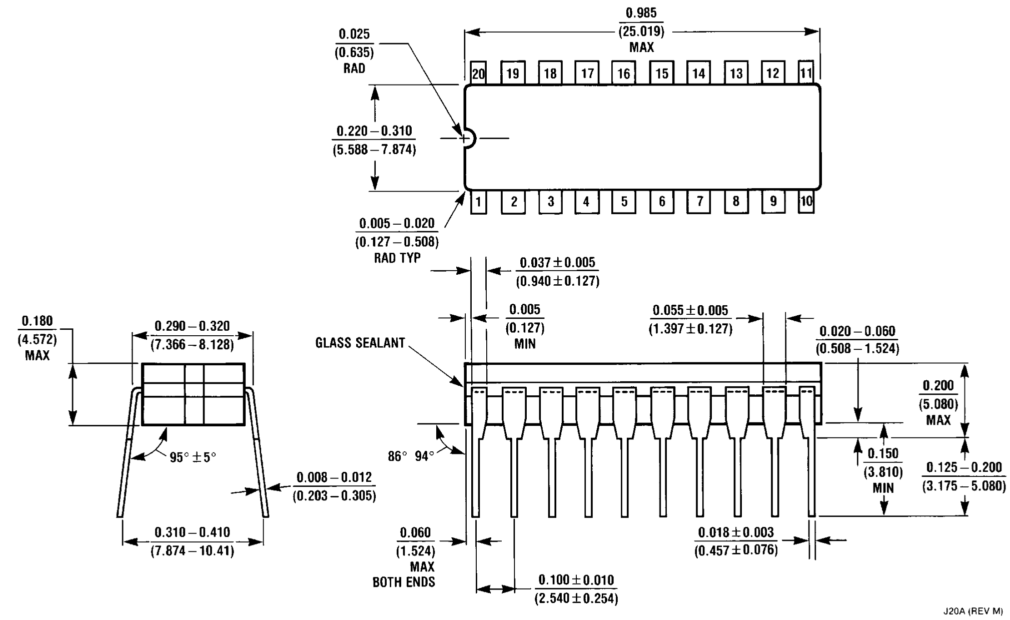
NC = No Change Z = High-Impedance Output State H = HIGH Voltage Level L = LOW Voltage Level

Logic Diagram

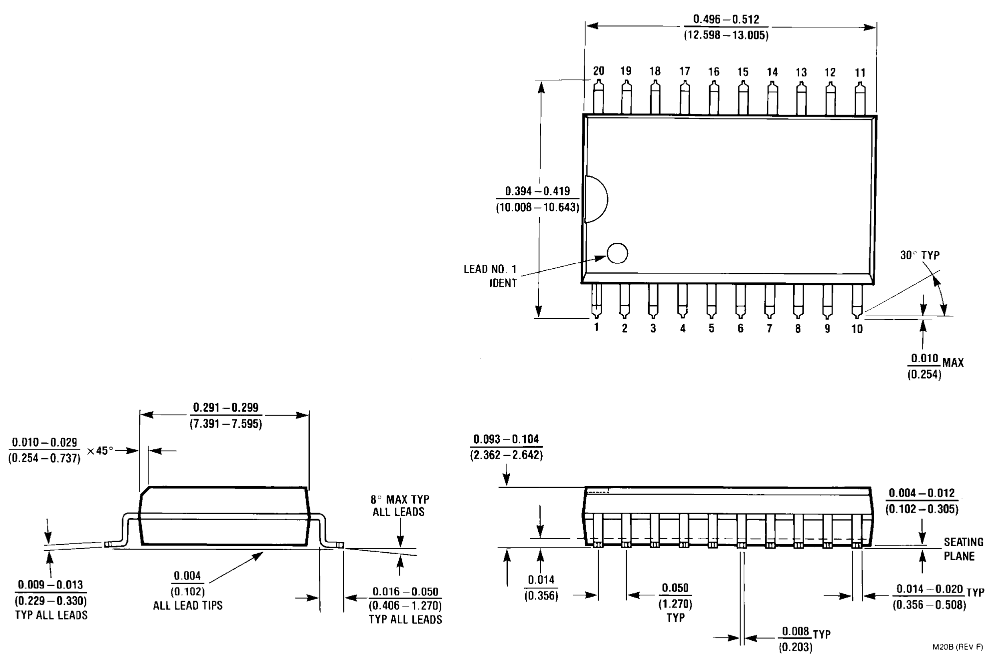


TL/F/9828-3

Physical Dimensions inches (millimeters)

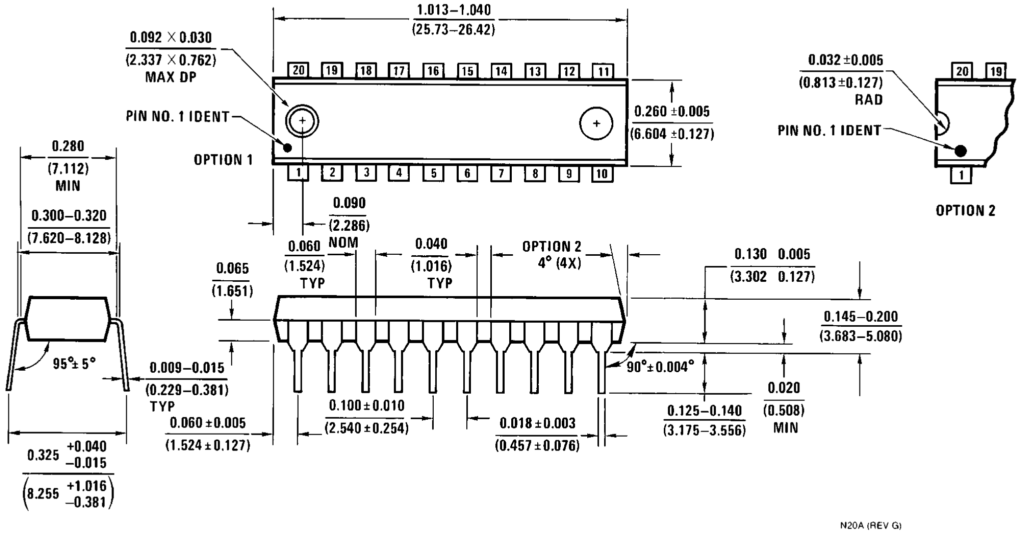


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS322J
NS Package Number J20A



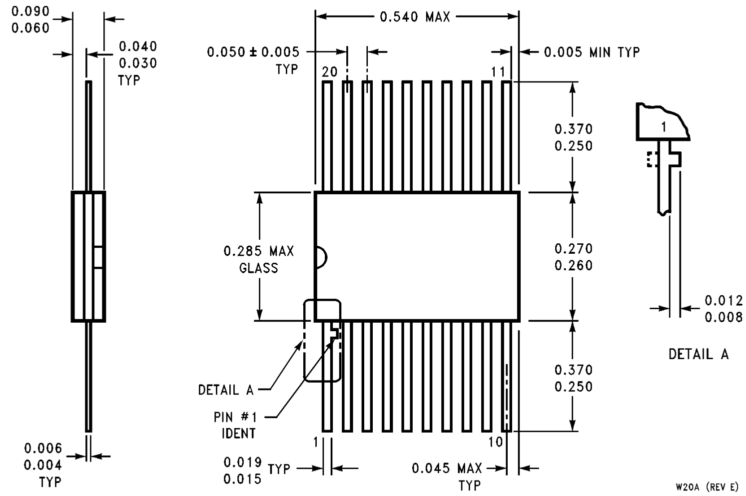
20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS322WM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS322N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS322W
NS Package Number W20A

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National Semiconductor

April 1992

DM54LS323/DM74LS323 8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

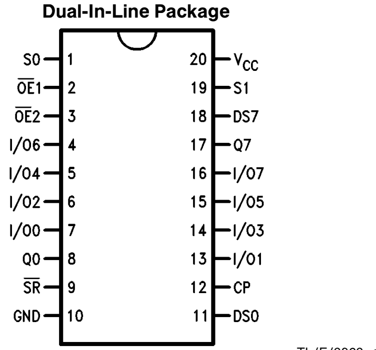
The 'LS323 is an 8-bit universal shift/storage register with TRI-STATE® outputs. Its function is similar to the 'LS299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate inputs and outputs are provided for flip-flops Q0 and Q7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right, and parallel load. All modes are activated on the LOW-to-HIGH transition of the Clock.

Features

- Common I/O for reduced pin count
- Four operation modes: shift left, shift right, parallel load and store
- Separate continuous inputs and outputs from Q0 and Q7 allow easy cascading
- Fully synchronous reset
- TRI-STATE outputs for bus oriented applications

Connection Diagram

Dual-In-Line Package



TL/F/9829–1

Order Number DM54LS323J, DM54LS323W, DM74LS323WM or DM74LS323N
See NS Package Number J20A, M20B, N20A or W20A

Pin Names	Description
CP	Clock Pulse Input (Active Rising Edge)
D_S0	Serial Data Input for Right Shift
D_S7	Serial Data Input for Left Shift
S0, S1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input (Active LOW)
$\overline{OE}1$, $\overline{OE}2$	TRI-STATE Output Enable Inputs (Active LOW)
I/O0–I/O7	Parallel Data Inputs or TRI-STATE Parallel Outputs
Q0, Q7	Serial Outputs

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS323			DM74LS323			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW S0 or S1 to CP	24 24			24 24			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW S0 or S1 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	15 15			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW I/O_n, D_S0, D_S7 to CP	5 5			0 0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{SR}$ to CP	30 20			15 15			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{SR}$ to CP	0 0			0 0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	15 15			15 15			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V V_I = 10V (DM54)	Others			0.1	mA
			S_n Inputs			0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Others			20	μA
			S_n Inputs			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Others			−0.4	mA
			S_n Inputs			−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				60	mA
I_{OZH}	TRI-STATE Output Off Current HIGH	V_{CC} = Max V_O = 2.7V				40	μA
I_{OZL}	TRI-STATE Output Off Current LOW	V_{CC} = Max V_O = 0.4V				−400	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	DM54LS323		DM74LS323		Units
		C_L = 15 pF		R_L = 2 kΩ, C_L = 15 pF		
		Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	35		35		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q0 or Q7		26 28		23 25	ns
t_{PLH} t_{PHL}	Propagation Delay CP to I/O_n		25 35		25 29	ns
t_{PZH} t_{PZL}	Output Enable Time C_L = 50 pF		18 25		18 23	ns
t_{PHZ} t_{PLZ}	Output Disable Time C_L = 5 pF		15 20		15 15	ns

Functional Description

The 'LS323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S0 and S1 as shown in the Mode Select Table. All flip-flop outputs are brought out through TRI-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q0 and Q7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

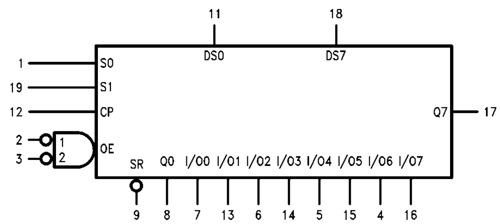
A HIGH signal on either $\overline{OE}$1 or $\overline{OE}$2 disables the TRI-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The TRI-STATE buffers are also disabled by HIGH signals on both S0 and S1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S1	S0	CP	
L	X	X	↗	Synchronous Reset; Q0–Q7 = LOW
H	H	H	↗	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	↗	Shift Right; DS0 → Q0, Q0 → Q1, etc.
H	H	L	↗	Shift Left; DS7 → Q7, Q7 → Q6, etc.
H	H	H	X	Hold

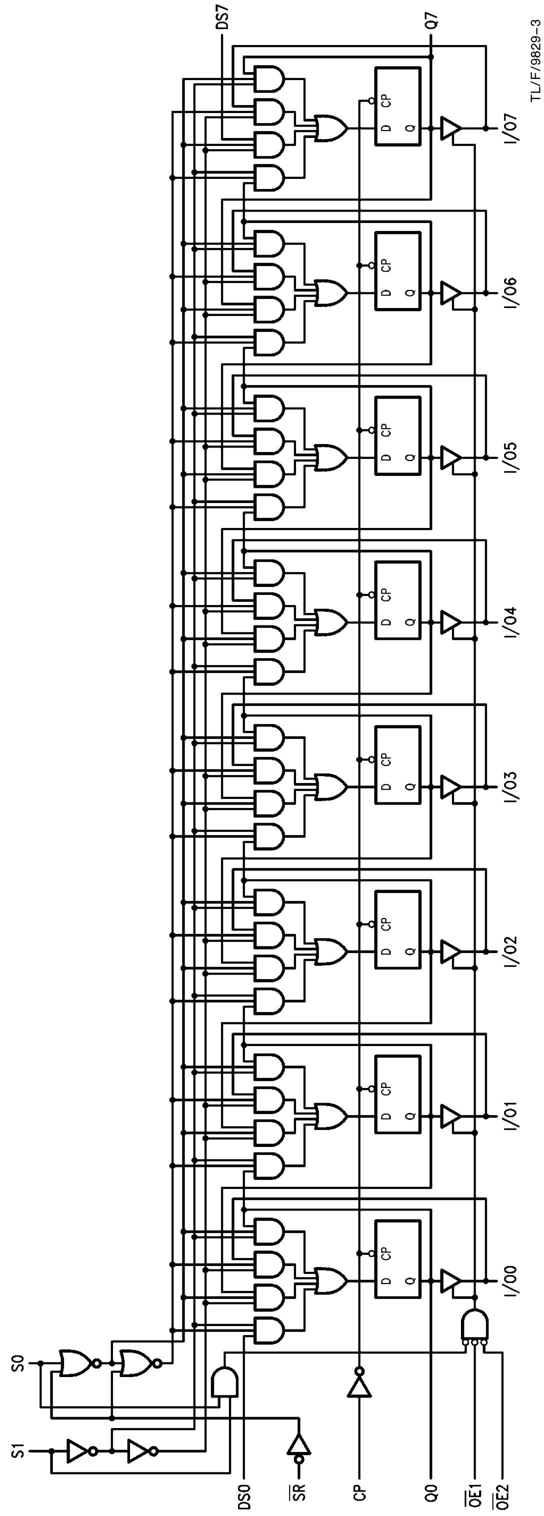
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Symbol

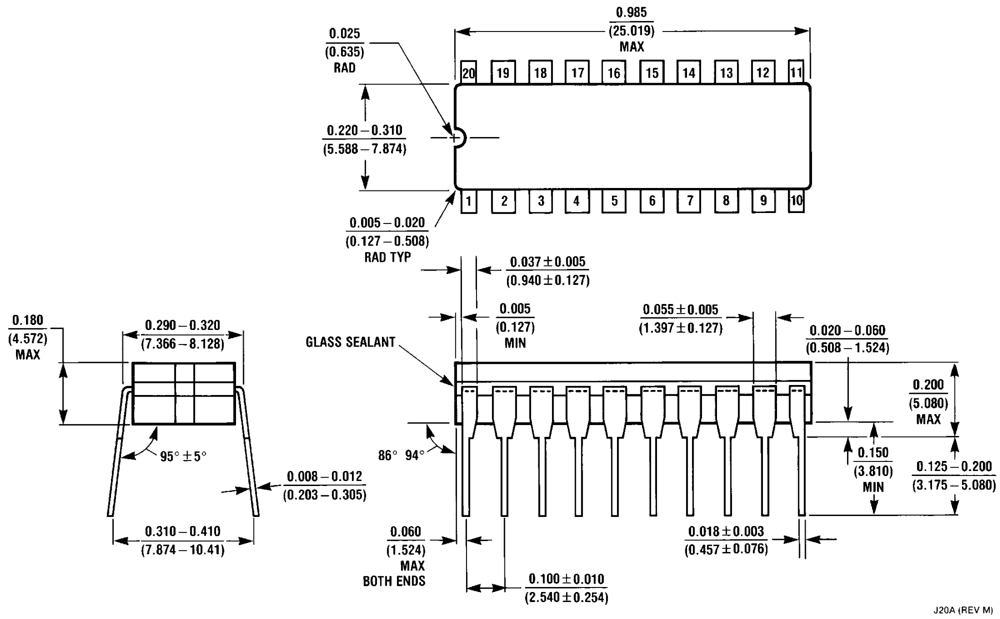


V_{CC} = Pin 20
GND = Pin 10
TL/F/9829–2

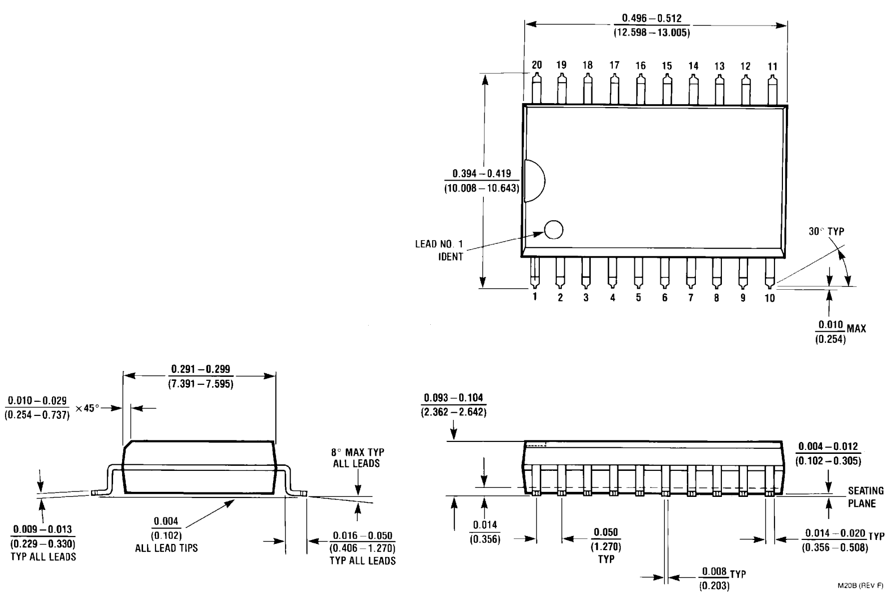
Logic Diagram



Physical Dimensions inches (millimeters)

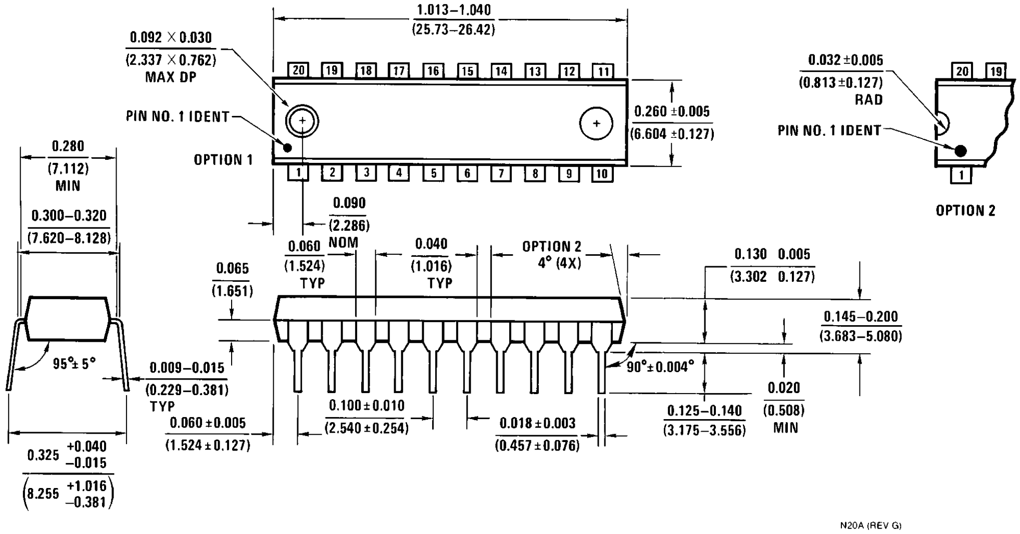


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS323J
NS Package Number J20A



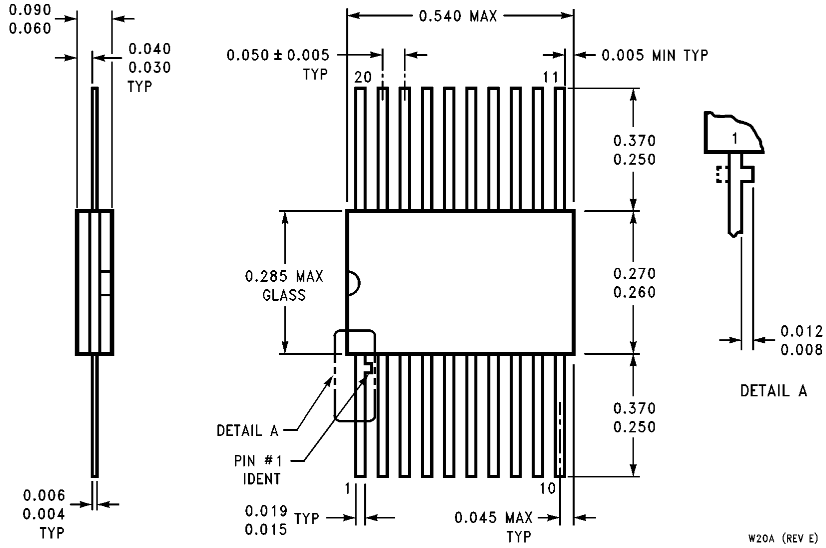
20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS323WM
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS323N
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flat Package (W)
Order Number DM54LS323W
NS Package Number W20A

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National Semiconductor

May 1992

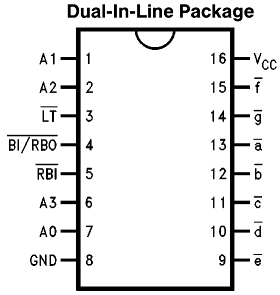
DM54LS347/DM74LS347 BCD to 7-Segment Decoder/Driver

General Description

The ’LS347 is the same as the ’LS47 except that the Output OFF Voltage, V_{OH}, is specified as 7.0V rather than 15V, with the same I_{OH} limit of 250 μA. For all other information please refer to the ’LS47 data sheet.

Connection Diagram

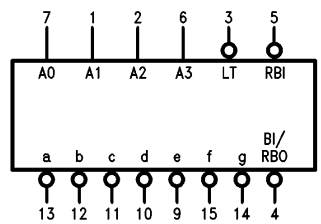
Dual-In-Line Package



TL/F/10184–1

Order Number DM54LS347J, DM54LS347W, DM74LS347M or DM74LS347N
See NS Package Number J16A, M16A, N16E or W16A

Logic Symbol



TL/F/10184–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
A0–A3	BCD Inputs
$\overline{RBI}$	Ripple Blanking Input (Active LOW)
$\overline{LT}$	Lamp Test Input (Active LOW)
$\overline{BI}/\overline{RBO}$	Blanking Input (Active LOW) or Ripple Blanking Output (Active LOW)
$\overline{a}$–$\overline{g}$	*Segment Outputs (Active LOW)

*OC—Open Collector

 TL/F/10184 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS347			DM74LS347			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Voltage			−50			−50	μA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Other Input			−0.4	mA
			$BI/\overline{RBO}$ Input			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−0.3		−2.0	mA
			DM74	−0.3		−2.0	
I_{CC}	Supply Current	V_{CC} = Max				13	mA
I_{OFF}		Segment Outputs, V_O = 7V				250	μA

Switching Characteristics

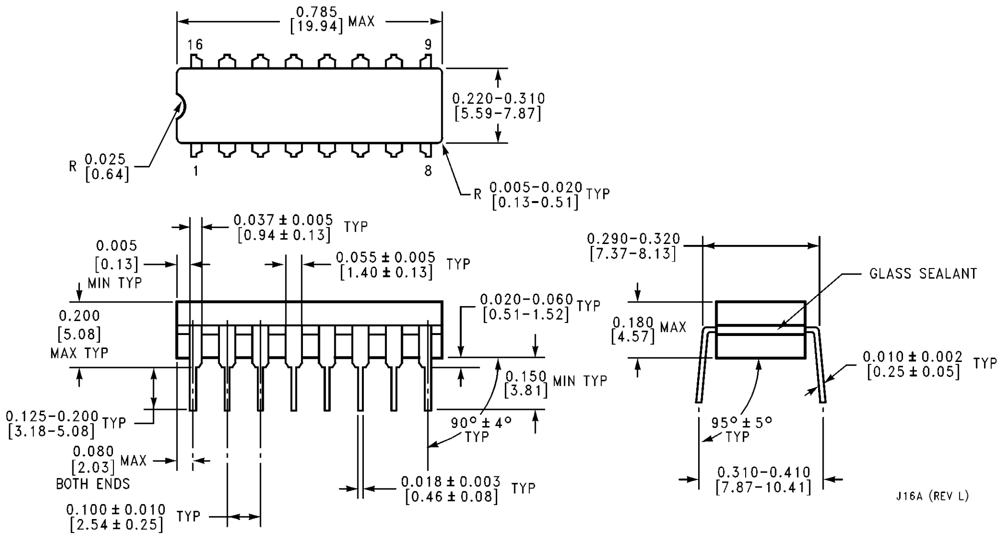
at V_{CC} = 5V and T_A = 25°C:

Symbol	Parameter	C_L = 15 pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to $\overline{a}$–$\overline{g}$		100 100	ns ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{RBI}$ to $\overline{a}$–$\overline{g}$		100 100	ns ns

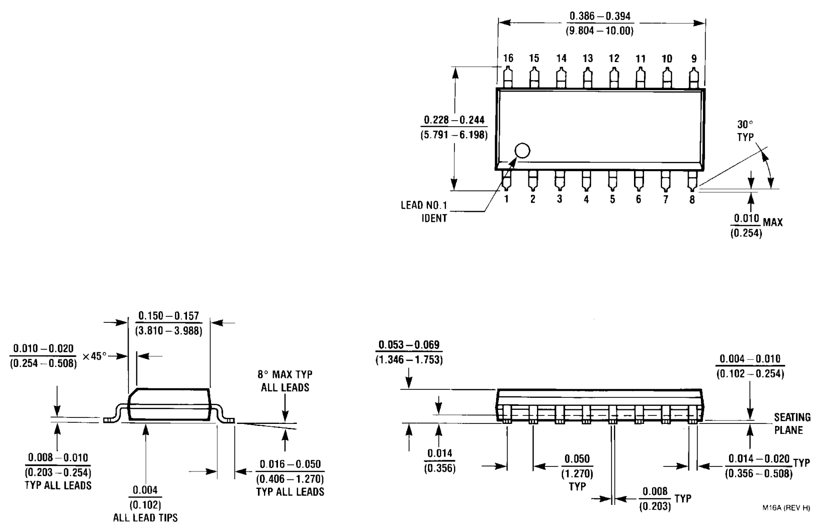
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Physical Dimensions inches (millimeters)

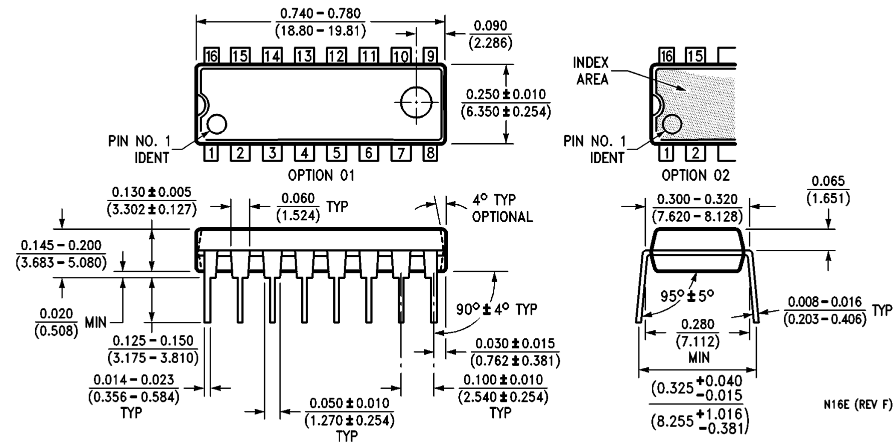


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS347J
NS Package Number J16A

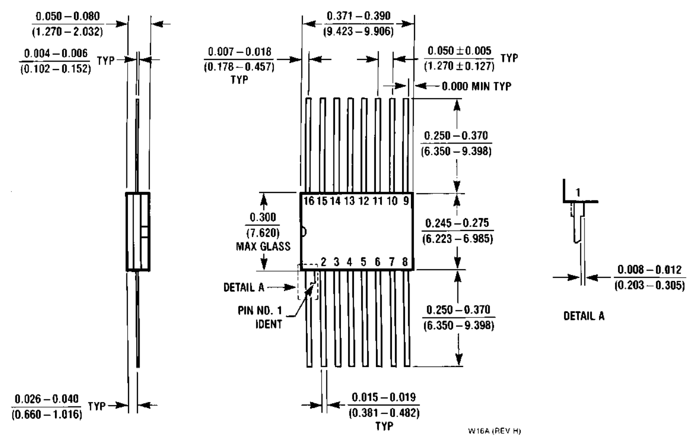


16-Lead Small Outline Molded Package (M)
Order Number DM74LS347M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS347N
NS Package Number N16E



16-Lead Ceramic Flat Package (W)
Order Number DM54LS347W
NS Package Number W16A

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National Semiconductor

June 1989

54LS352/DM74LS352 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

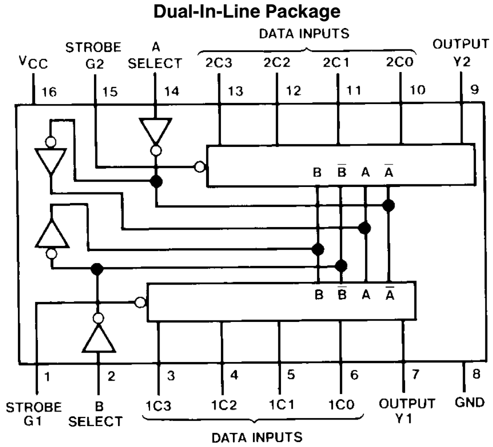
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Inverting version of DM54/74LS153
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 15 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

Connection Diagram

Dual-In-Line Package



TL/F/6425–1

Order Number 54LS352DMQB, 54LS352FMQB, DM74LS352M or DM74LS352N
See NS Package Number J16A, M16A, N16E or W16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	**A**	**C0**	**C1**	**C2**	**C3**	**G**	**Y**
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care

 TL/F/6425

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55° C to +125°C
DM74LS	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS352			DM74LS352			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			12			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V	54LS			0.1	mA
		V_{CC} = Max, V_I = 7V	DM74				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

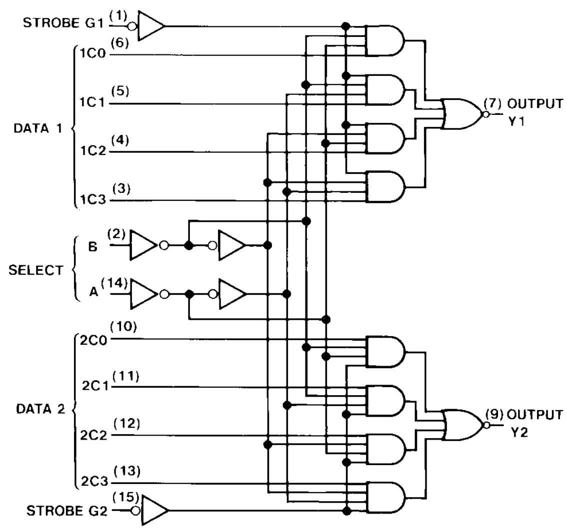
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs at ground.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

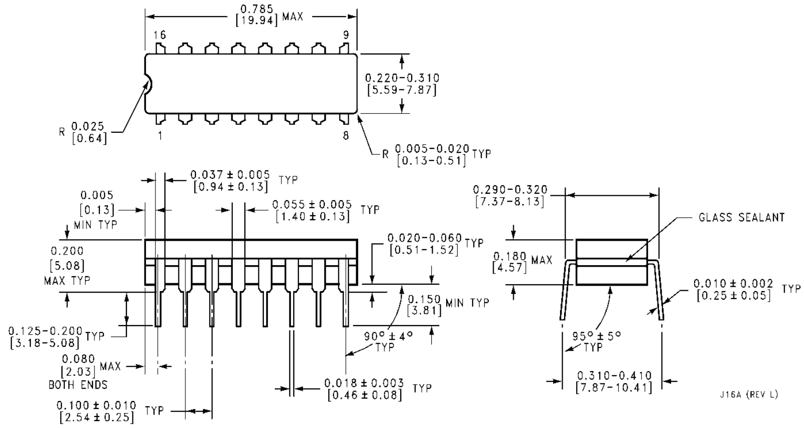
Symbol	Parameter	From (Input) To (Output)	54LS		DM74LS		Units
			$C_L = 15$ pF		$C_L = 50$ pF, $R_L = 2$ kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		12		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		12		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		22		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		15		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		20		41	ns

Logic Diagram

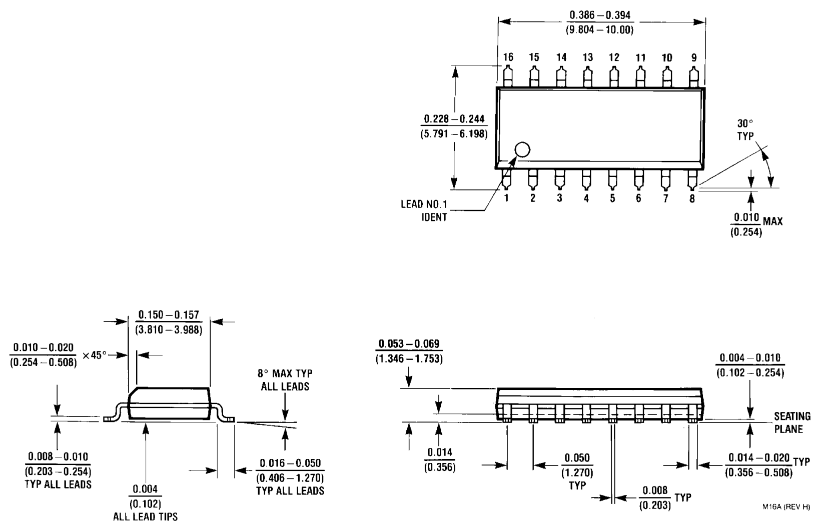


TL/F/6425–2

Physical Dimensions inches (millimeters)

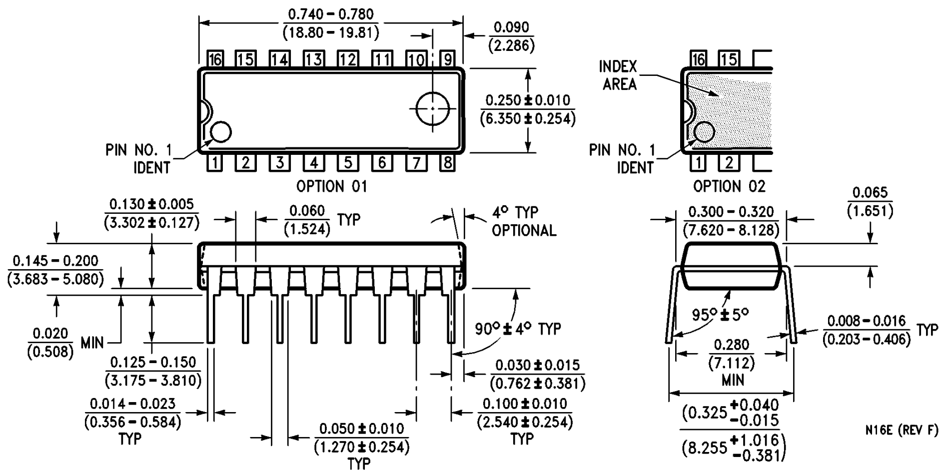


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS352DMQB
NS Package Number J16A



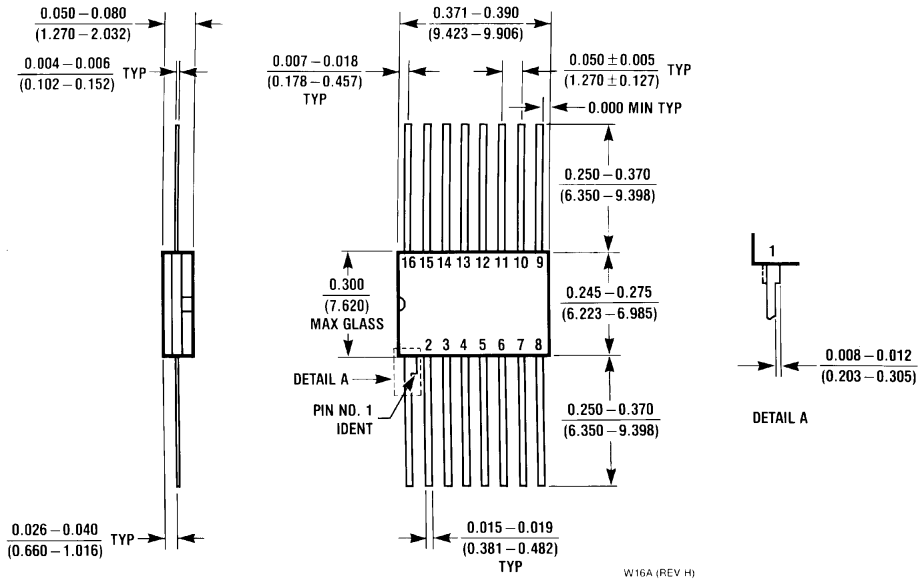
16-Lead Small Outline Molded Package (M)
Order Number DM74LS352M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS352N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS352FMQB
NS Package Number W16A

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National Semiconductor

February 1992

DM74LS353
Dual 4-Input Multiplexer with TRI-STATE® Outputs

General Description

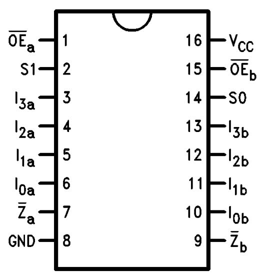
The '353 is a dual 4-input multiplexer with TRI-STATE outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all National TTL families.

Features

- Inverted version of 'LS253
- Schottky process for high speed
- Multifunction capability

Connection Diagram

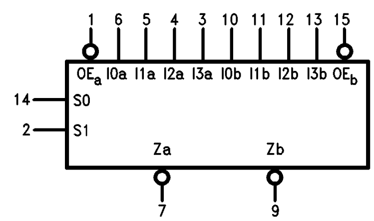
Dual-In-Line Package



TL/F/10185–1

Order Number DM74LS353M or DM74LS353N
See NS Package Number M16A or N16E

Logic Symbol



TL/F/10185–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
I0a–I3a	Side A Data Inputs
I0b–I3b	Side B Data Inputs
S0, S1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input (Active Low)
$\overline{OE}_b$	Side B Output Enable Input (Active Low)
$\overline{Z}_a$, $\overline{Z}_b$	TRI-STATE Outputs (Inverted)

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−2.6	mA
I_{OL}	Low Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	2.7			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−30		−130	mA
I_{CCL}	Supply Current Outputs HIGH	V_{CC} = Max, In, Sn, $\overline{OE}$n = GND			12	mA
I_{CCZ}	Supply Current Outputs OFF	V_{CC} = Max, $\overline{OE}$n = 4.5V In, Sn = GND			14	mA
I_{OZH}	TRI-STATE Output OFF Current HIGH	V_{CC} = V_{CCH} V_{OZH} = 2.7V			20	μA
I_{OZL}	TRI-STATE Output OFF Current LOW	V_{CC} = V_{CCH} V_{OZL} = 0.4V			−20	μA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 50\ pF$		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Sn to $\overline{Z}$n		24 32	ns
t_{PLH} t_{PHL}	Propagation Delay In to $\overline{Z}$n		15 15	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Zn		18 18	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Zn		18 18	ns

Functional Description

The 'LS353 contains two identical 4-input multiplexers with TRI-STATE outputs. They select two bits from four sources selected by common Select inputs (S0, S1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$), $\overline{OE}_b$) inputs which when HIGH, force the outputs to a high impedance (high Z) state. The logic equations for the outputs are shown below:

If the outputs of TRI-STATE devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so that there is no overlap.

$$\overline{Z_a} = \overline{\overline{OEa} \bullet (I0a \bullet \overline{S1} \bullet \overline{S0} + I1a \bullet \overline{S1} \bullet S0 + I2a \bullet S1 \bullet \overline{S0} + I3a \bullet S1 \bullet S0)}$$

$$\overline{Z_b} = \overline{\overline{OE_b} \bullet (I0b \bullet \overline{S1} \bullet \overline{S0} + I1b \bullet \overline{S1} \bullet S0 + I2b \bullet S1 \bullet \overline{S0} + I3b \bullet S1 \bullet S0)}$$

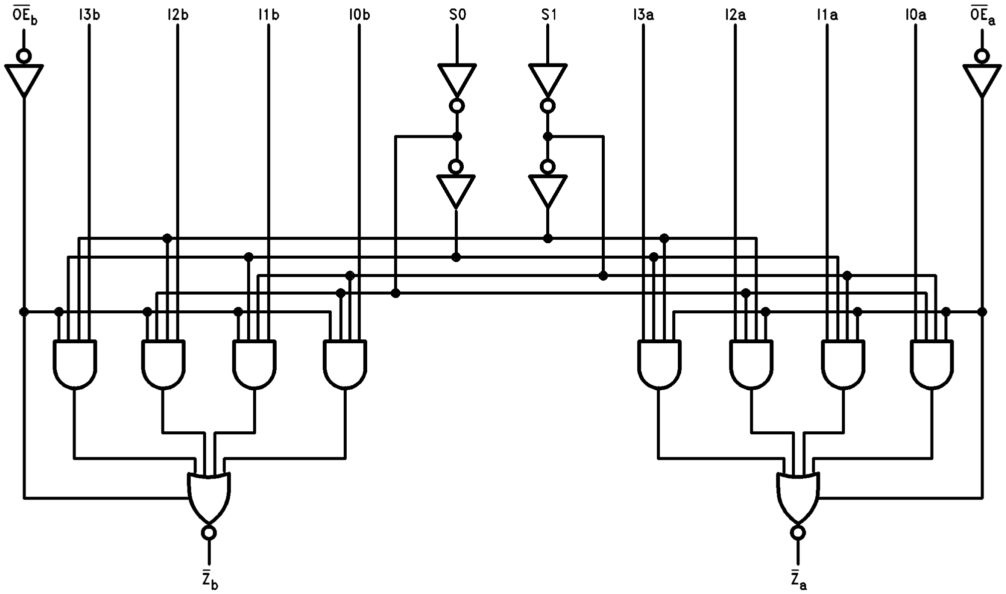
Truth Table

Select Inputs		Data Inputs				Output Enable	Output
S0	S1	I0	I1	I2	I3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs S0 and S1 are common to both sections.

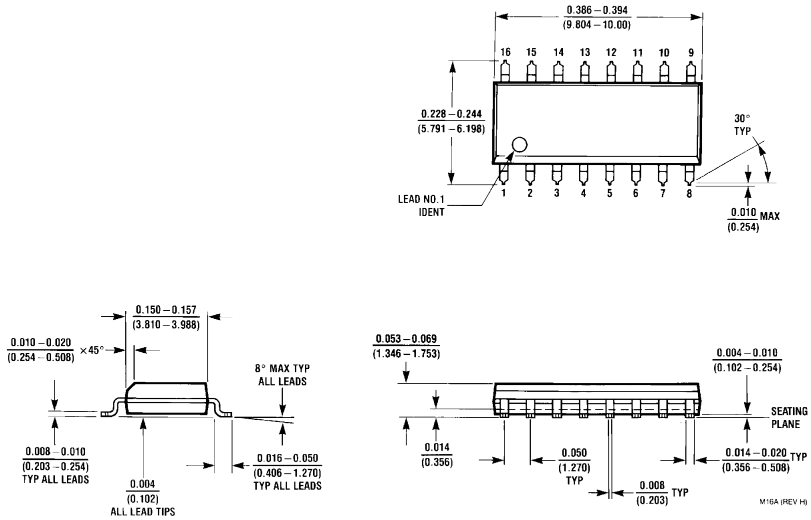
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
(Z) = High Impedance

Logic Diagram



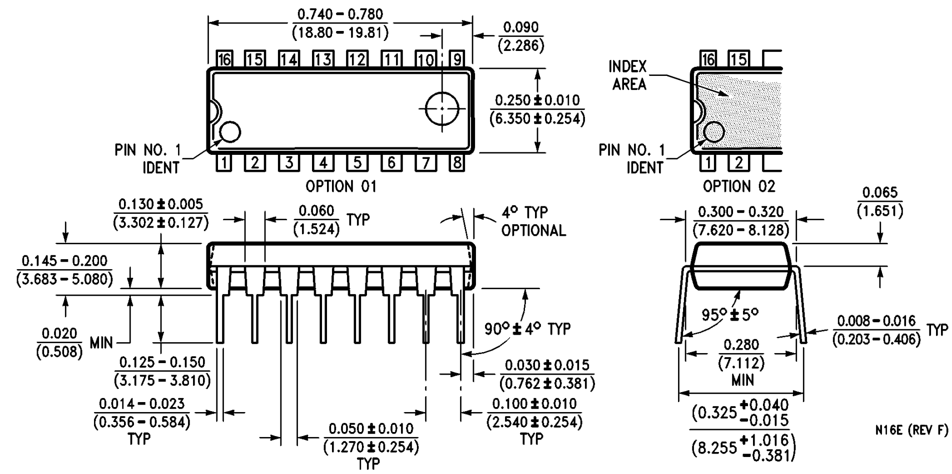
TL/F/10185–3

Physical Dimensions inches (millimeters)



16-Lead Small Outline Molded Package (M)
Order Number DM74LS353M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS353N
NS Package Number N16E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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FAIRCHILD
SEMICONDUCTOR™

March 1998

DM74LS365A
Hex 3-STATE Buffers

General Description

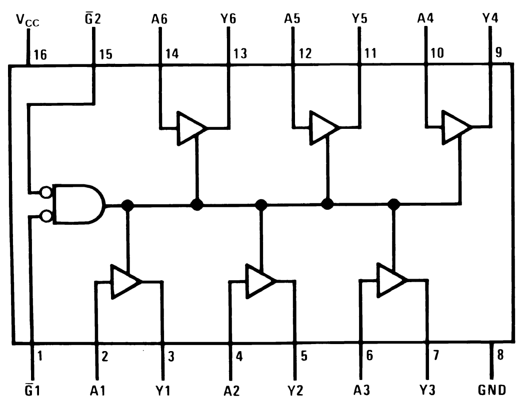
This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS365A) is available. Contact a Fairchild Semiconductor Sales Office/Distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006427-1

Order Number 54LS365ADMQB, 54LS365AFMQB, 54LS365ALMQB, DM54LS365AJ, DM54LS365AW, DM74LS265AM or DM74LS365AN
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Y = A

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS365A			DM74LS365A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 5)	A Input			−20	µA
		V_{CC} = Max, V_I = 0.4V (Note 6)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			14	24	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 5: Both $\overline{G}$ inputs are at 2V.

Note 6: Both $\overline{G}$ inputs at 0.4V.

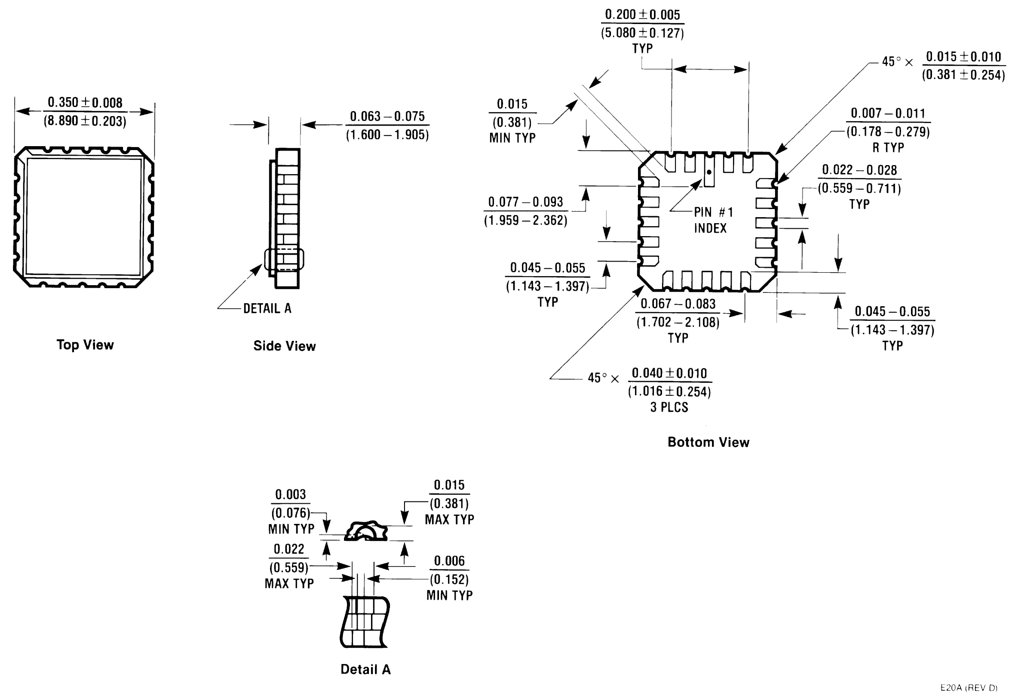
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

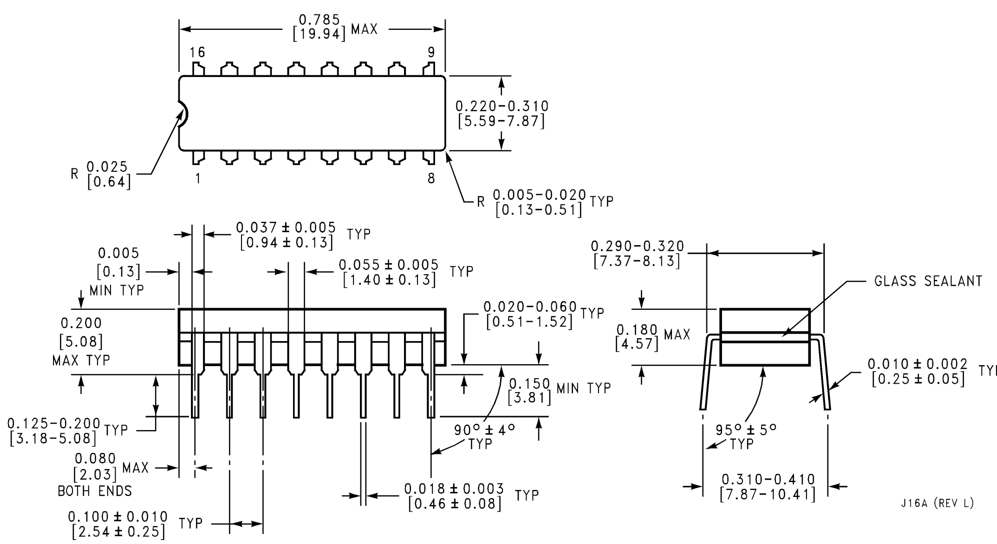
Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 7)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 7)		20			ns

Note 7: C_L = 5 pF.

Physical Dimensions inches (millimeters) unless otherwise noted

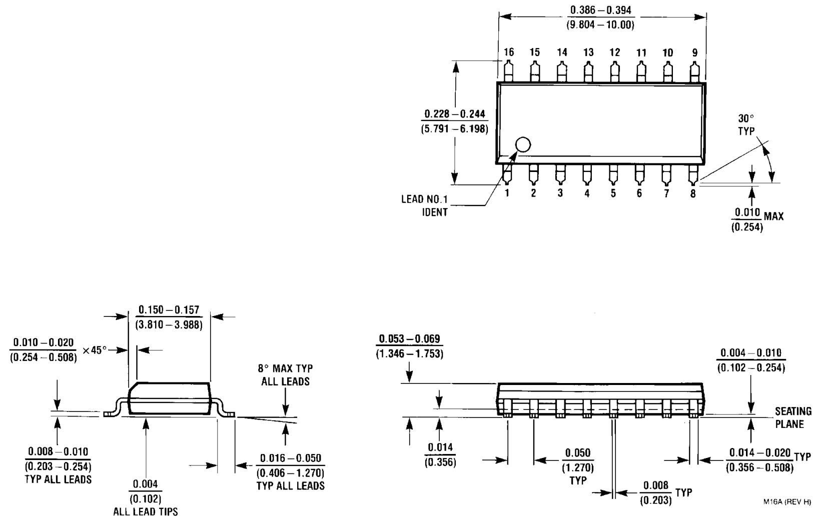


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS365ALMQB
Package Number E20A

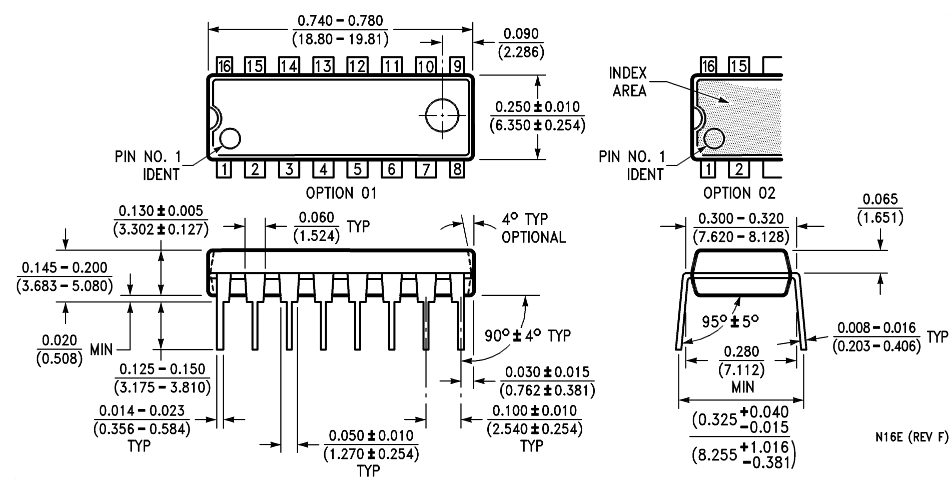


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS365ADMQB or DM54LS365AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

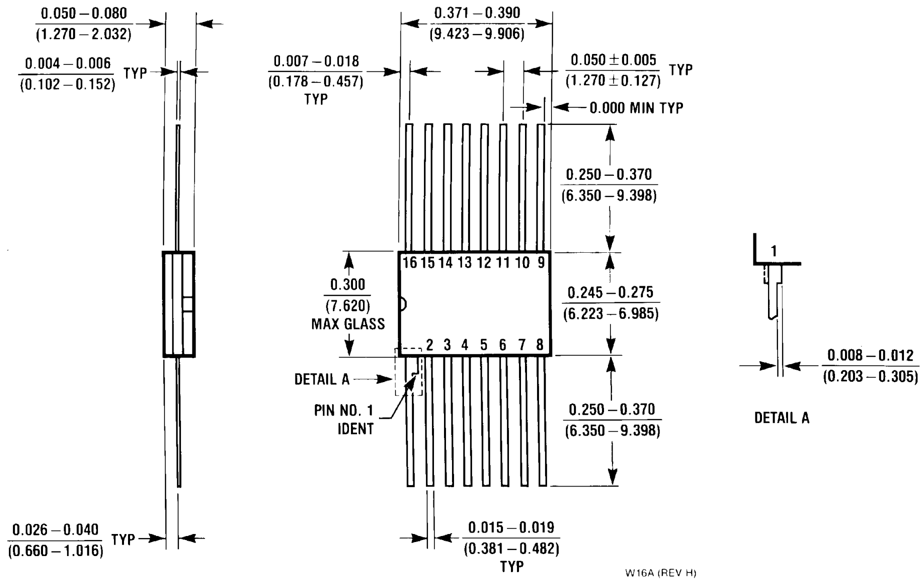


16-Lead Small Outline Molded Package (M)
Order Number DM74LS365AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS365AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS365AFMQB or DM54LS365AW
Package Number W16A

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March 1998

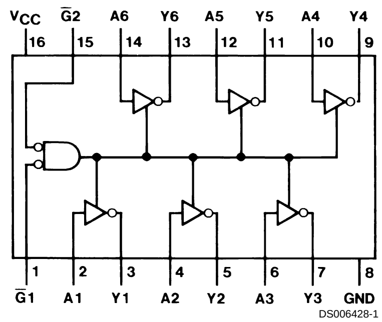
DM74LS366A
Hex 3-STATE Inverting Buffer

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



Order Number DM54LS366AJ, DM54LS366AW, DM54LS366AE, DM74LS366AM or DM74LS366AN
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

$Y = \overline{A}$

Inputs			Output
$\overline{G}$ 1	$\overline{G}$ 2	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS366A			DM74LS366A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 5)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 6)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−30		−130	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			12	21	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 5: Both $\overline{G}$ inputs are at 2V.

Note 6: Both $\overline{G}$ inputs at 0.4V.

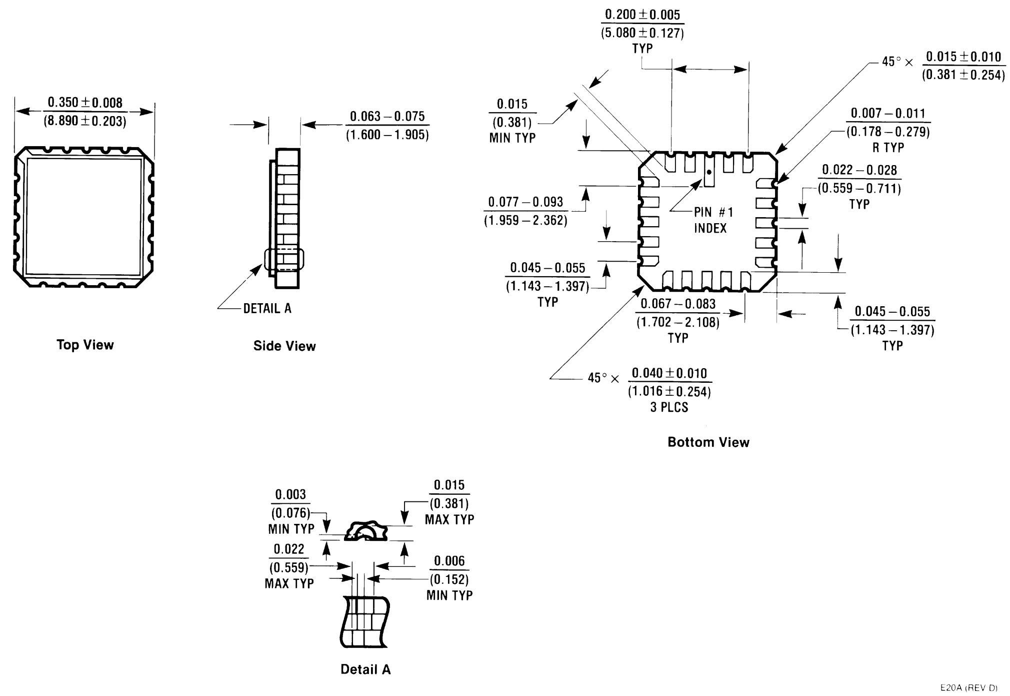
Switching Characteristics:

for test waveforms and output load. V_{CC} = 5V, T_A = 25˚C

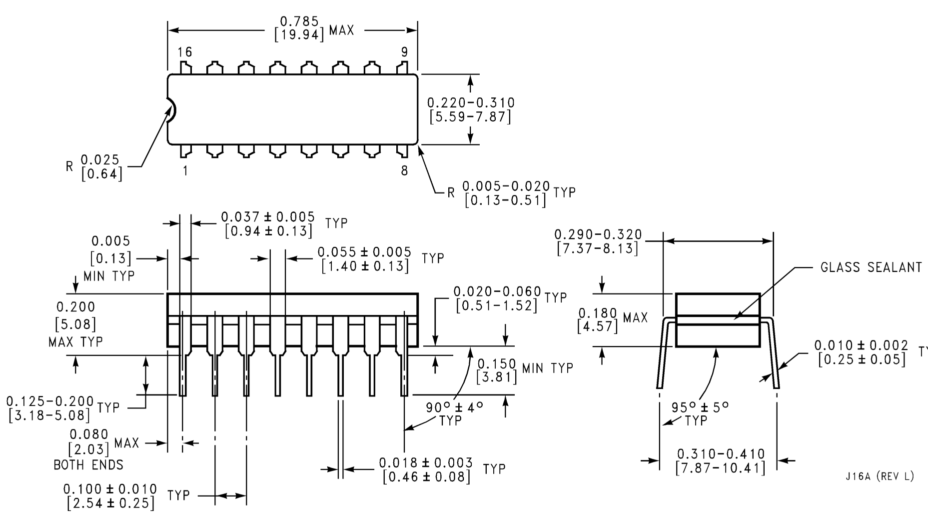
Symbol	Parameter	DM54LS		DM74LS				Units
		C_L = 50 pF		R_L = 667Ω				
				C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		12		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		24		30		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 7)		25		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 7)		20		20			ns

Note 7: C_L = 5 pF.

Physical Dimensions inches (millimeters) unless otherwise noted

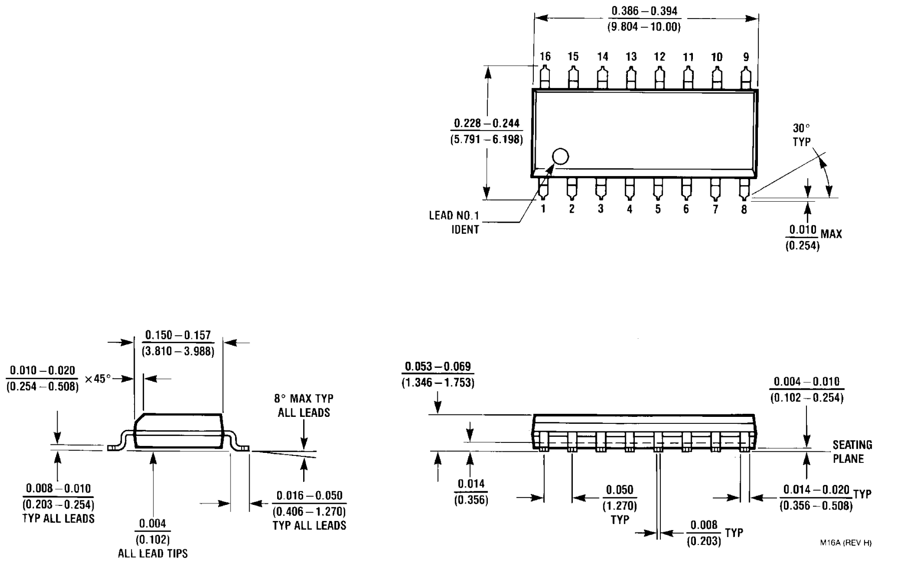


Ceramic Leadless Chip Carrier Package (E)
Order Number DM54LS366AE
Package Number E20A

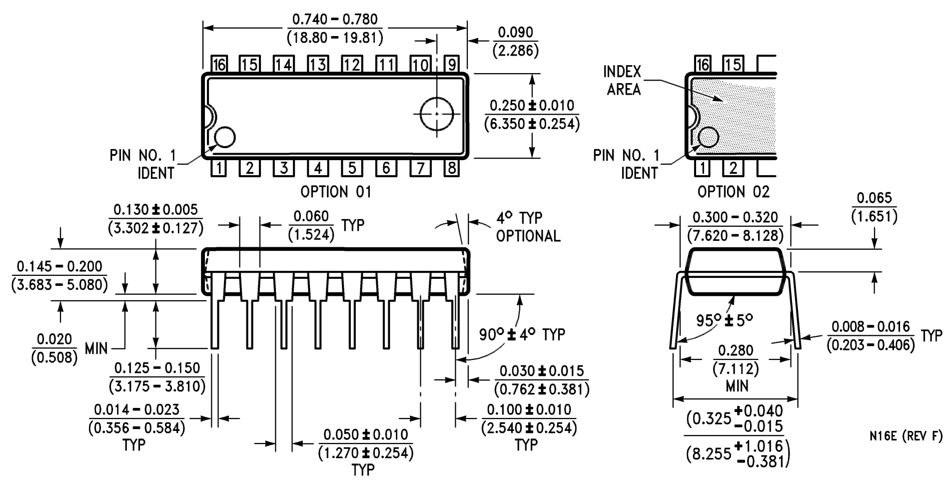


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS366AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

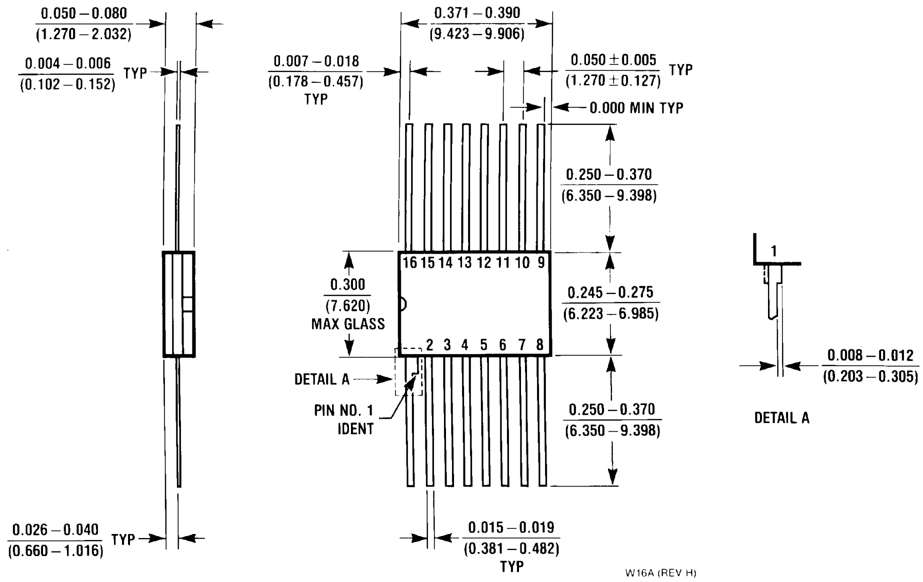


16-Lead Small Outline Molded Package (M)
Order Number DM74LS366AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS366AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS366AW
Package Number W16A

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March 1998

DM74LS367A
Hex 3-STATE Buffers

General Description

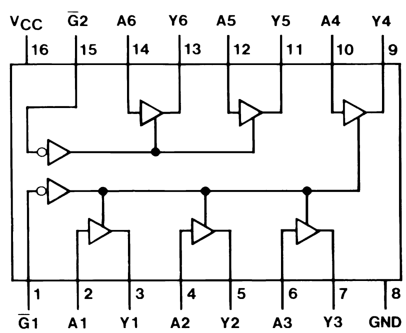
This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the 3-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate military/aerospace device (54LS367A) is available. Contact a Fairchild Semiconductor sales office/distributor for specifications.

Connection Diagram

Dual-In-Line Package



DS006429-1

Order Number 54LS367ADMQB, 54LS367AFMQB, 54LS367ALMQB, DM54LS367AJ, DM54LS367AW, DM74LS367AM or DM74LS367AN
See Package Number E20A, J16A, M16A, N16E or W16A

Function Table

Y = A

Inputs		Output
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = 3-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C
Storage Temperature Range	−65˚C to +150˚C

Recommended Operating Conditions

Symbol	Parameter	DM54LS367A			DM74LS367A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 5)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 6)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			14	24	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 5: Both $\overline{G}$ inputs are at 2V.

Note 6: Both $\overline{G}$ inputs at 0.4V.

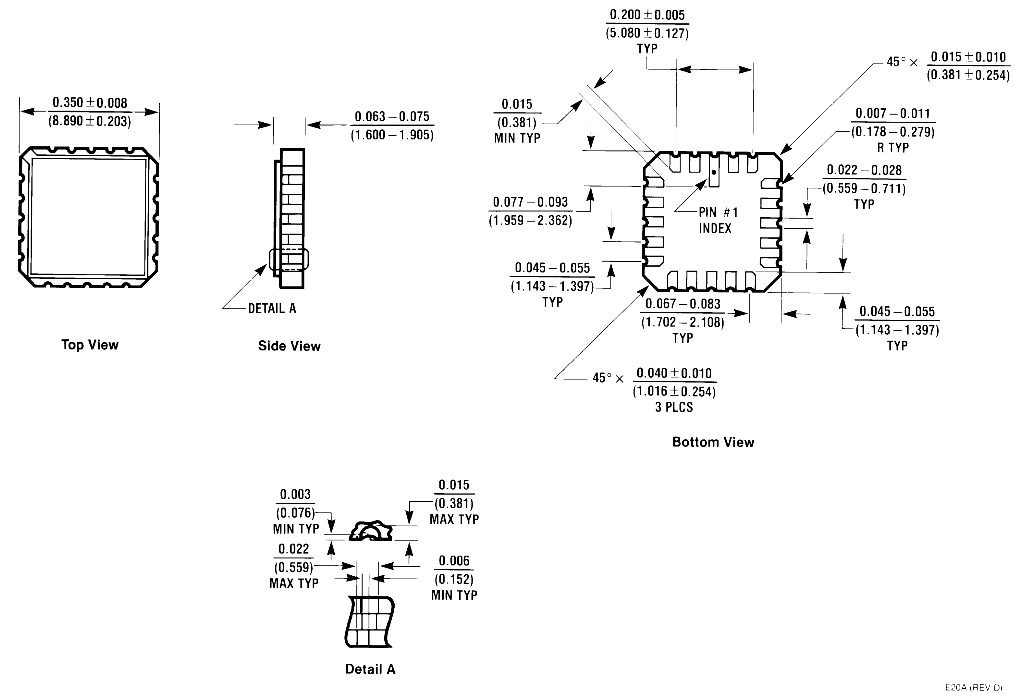
Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

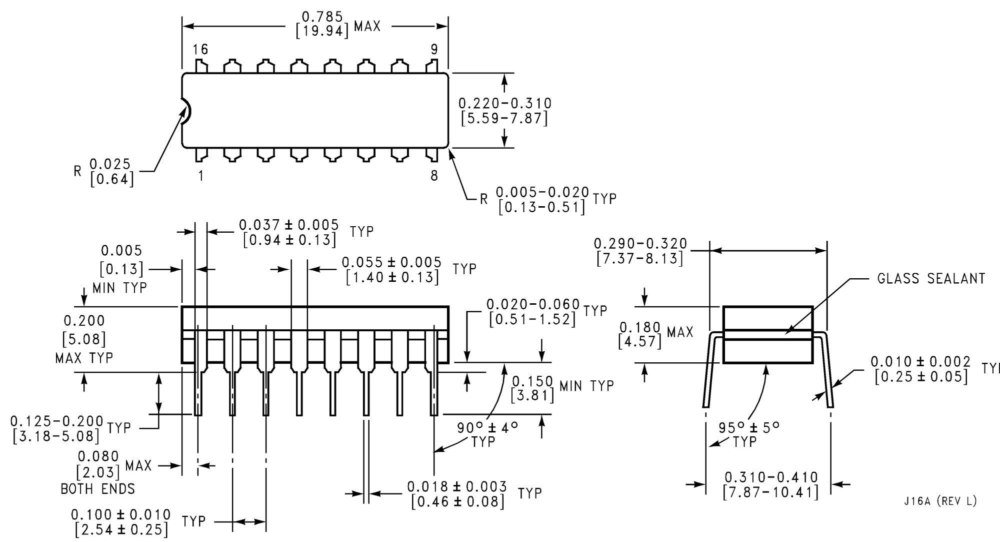
Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 7)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 7)		20			ns

Note 7: C_L = 5 pF.

Physical Dimensions inches (millimeters) unless otherwise noted

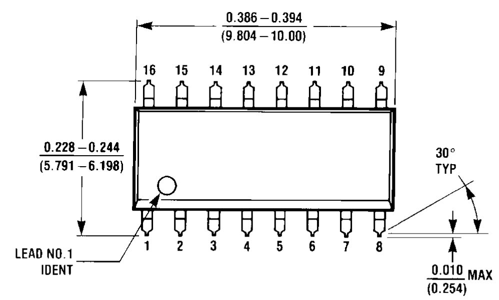


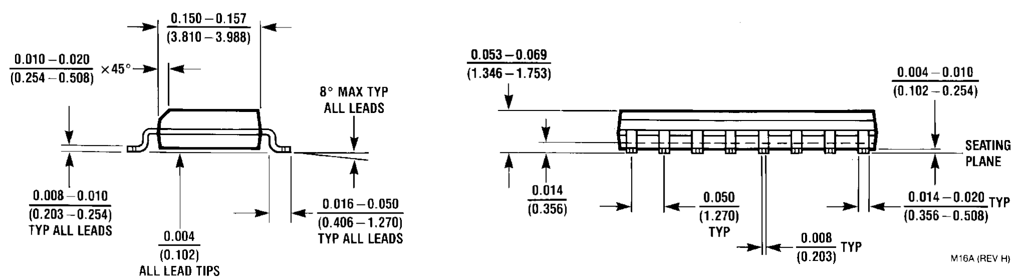
Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS367ALMQB
Package Number E20A



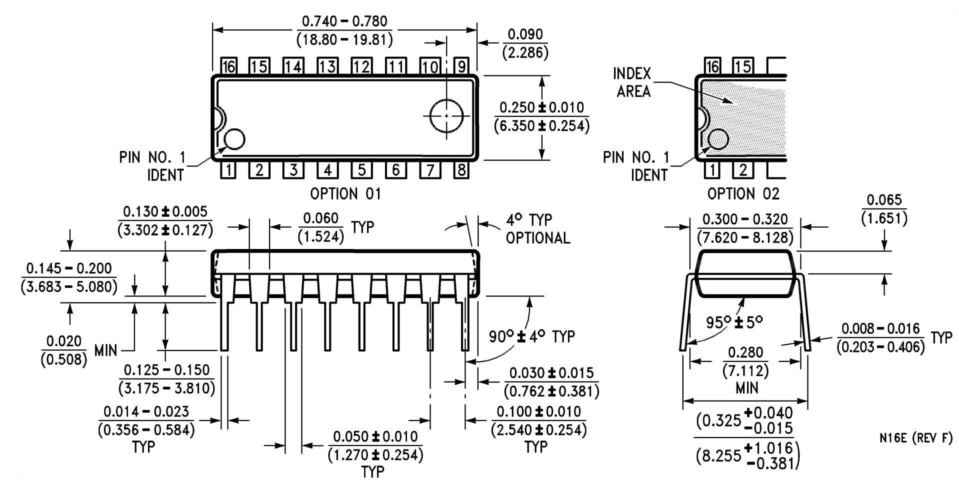
Ceramic Dual-In-Line Package (J)
Order Number 54LS367ADMQB or DM54LS367AJ
Package Number J16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



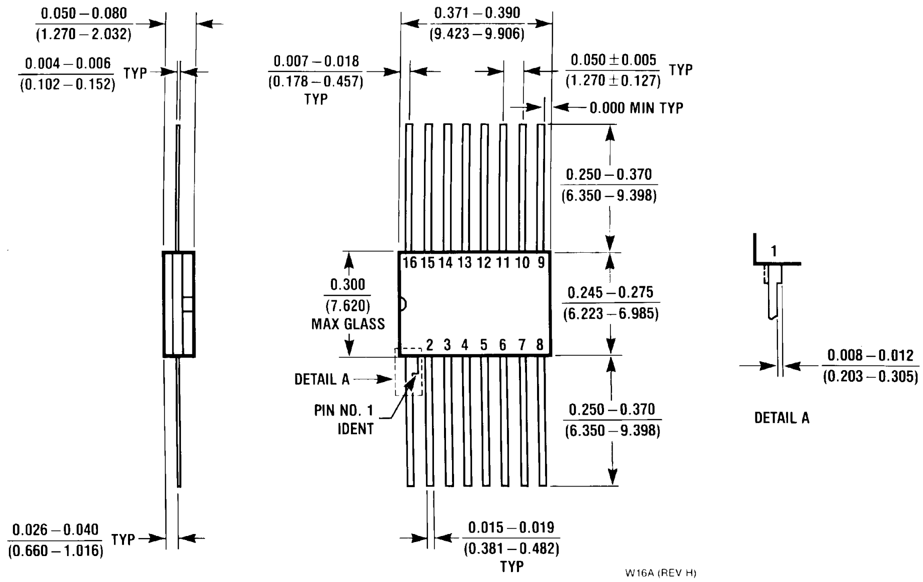


16-Lead Small Outline Molded Package (M)
Order Number DM74LS367AM
Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS367AN
Package Number N16E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS367AFMQB or DM54LS367AW
Package Number W16A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

May 1989

54LS368A/DM54LS368A/DM74LS368A Hex TRI-STATE® Inverting Buffers

General Description

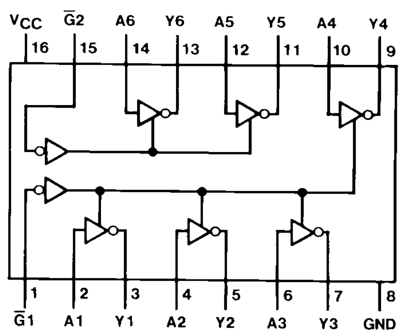
This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Features

- Alternate Military/Aerospace device (54LS368) is available. Contact a National Semiconductor Sales Office/ Distributor for specifications.

Connection Diagram

Dual-In-Line Package



TL/F/6430–1

Order Number 54LS368ADMQB, 54LS368AFMQB, 54LS368ALMQB, DM54LS368AJ, DM54LS368AW, DM74LS368AM or DM74LS368AN
See NS Package Number E20A, J16A, M16A, N16E or W16A

Function Table

$Y = \overline{A}$

Inputs		Output
A	$\overline{G}$	Y
L	L	H
H	L	L
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS and 54LS	$-55°C$ to $+125°C$
DM74LS	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS368A			DM74LS368A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			-1			-2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = -18 mA				-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			-20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			-0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			-0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				-20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	-20		-100	mA
			DM74	-20		-100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

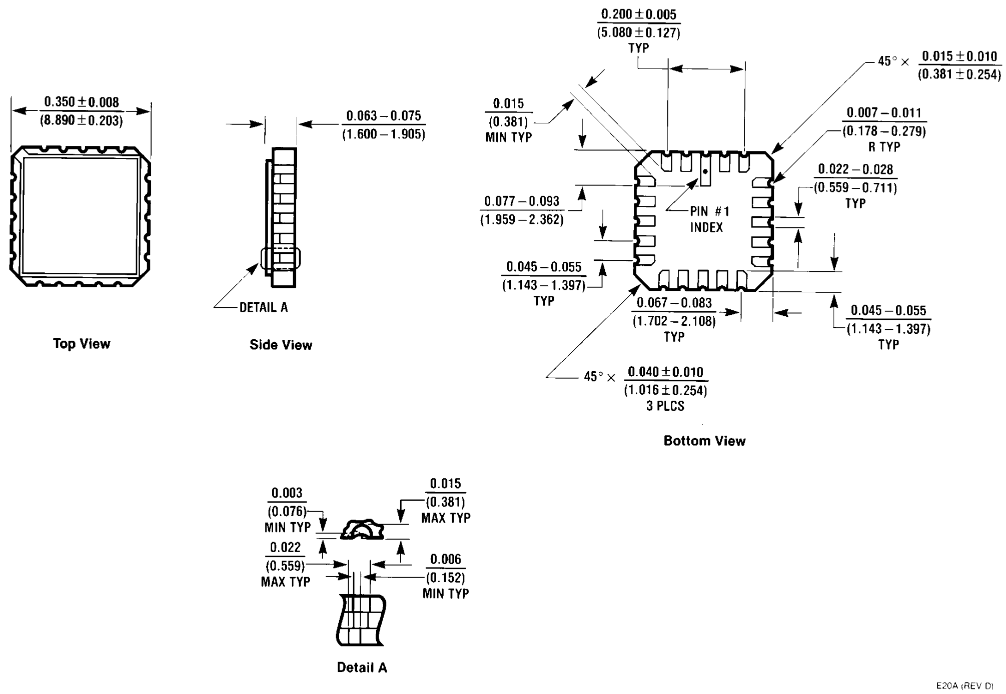
Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$ (See Section 1 for Test Waveforms and Output Load)

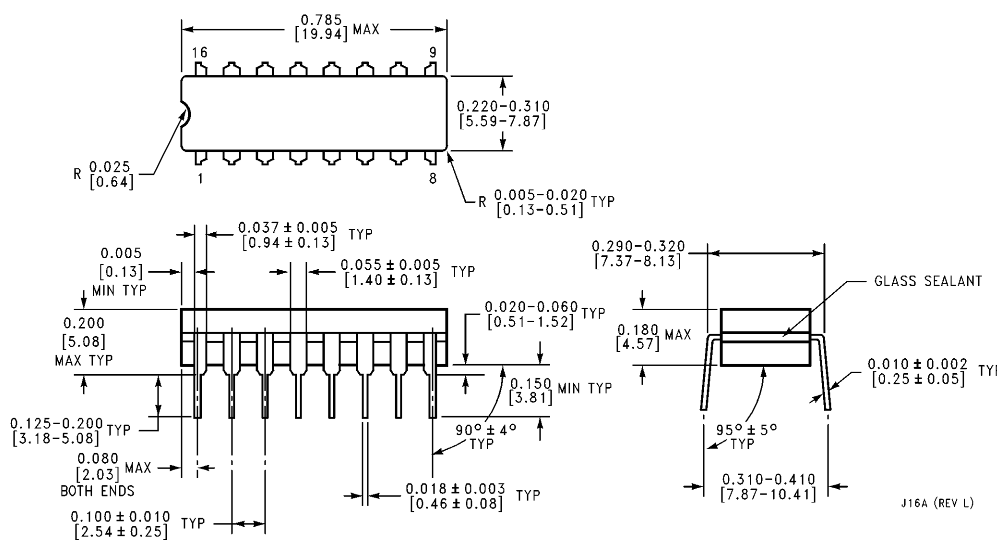
Symbol	Parameter	$R_L = 667\Omega$				Units
		$C_L = 50$ pF		$C_L = 150$ pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: $C_L = 5$ pF.

Physical Dimensions inches (millimeters)

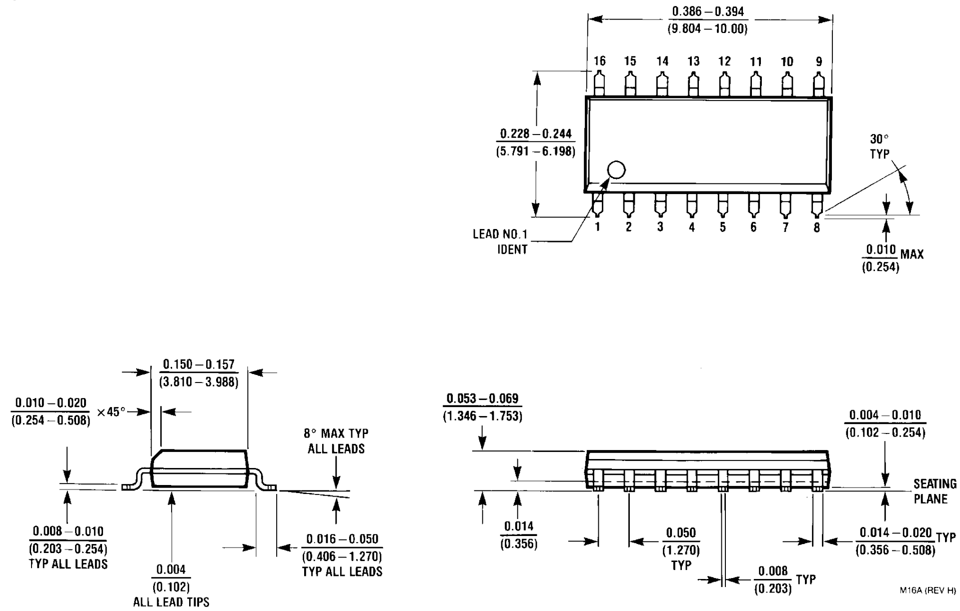


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS368ALMQB
NS Package Number E20A

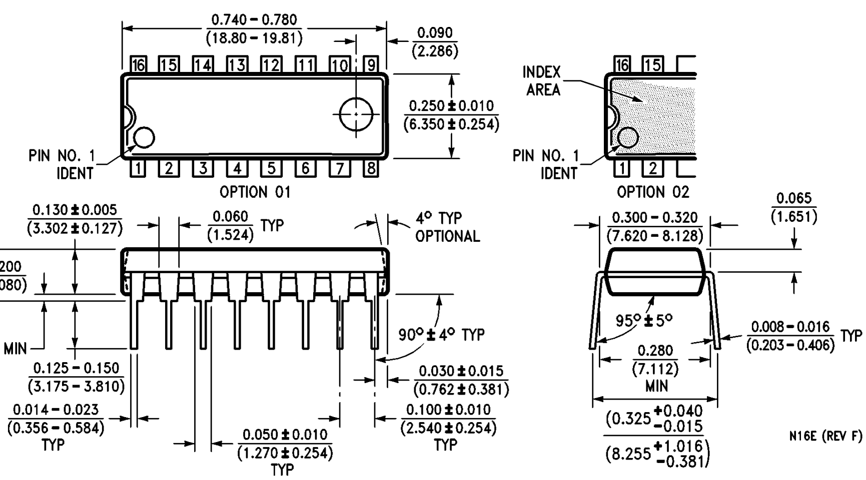


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS368ADMQB or DM54LS368AJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

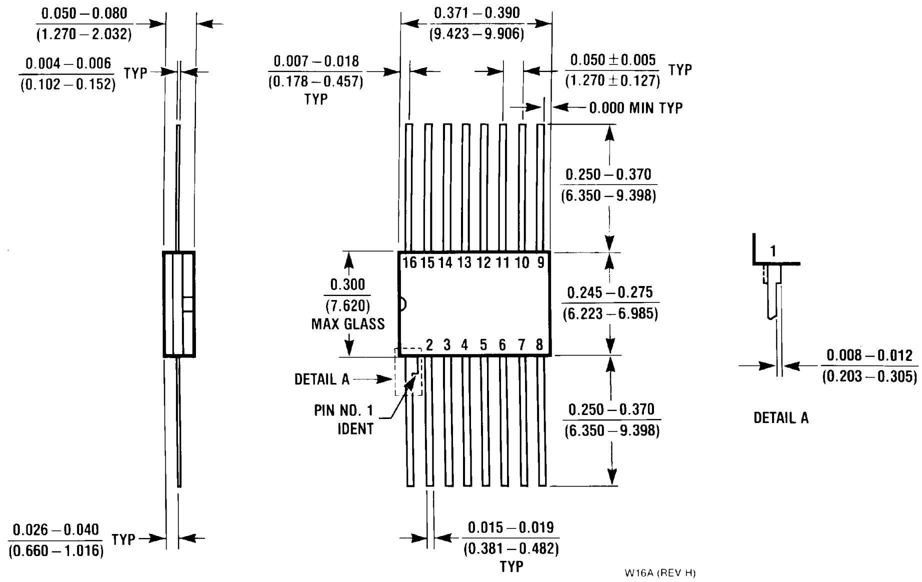


16-Lead Small Outline Molded Package (M)
Order Number DM74LS368AM
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS368AN
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54LS368AFMQB or DM54LS368AW
NS Package Number W16A

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FAIRCHILD
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March 1998

DM74LS373/DM74LS374 3-STATE Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole 3-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

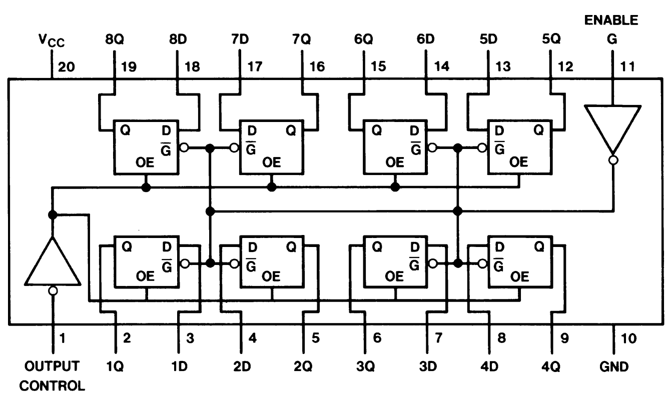
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- 3-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- P-N-P inputs reduce D-C loading on data lines

Connection Diagrams

Dual-In-Line Packages
'LS373

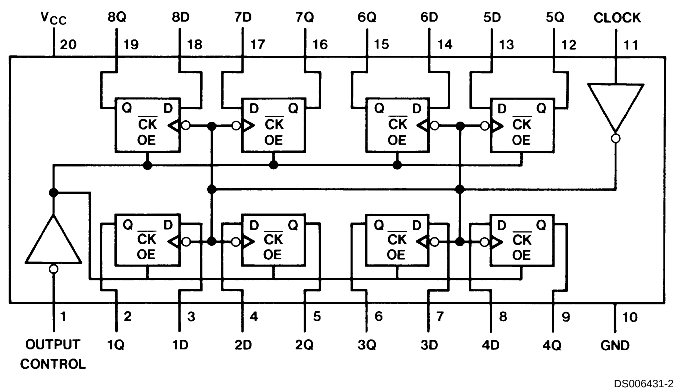


DS006431-1

Order Number DM54LS373J, DM54LS373W, DM74LS373N or DM74LS373WM
See Package Number J20A, M20B, N20A or W20A

Connection Diagrams (Continued)

'LS374



Order Number DM54LS374J, DM54LS374W, DM74LS374WM or DM74LS374N
See Package Number J20A, M20B, N20A or W20A

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

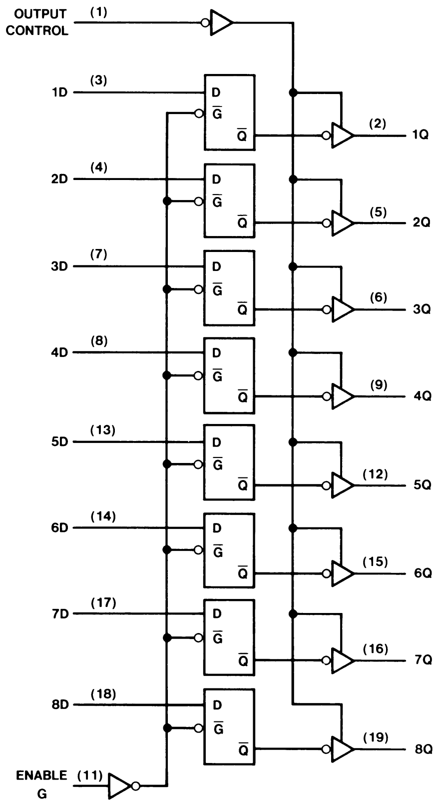
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

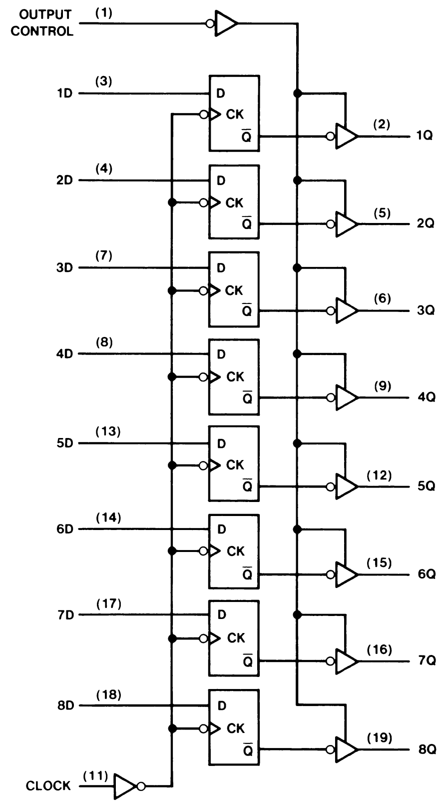
Logic Diagrams

DM54/74LS334
Transparent Latches



DS006431-3

DM54/74LS374
Positive-Edge-Triggered Flip-Flops



DS006431-4

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65˚C to +150˚C
Operating Free Air Temperature Range	
DM54LS	−55˚C to +125˚C
DM74LS	0˚C to +70˚C

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Votage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width (Note 3)	Enable High	15			15			ns
		Enable Low	15			15			
t_{SU}	Data Setup Time (Notes 2, 3)		5↓			5↓			ns
t_H	Data Hold Time (Notes 2, 3)		20↓			20↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	˚C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 3: T_A = 25˚C and V_{CC} = 5V.

'LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−50		−225	

’LS373 Electrical Characteristics (Continued)

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{CC}	Supply Current	V_{CC} = Max, OC = 4.5V, D_n, Enable = GND		24	40	mA

’LS373 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		18		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		30		36	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		28		36	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		36		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)	Output Control to Any Q		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)	Output Control to Any Q		25			ns

Note 4: All typicals are at V_{CC} = 5V, T_A = 25˚C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS374			DM74LS374			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA

Recommended Operating Conditions (Continued)

Symbol	Parameter		DM54LS374			DM74LS374			Units
			Min	Nom	Max	Min	Nom	Max	
t_W	Pulse Width	Clock High	15			15			ns
	(Note 8)	Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 7, 8)		20↑			20↑			ns
t_H	Data Hold Time (Notes 7, 8)		1↑			1↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 7: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 8: T_A = 25°C and V_{CC} = 5V.

’LS374 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 9)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min I_{OH} = Max V_{IL} = Max V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 10)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CC}	Supply Current	V_{CC} = Max, D_n = GND, OC = 4.5V			27	45	mA

’LS374 Switching Characteristics

at V_{CC} = 5V and T_A = 25˚C

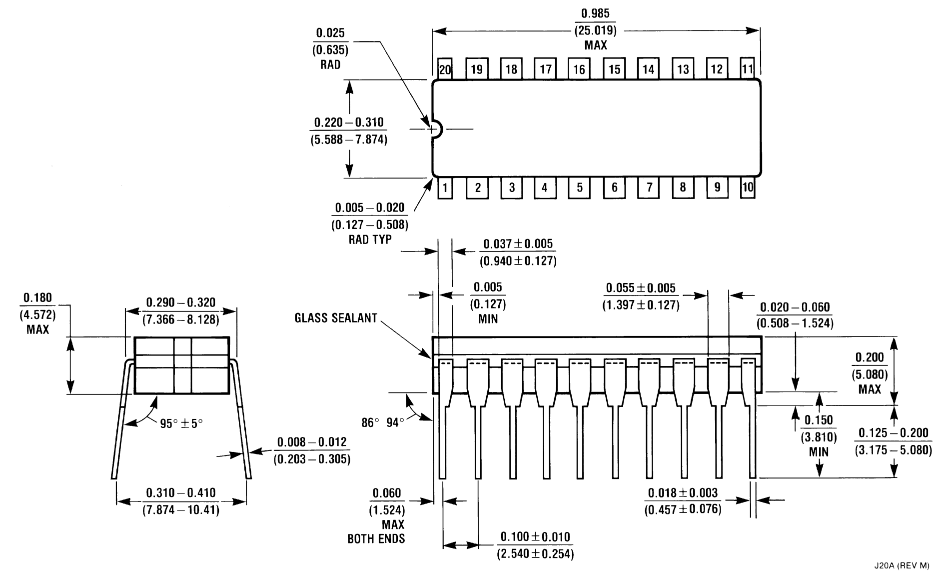
Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	35		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		28		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		38	ns
t_{PZH}	Output Enable Time to High Level Output		28		44	ns
t_{PZL}	Output Enable Time to Low Level Output		28		44	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 11)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 11)		25			ns

Note 9: All typicals are at V_{CC} = 5V, T_A = 25˚C.

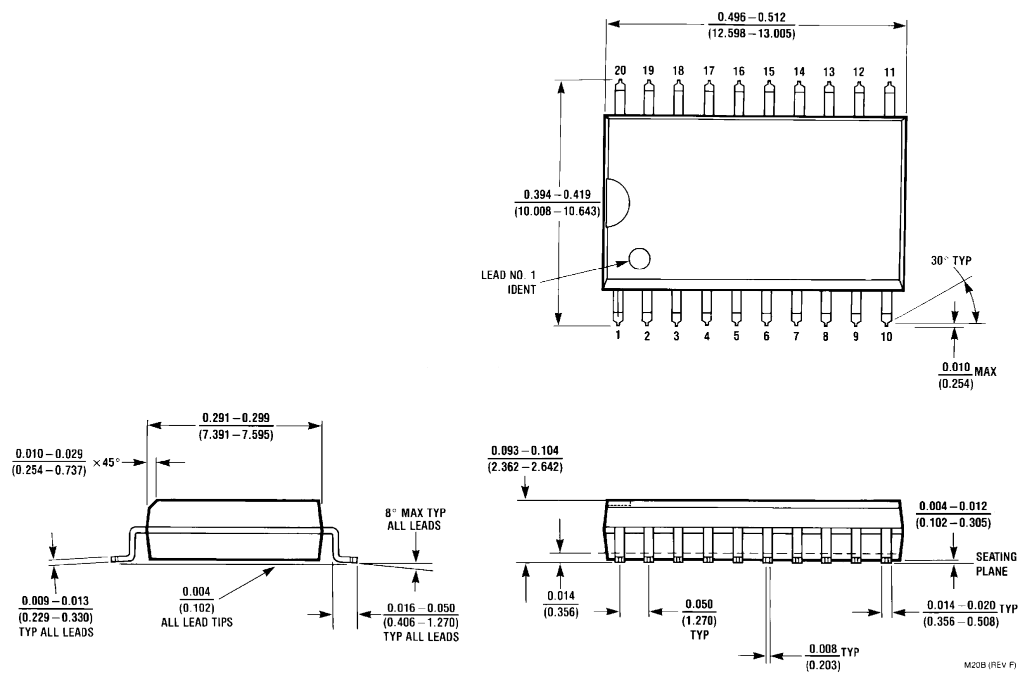
Note 10: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 11: C_L = 5 pF.

Physical Dimensions inches (millimeters) unless otherwise noted

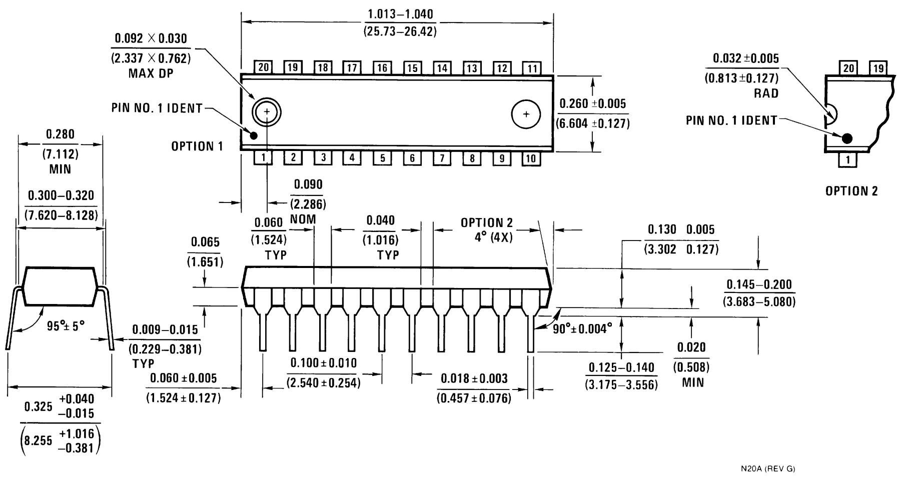


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS373J or DM54LS374J
Package Number J20A

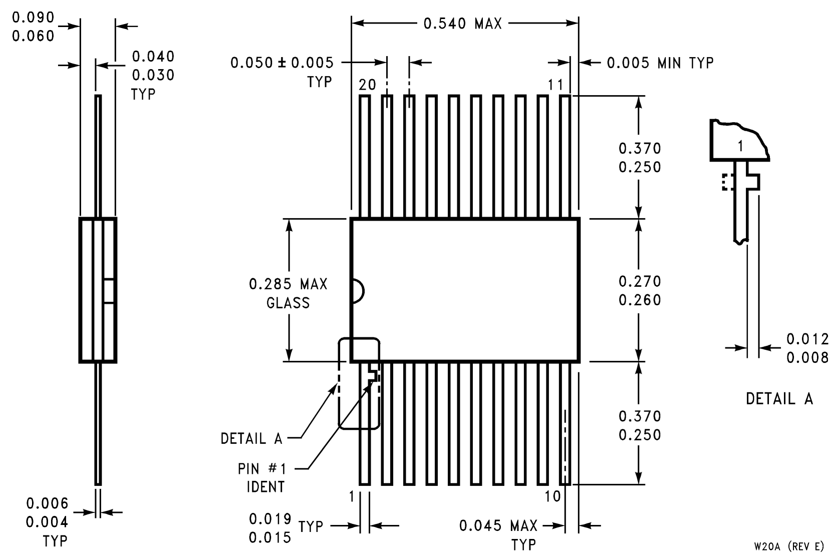


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS373WM or DM74LS374WM
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS373N and DM74LS374N
Package Number N20A



20-Lead Ceramic Flat Package (W)
Order Number DM54LS373W or DM54LS374W
Package Number W20A

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National Semiconductor

February 1992

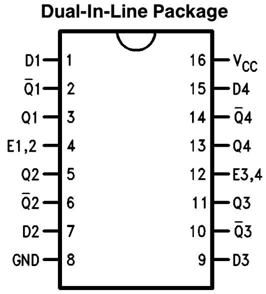
DM74LS375 4-Bit Latch

General Description

The 'LS375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The 'LS375 is functionally identical to the 'LS75 except for the corner power pins.

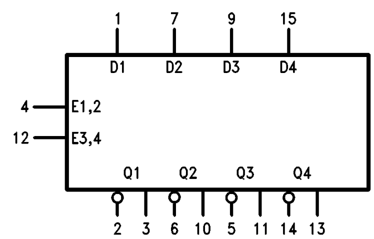
Connection Diagram

Dual-In-Line Package



TL/F/9830–1

Logic Symbol



TL/F/9830–2

V_{CC} = Pin 16
GND = Pin 8

Order Number DM74LS375M or DM74LS375N
See NS Package Number M16A or N16E

Pin Name	Description
D1–D4	Data Inputs
E1, 2	Latches 1, 2 Enable Inputs
E3, 4	Latches 3, 4 Enable Inputs
Q1–Q4	Latch Outputs
$\overline{Q}$1–Q4	Complementary Latch Outputs

 RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−0.4	mA
I_{OL}	Low Level Output Current			8	mA
T_A	Free Air Operating Temperature	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to E_n	20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to E_n	0			ns
t_w (H)	E_n Pulse Width HIGH	20			ns

Electrical Characteristics

Over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.35	0.5	V
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Others			0.1	mA
			Enable Input			0.4	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Others			20	μA
			Enable Input			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Others			−0.4	mA
			Enable Input			−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max				12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

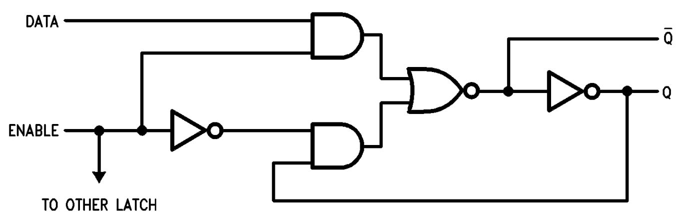
Symbol	Parameter	$C_L = 15$ pF		Units
		Min	Max	
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		27 23	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{Q}_n$		20 15	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to Q_n		27 25	ns
t_{PLH} t_{PHL}	Propagation Delay E_n to $\overline{Q}_n$		30 18	ns

Truth Table (Each Latch)

t_n	t_{n+1}
D	Q
H L	H L

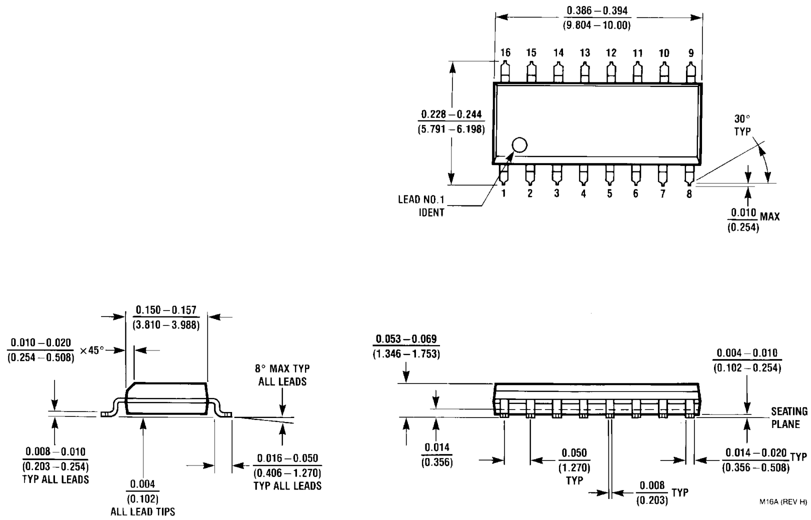
t_n = Bit time before Enable negative going transition.
t_{n+1} = Bit time after Enable negative going transition.
H = HIGH Voltage Level
L = LOW Voltage Level

Logic Diagram (1/4 of diagram shown)



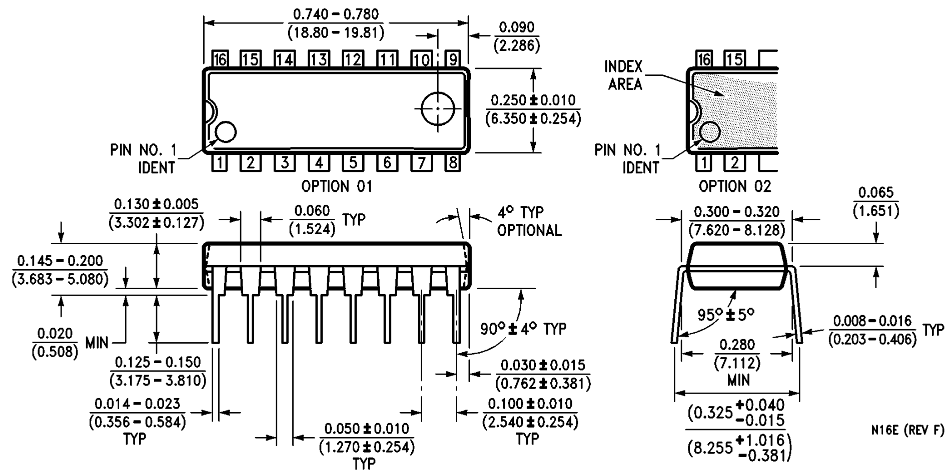
TL/F/9830–3

Physical Dimensions inches (millimeters)



16-Lead Small Outline Molded Package (M)
Order Number DM74LS375M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS375N
NS Package Number N16E

LIFE SUPPORT POLICY

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March 1998

DM74LS377
Octal D Flip-Flop with Common Enable and Clock

General Description

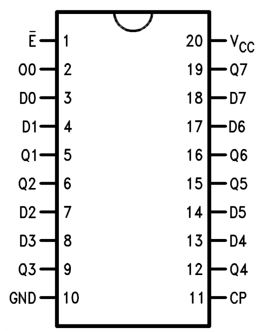
The 'LS377 is an 8-bit register built using advanced low power Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered common input enable. The device is packaged in the space-saving (0.3 inch row spacing) 20-pin package.

Features

- 8-bit high speed parallel registers
- Positive edge-triggered D-type flip-flops
- Fully buffered common clock and enable inputs

Connection Diagram

Dual-In-Line Package



DS009831-1

Order Number DM54LS377E, DM54LS377J, DM54LS377W, DM74LS377WM or DM74LS377N
See Package Number
E20A, J20A, M20B, N20A or W20A

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q7	Flip-Flop Outputs

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	DM54LS377			DM74LS377			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to CP	20 20			10 10			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to CP	5.0 5.0			5.0 5.0			ns
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{E}$ to CP	10 20			10 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5.0 5.0			5.0 5.0			ns
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 20			20 20			ns

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5			V
		V_{IL} = Max	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54			0.4	V
		V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−20		−100	mA
		(Note 3)	DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				28	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25˚C

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH}	Propagation Delay		25	ns
t_{PHL}	CP to Q_n		25	

Functional Description

The 'LS377 consists of eight edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable input ($\overline{E}$) are common to all flip-flops.

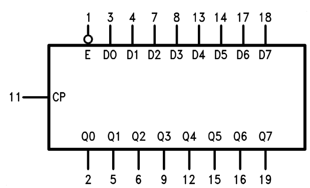
When $\overline{E}$ is LOW, new data is entered into the register on the next LOW-to-HIGH transition of CP. When $\overline{E}$ is HIGH, the register will retain the present data independent of the CP.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	X	X	No Change
L	↗	H	H
L	↗	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

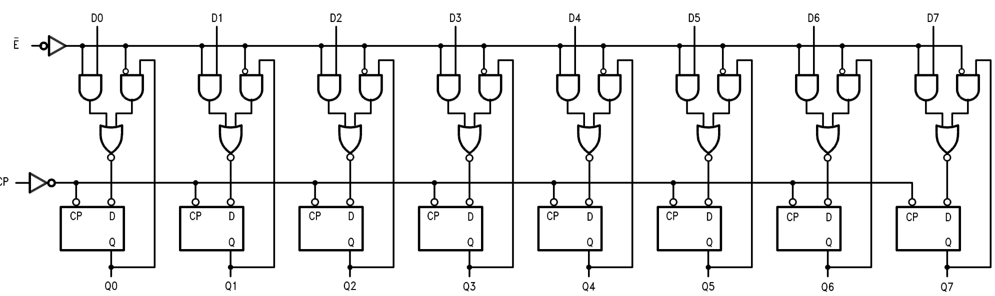
Logic Symbol



DS009831-2

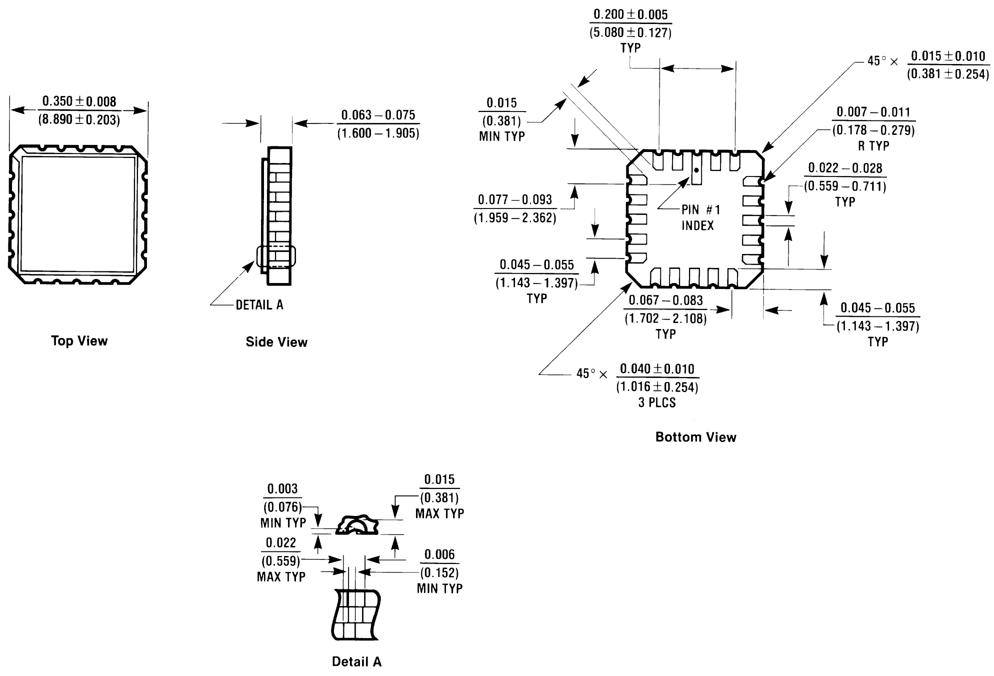
V_{CC} = Pin 20
GND = Pin 10

Logic Diagram



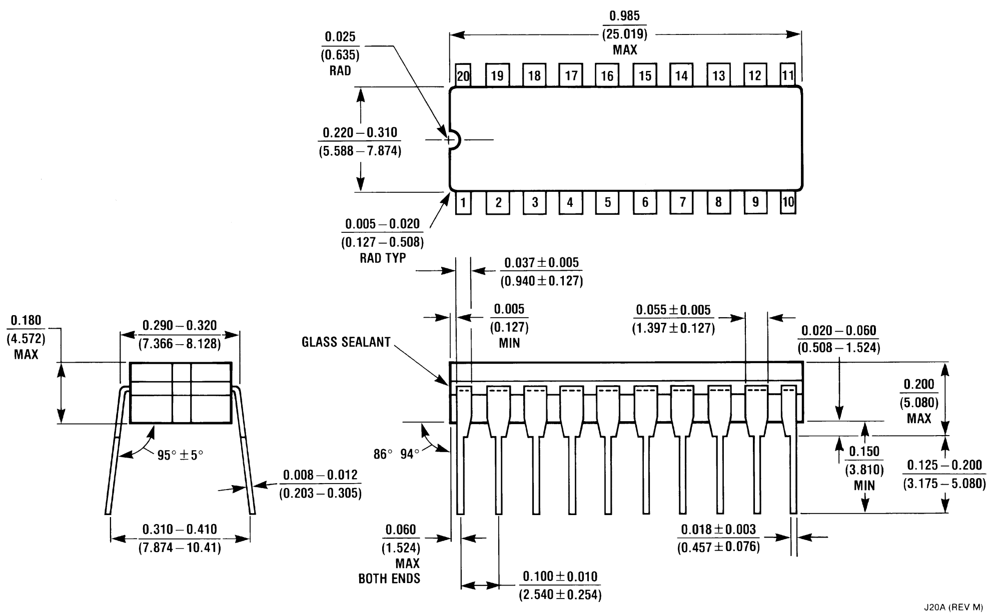
DS009831-3

Physical Dimensions inches (millimeters) unless otherwise noted

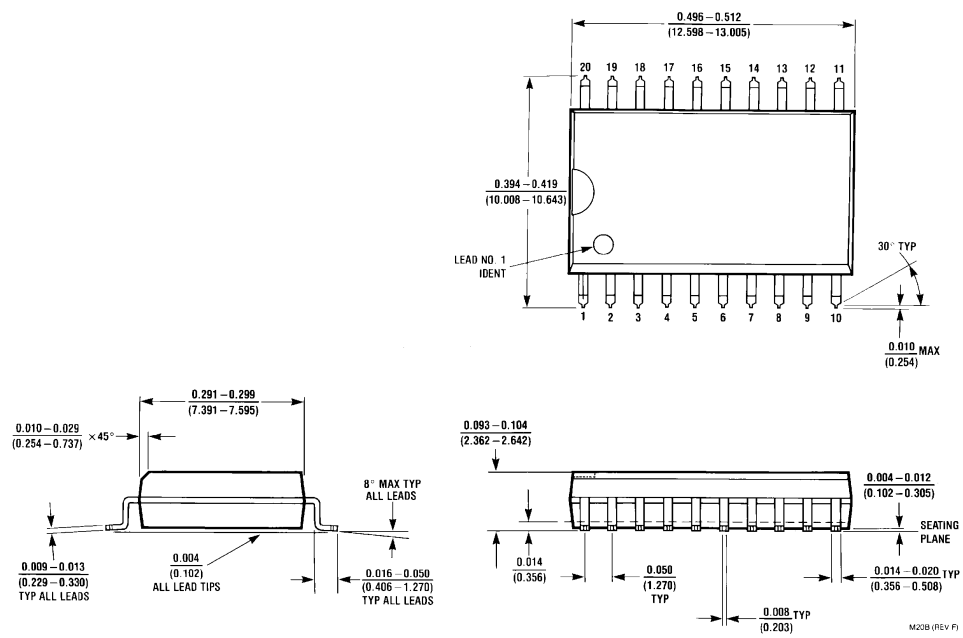


Ceramic Leadless Chip Carrier (E)
Order Number DM54LS377E
Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

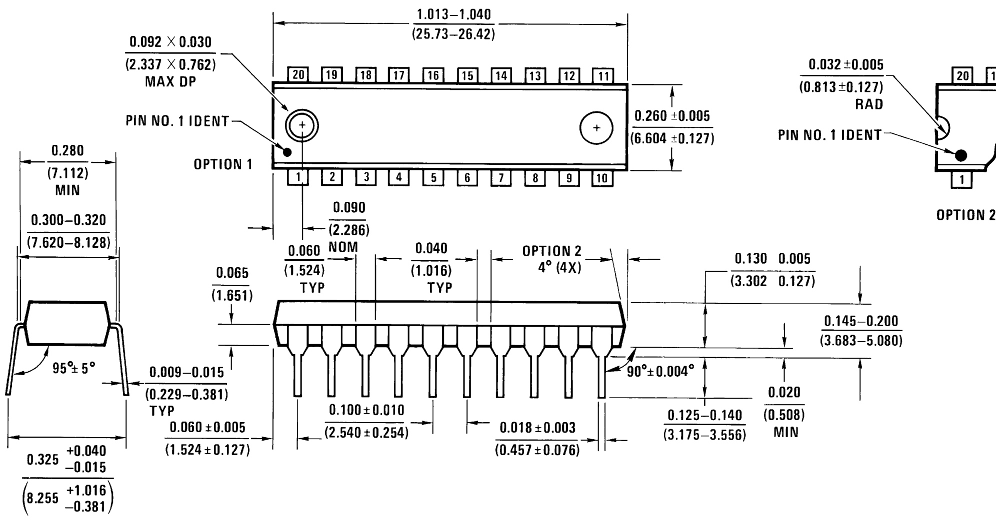


20-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS377J
Package Number J20A

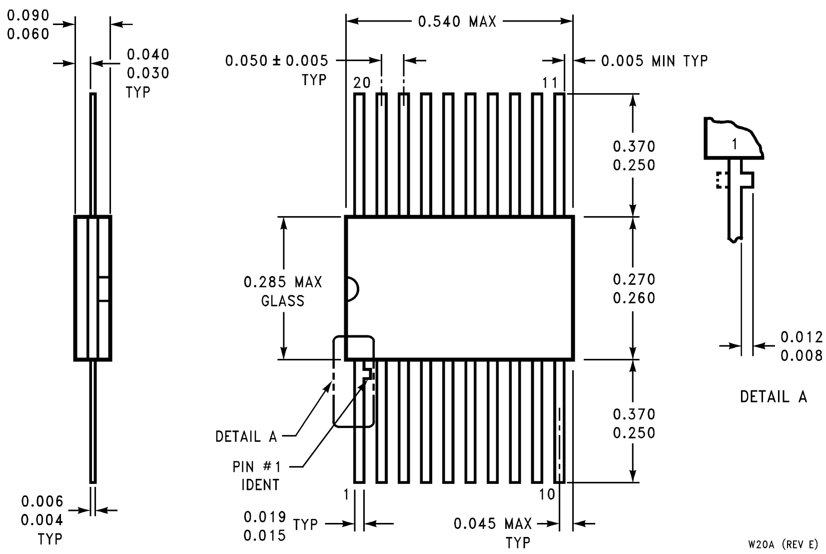


20-Lead Wide Small Outline Molded Package (M)
Order Number DM74LS377WM
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS377N
Package Number N20A



20-Lead Ceramic Flat Package (W)
Order Number DM54LS377W
Package Number W20A

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National Semiconductor

May 1992

DM54LS378/DM74LS378 Parallel D Register with Enable

General Description

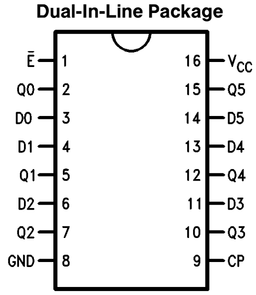
The 'LS378 is a 6-bit register with a buffered common enable. This device is similar to the 'LS174, but with common Enable rather than common Master Reset.

Features

- 6-bit high speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high speed termination effects
- Full TTL and CMOS compatible

Connection Diagram

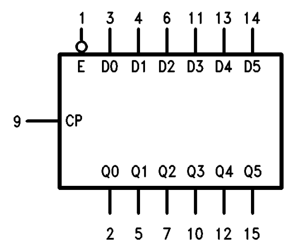
Dual-In-Line Package



TL/F/9832–1

Order Number DM54LS378E, DM54LS378J, DM74LS378M, DM74LS378N or DM54LS378N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



TL/F/9832–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\bar{E}$	Enable Input (Active LOW)
D0–D5	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q5	Flip-Flop Outputs

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−54°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS378			DM74LS378			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H)	Setup Time HIGH, D_n to CP	20			20			ns
t_h (H)	Hold Time HIGH, D_n to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, D_n to CP	20			20			ns
t_h (L)	Hold Time LOW, D_n to CP	5.0			5.0			ns
t_s (H)	Setup Time HIGH, $\overline{E}$ to CP	30			30			ns
t_h (H)	Hold Time HIGH, $\overline{E}$ to CP	5.0			5.0			ns
t_s (L)	Setup Time LOW, $\overline{E}$ to CP	30			30			ns
t_h (L)	Hold Time LOW, $\overline{E}$ to CP	5.0			5.0			ns
t_w (H)	CP Pulse Width HIGH	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_I = 10V	DM54				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20.0	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max D_n; $\overline{E}$ = GND, CP =				22	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$

Symbol	Parameter	2 kΩ, C_L = 15 pF		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n		27 27	ns

Functional Description

The 'LS378 consists of eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

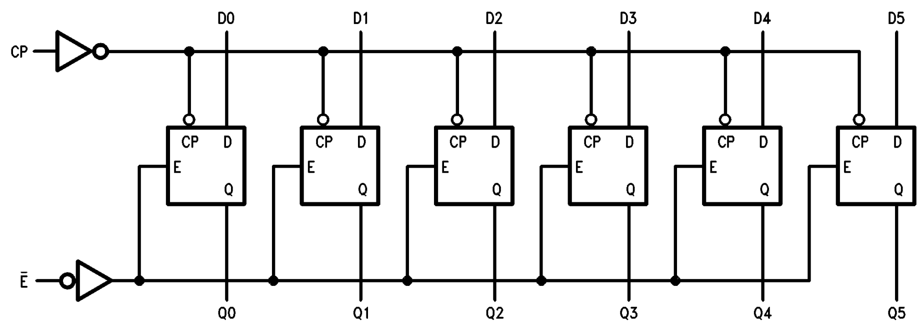
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\overline{E}$	CP	D_n	Q_n
H	↗	X	No change
L	↗	H	H
L	↗	L	L

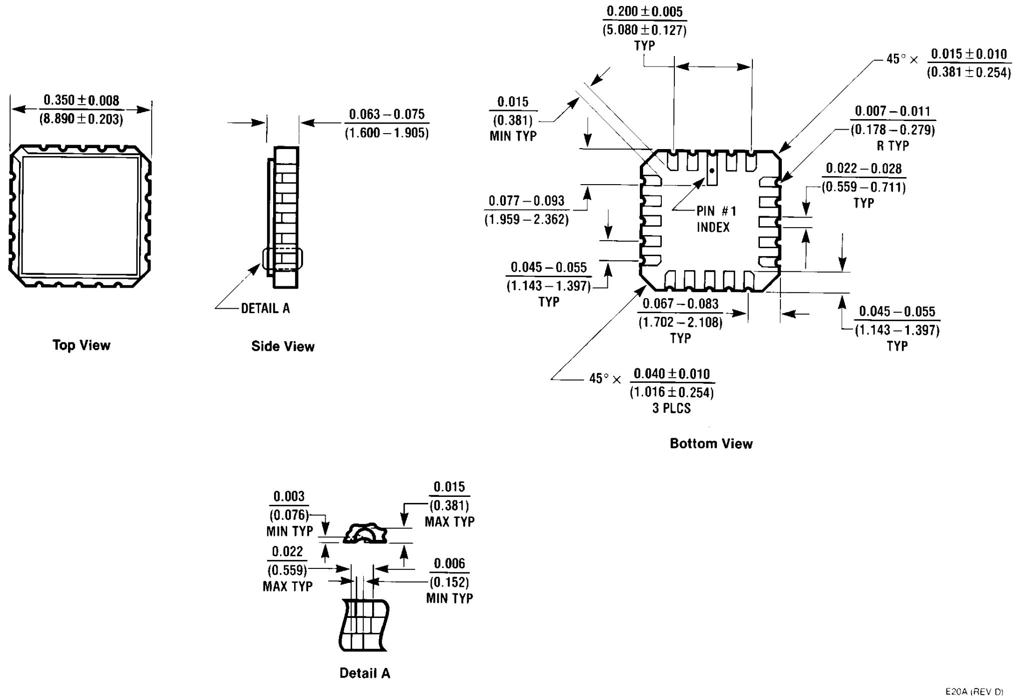
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

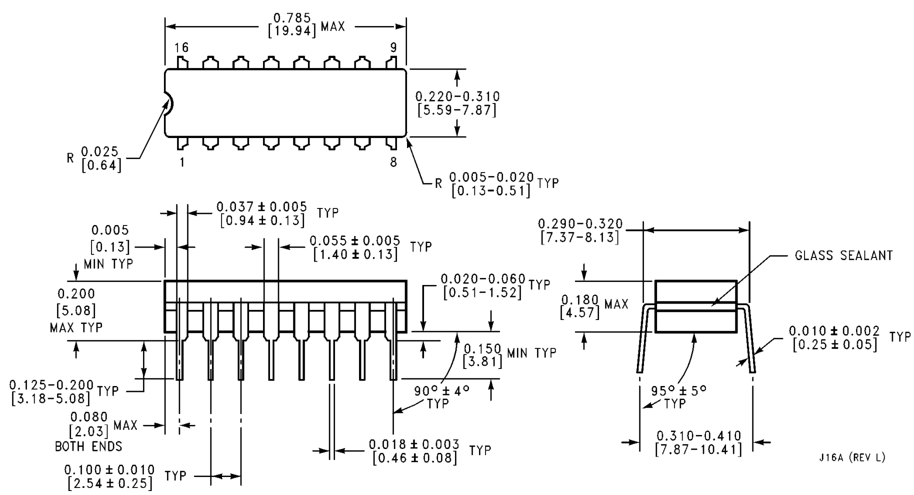


TL/F/9832-3

Physical Dimensions inches (millimeters)

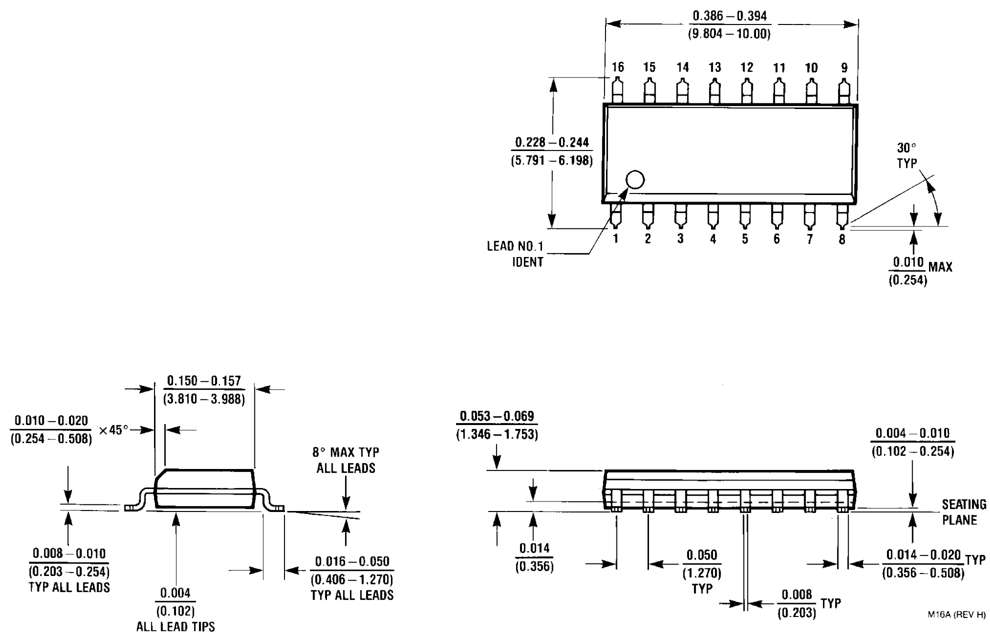


20 Terminal Ceramic Leadless Chip Carrier (E)
Order Number DM54LS378E
NS Package Number E20A

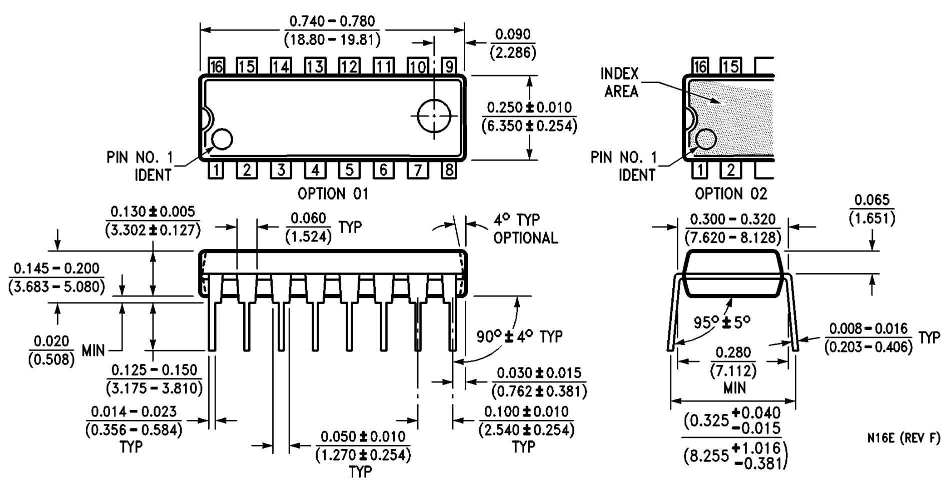


16-Lead Ceramic Dual-In-Line Package (J)
Order Number DM54LS378J
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)

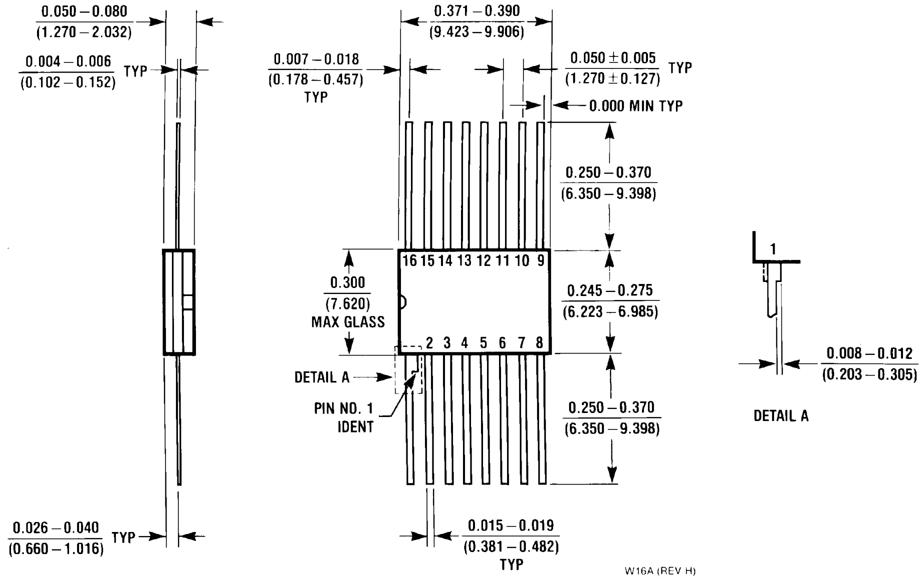


16-Lead Small Outline Molded Package (M)
Order Number DM74LS378M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS378N
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number DM54LS378W
NS Package Number W16A

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National Semiconductor

June 1989

54LS379/DM74LS379
Quad Parallel Register with Enable

General Description

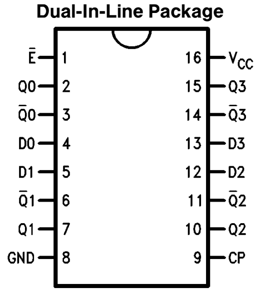
The LS379 is a 4-bit register with buffered common Enable. This device is similar to the LS175 but features the common Enable rather than common Master Reset.

Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- Buffered common enable input
- True and complement outputs

Connection Diagram

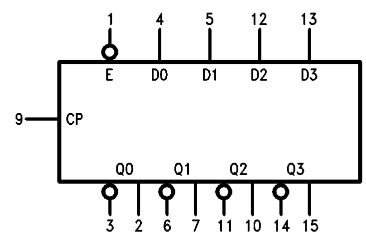
Dual-In-Line Package



TL/F/10186–1

Order Number 54LS379DMQB, 54LS379FMQB, 54LS379LMQB, DM74LS379M or DM74LS379N
See NS Package Number E20A, J16A, M16A, N16E or W16A

Logic Symbol



TL/F/10186–2

V_{CC} = Pin 16
GND = Pin 8

Pin Names	Description
$\overline{E}$	Enable Input (Active LOW)
D0–D3	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
Q0–Q3	Flip-Flop Outputs
$\overline{Q}0$–$\overline{Q}3$	Complement Outputs

 TL/F/10186 RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS379			DM74LS379			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s(H) t_s(L)	Setup Time HIGH or LOW Dn to CP	20			20			ns
t_h(H) t_h(L)	Hold Time HIGH or LOW Dn to CP	5			5			ns
t_s(H) t_s(L)	Setup Time HIGH or LOW $\overline{E}$ to CP	25			25			ns
t_h(H) t_h(L)	Hold Time HIGH or LOW $\overline{E}$ to CP	5			5			ns
t_w(L)	CP Pulse Width LOW	17			17			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5			V
			DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} Min, I_{OL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74			0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				18	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Note more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

$V_{CC} = +5.0V$, $T_A = +25°C$ (See Section 1 for test waveforms and output load)

Symbol	Parameter	$R_L = 2\ k\Omega$, $C_L = 15\ pF$		Units
		Min	Max	
f_{max}	Maximum Clock Frequency	30		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Qn		27 27	ns

Functional Description

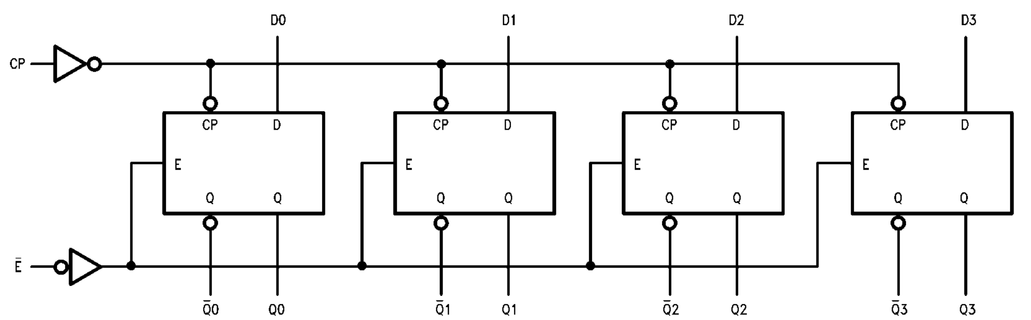
The LS379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. The Dn and $\overline{E}$ inputs can change when the clock is in either state, provided that the recommended setup and hold times are observed.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	Dn	Qn	$\overline{Q}$n
H	↗	X	No Change	No Change
L	↗	H	H	L
L	↗	L	L	H

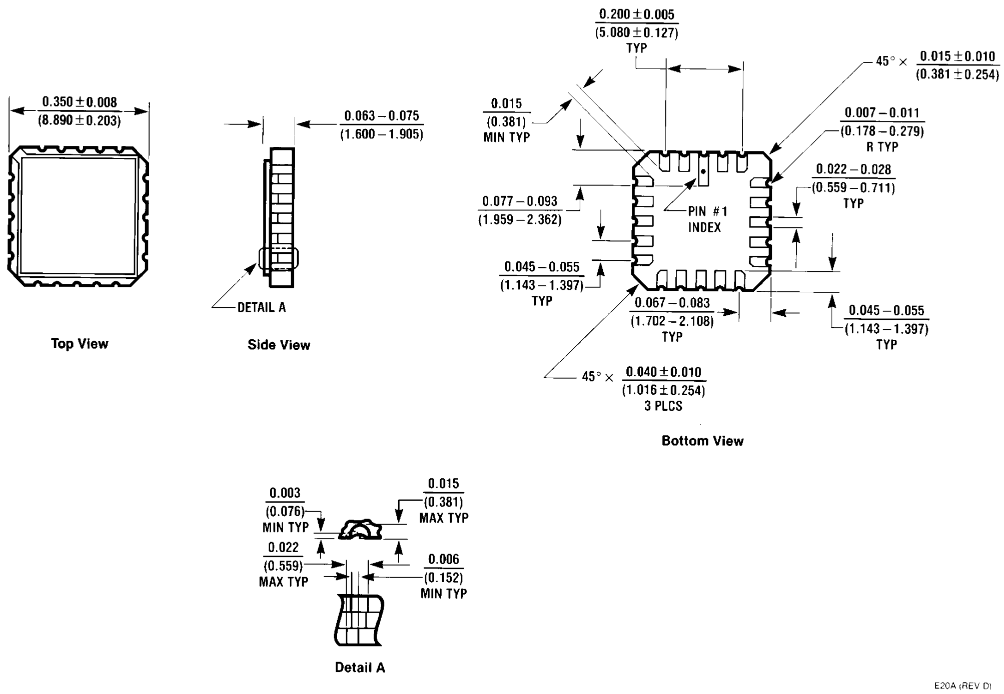
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram

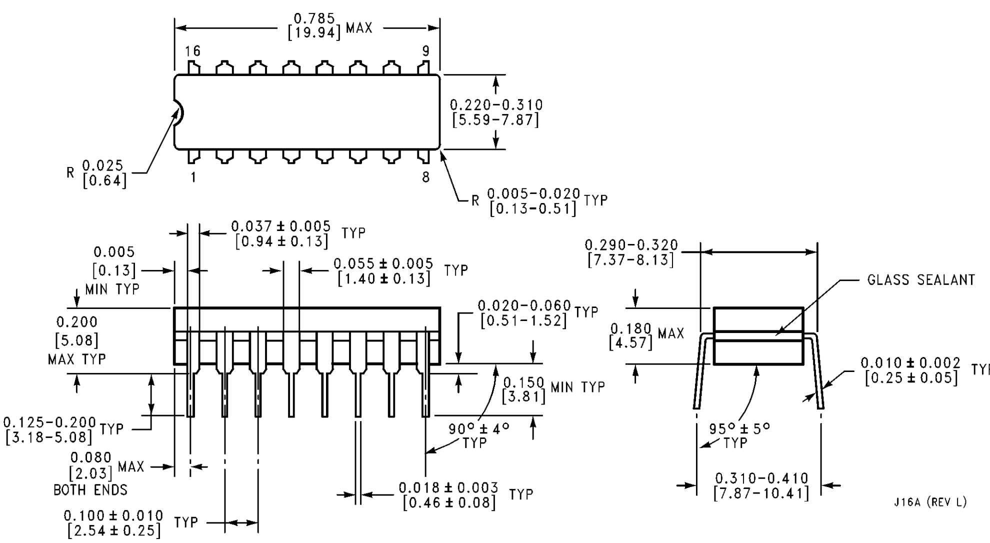


TL/F/10186–3

Physical Dimensions inches (millimeters)

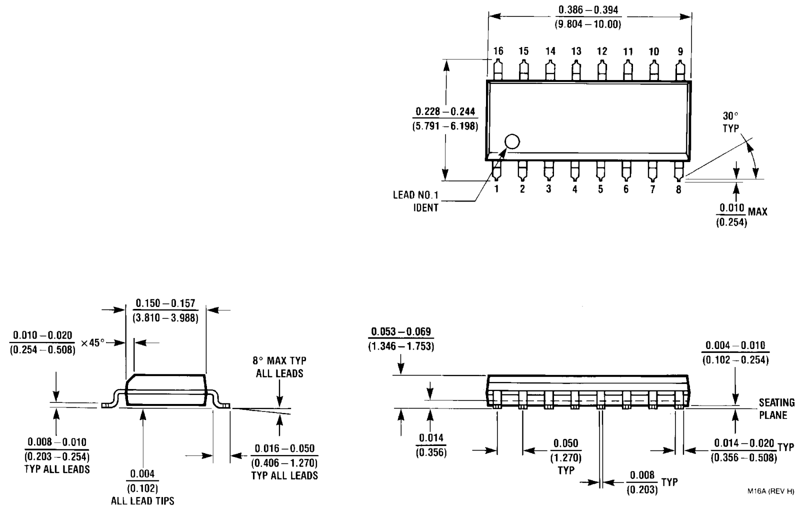


Ceramic Leadless Chip Carrier Package (E)
Order Number 54LS379LMQB
NS Package Number E20A

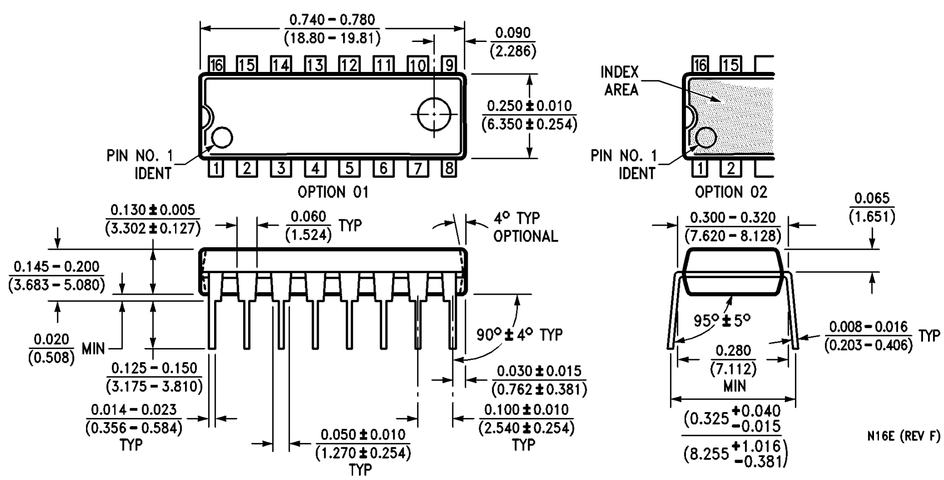


16-Lead Ceramic Dual-In-Line Package (J)
Order Number 54LS379DMQB
NS Package Number J16A

Physical Dimensions inches (millimeters)

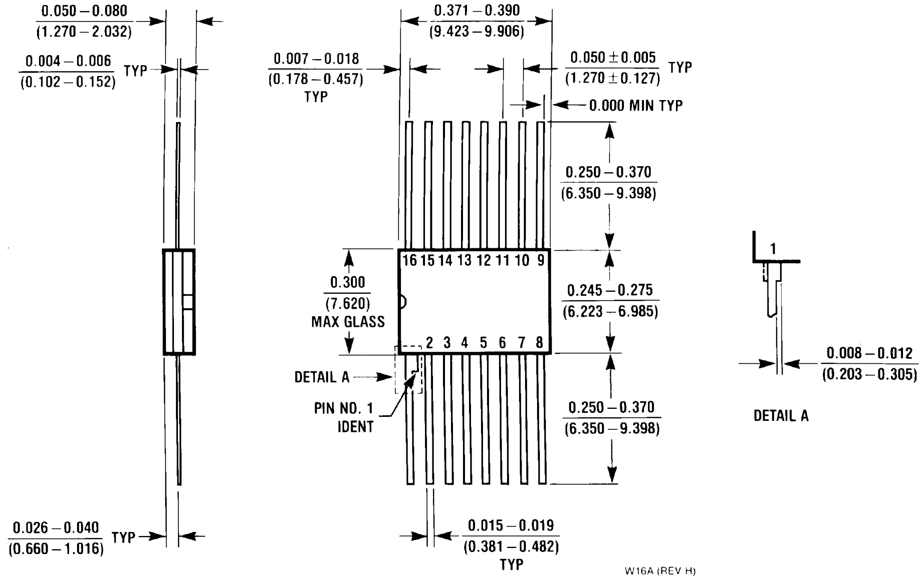


16-Lead Small Outline Molded Package (M)
Order Number DM74LS379M
NS Package Number M16A



16-Lead Molded Dual-In-Line Package (N)
Order Number DM74LS379N
NS Package Number N16E

Physical Dimensions inches (millimeters)



16-Lead Ceramic Flat Package (W)
Order Number 54LS379FMQB
NS Package Number W16A

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National Semiconductor

July 1989

DM54LS380/74LS380 Multifunction Octal Register

General Description

The 'LS380 is an 8-bit synchronous register with parallel load, load complement, preset, clear, and hold capacity. Four control inputs ($\overline{LD}$, POL, $\overline{CLR}$, $\overline{PR}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK). The LS380 combines the features of the LS374, LS377, LS273 and LS534 into a single 300 mil wide package.

The LOAD operation loads the inputs (D_7-D_0) into the output register (Q_7-Q_0), when POL is HIGH, or loads the compliment of the inputs when POL is LOW. The CLEAR operation resets the output register to all LOWs. The PRESET operation presets the output register to all HIGHs. The HOLD operation holds the previous value regardless of clock transitions. CLEAR overrides PRESET, PRESET overrides LOAD, and LOAD overrides HOLD.

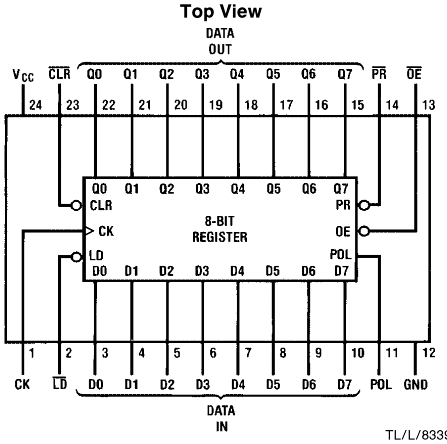
The output register (Q_7-Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus interface standards.

Features/Benefits

- Octal Register for general purposes interfacing applications
- 8 bits match byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- TRI-STATE® outputs
- Low current PNP inputs reduce loading

Connection Diagram

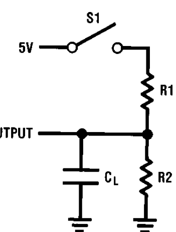
Top View



TL/L/8339-1

Order Number DM54LS380J, DM74LS380J or DM74LS380N
See NS Package Number J24F or N24C

Standard Test Load



TL/L/8339-2

Function Table

$\overline{OC}$	CLK	$\overline{CLR}$	$\overline{PR}$	$\overline{LD}$	POL	D7-D0	Q7-Q0	Operation
H	X	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	X	X	L	CLEAR
L	↑	H	L	X	X	X	H	PRESET
L	↑	H	H	H	X	X	Q	HOLD
L	↑	H	H	L	H	D	D	LOAD true
L	↑	H	H	L	L	D	$\overline{D}$	LOAD comp

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65° to +150°C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125*	0		75	°C
t_w	Width of Clock	High	40			40			ns
		Low	35			35			
t_{SU}	Set-Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

*Case temperature

Electrical Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = MAX	V_I = 0.4V				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC} = MAX	V_I = 2.4V				25	μA
I_I	Maximum Input Current	V_{CC} = MAX	V_I = 5.5V				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OL} = 12 mA			0.5	V
			COM	I_{OL} = 24 mA				
V_{OH}	High-Level Output Voltage	V_{CC} = MIN, V_{IL} = 0.8V, V_{IH} = 2V	MIL	I_{OH} = −2 mA	2.4			V
			COM	I_{OH} = −3.2 mA				
I_{OZL}	Off-State Output Current	V_{CC} = MAX, V_{IL} = 0.8V, V_{IH} = 2V		V_O = 0.4V			−100	μA
I_{OZH}				V_O = 2.4V			100	μA
I_{OS}	Output Short-Circuit Current*	V_{CC} = 5.0V		V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = MAX				120	180	mA

* No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

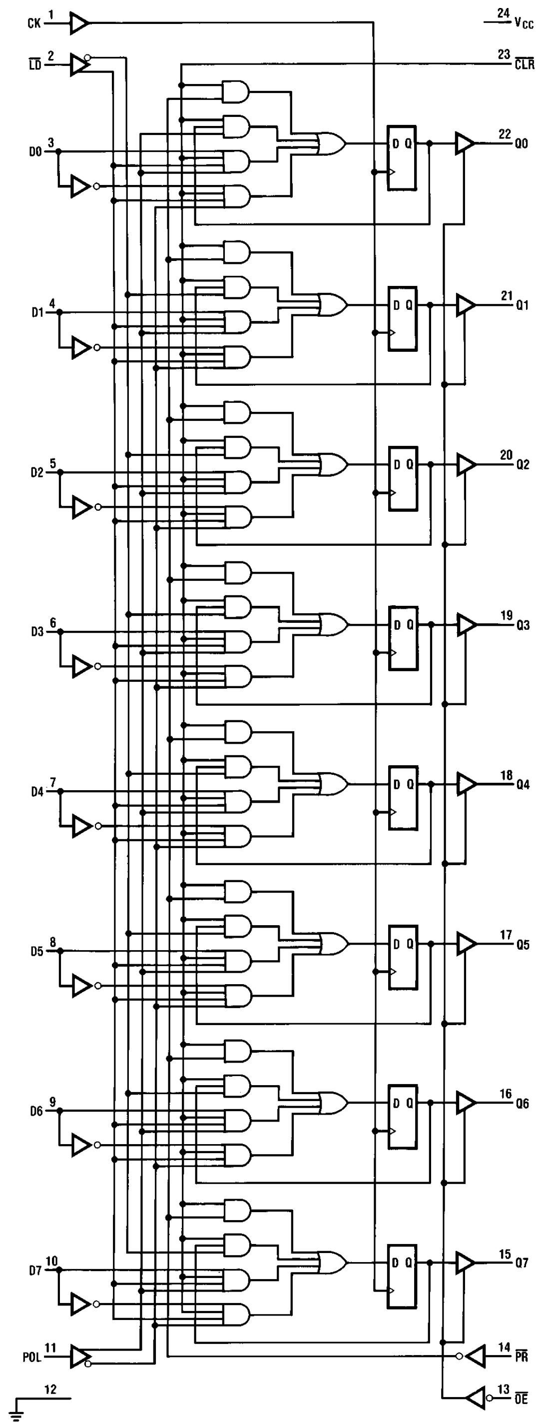
† All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency	C_L = 50 pF, R_1 = 200Ω, R_2 = 390Ω	10.5			12.5			MHz
t_{PD}	Clock to Q			20	35		20	30	ns
t_{PZX}	Output Enable Delay			35	55		35	45	ns
t_{PXZ}	Output Disable Delay			35	55		35	45	ns

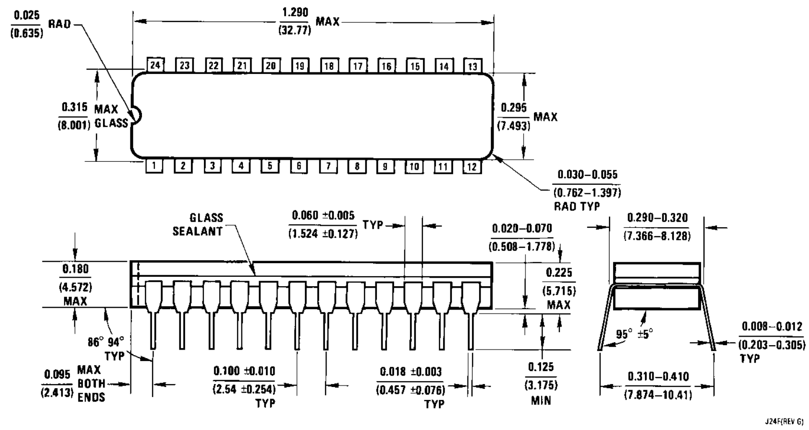
Logic Diagram

Octal Register

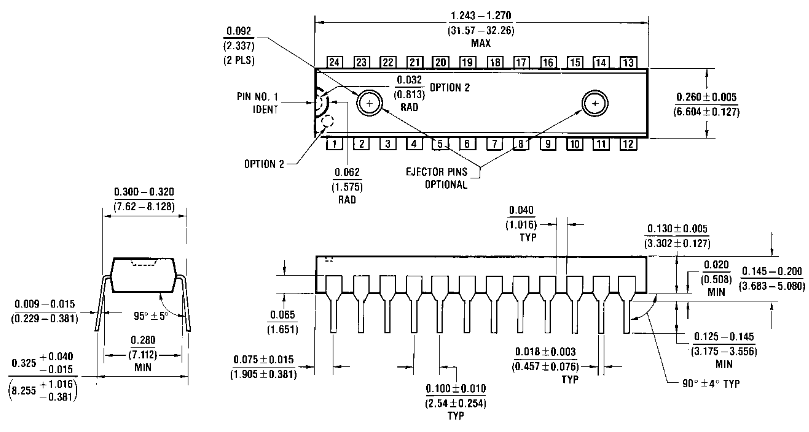


TL/L/8339–4

Physical Dimensions inches (millimeters)



24-Pin Narrow Ceramic Dual-In-Line Package (J)
Order Number DM54LS380J or DM74LS380J
NS Package Number J24F



24-Pin Narrow Plastic Dual-In-Line Package (N)
Order Number DM74LS380N
NS Package Number N24C

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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